A Peak 1.2MHz, >99.5% Efficiency, and >10kW/L Power Density Soft-Switched Inverter for EV Fast Charging Applications

Matthew Jahnes, *Student Member, IEEE*, Liwei Zhou, *Member, IEEE*,
Youssef Fahmy, *Student Member, IEEE*, and Matthias Preindl, *Senior Member, IEEE*

***Abstract*—A >99.5% efficient grid-tied inverter with peak values of 30kW power, 13.7kW/L volumetric power density, 10.17kW/kg gravimetric power density, and 1.2MHz switching frequency is proposed in this paper. This union of high efficiency and high power density is achieved through a unique combination of technologies and is maximally leveraged through an $\eta\rho$ optimization. The first is a variable frequency critical soft-switching (VFCSS) scheme that allows the converter to maintain soft-switching over all permissible load conditions. This enables a simultaneous increase of the switching frequency and a decrease of the inductance without penalizing efficiency. The second technology is an additional capacitance placed across the drain-source terminals of each FET. This can allow for over a 40% reduction in turn-off losses at the expense of an increase in the required dead time. The last technology is a simple open-loop duty cycle compensation scheme that effectively mitigates the distortion caused by the combination of high switching frequencies and large dead times. An $\eta\rho$ optimization process with its associated volume and loss estimations are provided. A brief discussion on the control of the converter is shown followed by a description of the constructed physical prototype. Lastly, experimental results showing efficiency, rated power operation, total harmonic distortion, and transient load steps are provided for a grouping of different grid voltages.**

***Index Terms*—AC/DC, Power Converter, Inverter, SiC, Density, Efficiency.**

I. Introduction

High performance Electric Vehicles (EVs), of all types and mediums in which they travel, benefit from dense and efficient power electronics. Electric vehicle range is one of the key barriers preventing mass adoption of EVs, especially in rural areas [1], and is a characteristic where EVs fall short when compared to their internal combustion counterparts. One way of increasing the range is by maximizing the efficiency of the power conversion devices in the vehicle. This allows for more prudent use of the vehicles limited energy storage, increasing its range and/or relaxing the requirements on energy storage devices. High efficiency is also important for stationary EV chargers, most notably vehicle-to-grid (V2G) applications where round-trip efficiency is emphasized [2].

Equally important to EVs is the power density, both gravimetric and volumetric. These applications typically relate to but are not limited to mobile vehicular power electronics. This includes on-board chargers (OBC) for electric vehicles (EVs) [3], [4], which is becoming increasingly important as the mass-adoption of EVs continues [5]. Some OBCs are also reconfigurable as traction inverters, further emphasizing the importance of both power density and efficiency [6].

Other vehicles, such as airplanes and boats, also drive the market for high efficiency and high power density converters [7]–[10]. The reasoning is two-fold, better efficiency results in more range, and higher power density results in better vehicle dynamics [11], [12]. A concurrent improvement in both results in a better vehicle, and the push for simultaneous improvement in both power density and efficiency persists.

This paper pertains to the simultaneous improvement of both power density and efficiency with a specific target application of EV fast charging. It is often the case where there is a trade-off between power density and efficiency [13], [14] and improvements in one area require a sacrifice in the other. This is disadvantageous to many applications where both high efficiency and high power density are prioritized, such as the aforementioned vehicular applications. The quick charging times desired by EV consumers demand higher efficiency, power density, and overall power levels from their associated chargers.

There are a range of existing approaches to increasing both power density and efficiency. They can broadly be split between two areas: mechanical improvements and electrical improvements. Mechanical improvements include novel packaging/layout methods [34]–[36] and heatsink designs/heat rejection methods [37]–[39] that allow for a reduction in

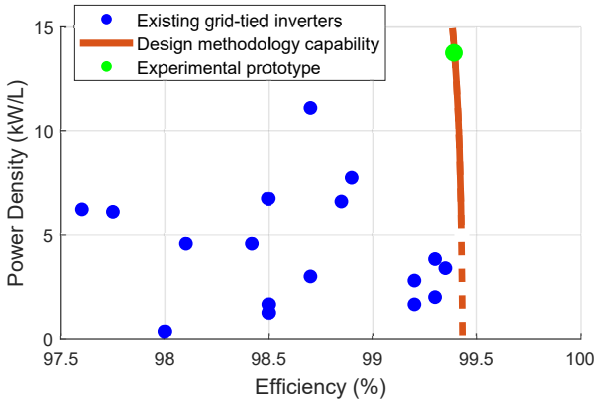

Fig. 1. Efficiency vs. power density comparison of current state-of-the-art converters and the proposed design methodology and experimental prototype [15]–[33].

Manuscript received 18 June 2023; revised 21 September 2023.

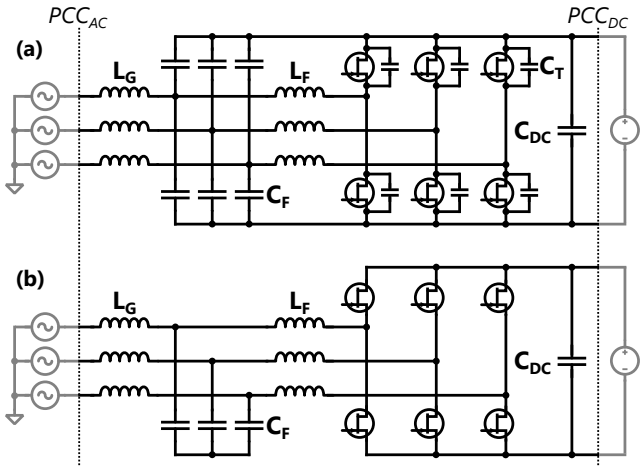

Fig. 2. (a): Topology of the proposed grid-tied inverter. (b): Typical grid-tied inverter topology.

volume and/or weight. An increase in the allowable heat rejection can also accompany an increase in the power level, further increasing the power density.

Electrical improvements come in the form of topological improvements [40], [41], semiconductor technology improvements [42], [43], and switching scheme improvements [44]. Semiconductor technology improvements, like the advent of Silicon Carbide (SiC) and Gallium Nitride (GaN) wide-badgap devices, have allowed for the simultaneous improvement of both power density and efficiency through their decreased switching loss, conduction loss, and increased permissible junction temperatures [42]. Soft-switching techniques, both hardware [43], [45] and software regulated [44], [46], have also been shown to reduce switching loss, allowing for an increase in switching frequency and an associated decrease in passive filter volume, benefiting both efficiency and power density.

Lastly, a common technique to maximally leverage these approaches is the formulation of an $\eta\rho$ Pareto frontier, which is an optimization process that allows for the simultaneous balancing of maximum efficiency (η) and maximum power density (ρ) [47]. Not all $\eta\rho$ optimizations are identical, with some having varying loss estimation techniques and volume estimation methods [48], [49]. Varying methods aside, a formal approach is necessary to optimally balance the multitude of parameters involved with power converter design.

A visualization of the power densities and efficiencies that have been achieved in current state-of-the-art grid-tied inverters can be seen in Fig. 1. These are all inverters that use a range of different efficiency, power density, and $\eta\rho$ optimization techniques. Also included in this figure is the Pareto frontier generated using the proposed techniques and the experimentally achieved η and ρ values. This shows that the efficacy of the proposed method as well as the achieved experimental results are beyond the current state-of-the-art.

The performance of the proposed inverter is achieved through a unique combination of methods. First is the variable frequency switching scheme, previously proposed in [50], that allows for soft-switching to be maintained over all loads

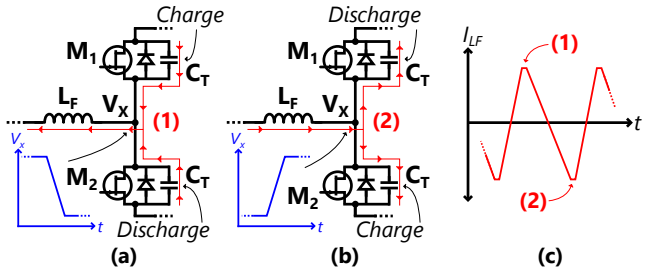

Fig. 3. Current paths that charge and discharge the additional drain-source capacitance C_T during soft-switching transients. (a): Upper turn-off and lower turn-on transient. (b): Upper turn-on and lower turn-off transient.

and operating conditions along with a substantial increase in switching frequency and decrease in filter inductance.

Second is the inclusion of an additional capacitance placed across the drain-source terminals of each FET which substantially decreases the turn-off energy, a technique commonly used in soft-switching converters [51]. To maintain soft-switching with this increased drain-source capacitance, a larger than typical dead time is required. This large dead time in conjunction with a high switching frequency has the potential to significantly distort the applied duty cycles.

The last technology is a simple open-loop duty cycle compensation scheme that mitigates the distortion that arises from the combination of high switching frequency and large dead times. The novelty of the proposed is in the unique combination of these three methods and the resulting improvement over the state-of-the-art with respect to power density and efficiency.

This paper is organized as follows: First, the overall topology is shown. The theory behind the proposed grouping of technologies as well as an $\eta\rho$ optimization that fully leverages them is provided. The resulting $\eta\rho$ Pareto Frontier is shown, an operating point selected, and a prototype 3-phase grid-tied inverter constructed. Lastly, experimental efficiency, distortion, and transient results are given. The overarching goal is to present a formulaic approach to maximize power density and efficiency for a given set of converter parameters using the proposed combination of technologies.

II. Topology

The topology of the proposed 3-phase grid-tied inverter consists of three half-bridges, one for each phase leg, and can be seen in Fig. 2-(A). There are notable differences between the proposed and the typical 3-phase grid-tied inverter topology of Fig. 2-(B). The most significant difference is the connection of the filter capacitors C_F, which in a typical grid-tied inverter topology have their star point left floating. The proposed makes two modifications: first the filter capacitor is split into two equal capacitors, an upper and lower capacitor. Second, the star-point of these capacitors is then connected back to the switches, the upper capacitors to the positive DC link and the lower capacitors to the negative DC link.

This has two beneficial effects. The connection of the star point of the filter capacitors back to the inverter allows for the common-mode voltage of these capacitors to be controlled.

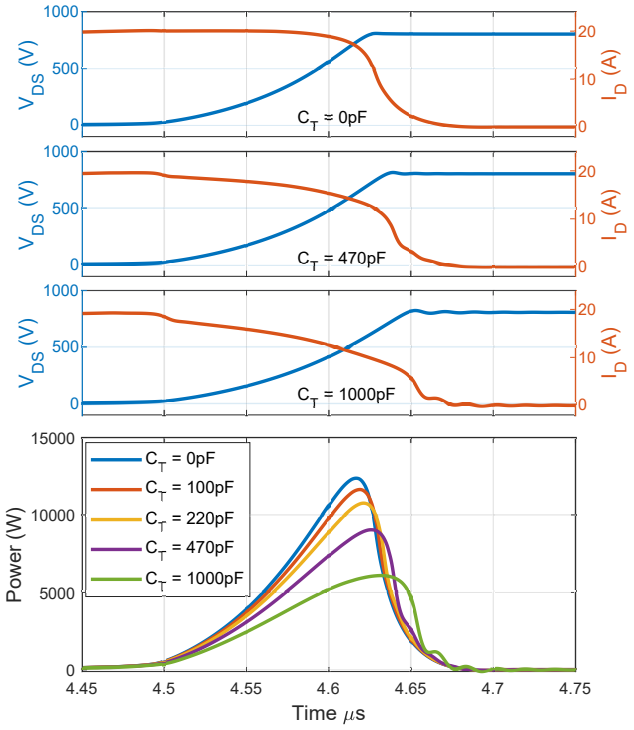

Fig. 4. Effect of C_T on turn-off switching energies. The top three plots show turn off voltage and current transients for different C_T values. The bottom plot shows the instantaneous power loss during turn-off switching transients for a grouping of C_T values.

Controlling the common-mode in this manner has marked EMI benefits and leakage current benefits [52]. In motor drive applications it can be used to significantly reduce the bearing currents [6], [53], and, although not implemented in this paper, harmonics can be injected into this common-mode that can be used to reduce both the required DC link voltage [54] and capacitance [55].

Splitting filter capacitance C_F also serves to partially cancel out ripple currents that otherwise would have been forced to be absorbed by the filter capacitances C_F and DC link capacitance C_{DC}. DC link ripple currents and output ripple currents can circulate through the upper C_F that connects them together and a portion of these currents will cancel. This has the effect of improving conducted EMI and reducing the required total capacitance of the inverter. More information on this upper capacitance can be found in [56].

The last topology modification is the addition of external drain-source capacitance C_T. This capacitance is leveraged to reduce the overall switching loss of the converter and is discussed in detail in the following section.

III. Additional FET Drain-Source Capacitance

As described in [51], an external capacitance connected across the drain-source terminals, shown in Fig. 2-(A), can be used to reduce the turn-off losses of the FET. This capacitance slows the V_{DS} rise time during the turn off transient, effectively reducing the non-zero V_{DS} and I_D overlap by spreading it out. This effect can be seen in Fig. 4, where the turn-off losses for a CREE C3M0032120k SiCFET with a grouping of

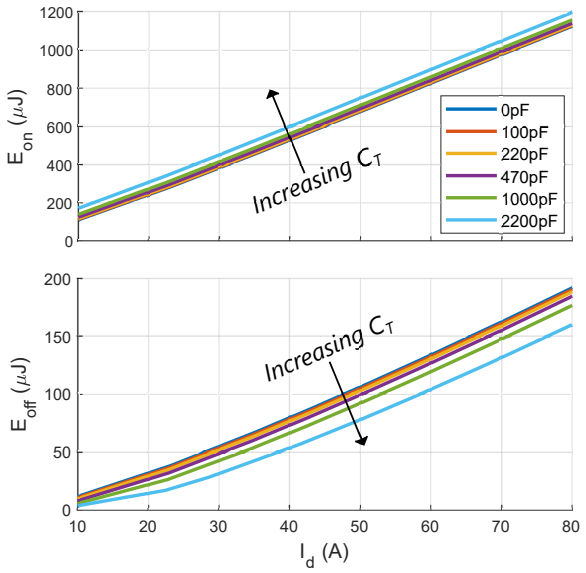

Fig. 5. 800V switching energies for a range of I_d currents and a grouping of C_T capacitances.

C_T values are found using the double pulse testing method at a temperature of 25°C.

It is important to note that Fig. 4 considers only the drain current of the FET which does not include the current through C_T, and therefore the resulting switching energies do not include the energy stored in C_T. The energy stored in C_T gets recovered during the discharging process and is not dissipated in the circuit. This is also true for the intrinsic drain-source capacitance of the FET C_{oss}, however, the current used to charge and discharge C_{oss} is included in the drain current I_D of Fig. 4 as it is not practical to disaggregate it. The shown switching energies reflect this and as a result should be considered an upper bound on what the actual switching energies are. In Fig. 4, the turn-off energies for $C_T = 470$pF and $C_T = 1000$pF are 82% and 65%, respectively, of the turn-off energy for $C_T = 0$pF.

There are two tradeoffs associated with increasing the drain-source capacitance. First is the turn-off transient switching time penalty that comes from the additional capacitance that needs to be charged and discharged during soft-switching. During the turn-off transient the drain-source capacitance is charged and discharged by by the inductor current I_{LF}. This can be visualized in Fig. 3 which shows the current paths for a turn-off transient. The dead time τ_d must be set to a value greater than this transition time to allow for the soft-switching to complete before the complementary switch is turned on.

Straightforward circuit analysis of Fig. 3 and the approximation that during the switching transient the inductor current is constant provides a switching transient time of

$$\Delta T_{com} = \frac{2C_{DS,eq}V_{bus}}{I_{LF,inst}}, \tag{1}$$

where ΔT_{com} is the switching transient time, $C_{DS,eq}$ is the effective drain-source capacitance of each FET and is equal to the sum of C_T, the intrinsic drain-source capacitance of the FET C_{oss}, and any parasitic capacitances of the PCB. V_{bus} is

the DC link voltage and $I_{LF,inst}$ is the instantaneous value of the inductor current during the switching transient. (1) is valid for switching instances where the energy stored in inductor L_F is much larger than the energy required to commutate the voltage of $C_{DS,eq}$. When this is not the case, a resonant transition must be assumed

$$\Delta T_{res} = \pi \sqrt{L_F C_{DS,eq}}, \tag{2}$$

where ΔT_{res} is the switching transient time during resonant transitions. Both (1) and (2) shows that the switching transient time is proportional to the effective output capacitance value $C_{DS,eq}$, (2) shows that it is also inversely proportional to the instantaneous inductor current.

Fig. 6 is a visualization of this trade-off where the inductor current is held constant at 20A for ΔT_{com}. Aan L_F value of $17\mu H$ and $C_{DS,eq}$ value equal to C_T are assumed for ΔT_{res} and the switching energies are found as a function of ΔT_{com}. The real ΔT value will be in between ΔT_{res} and ΔT_{com} with ΔT_{res} setting the upper bound.

It is shown that increasing the effective drain-source capacitance of the FET will reduce the turn-off loss of the FET during soft-switching. However, it will also increase the turn-on loss that is incurred during hard-switching. This is because the energy stored in the drain-source capacitance is dissipated within the FETs during hard-switching, while soft-switching allows for this energy to be recovered. Practically, increasing the drain-source capacitance will also increase the ringing during hard-switched transients, further increasing the hard-switching loss.

This tradeoff can be visualized in Fig. 5, where it can be seen that the decrease in turn-off switching energy is less than the increase in turn-on switching energy for a given value of additional drain-source capacitance C_T. Therefore, in order to avoid being penalized by the additional drain-source capacitance, a robust method for maintaining soft-switching must be implemented. This method is discussed in the following section.

IV. Variable Frequency Critical Soft-Switching

A variable switching frequency scheme is used to maintain soft-switching over the entire operating range of the inverter. This is critical to the inverter's functionality as soft-switching allows for the exchange of turn-on losses with turn-off losses

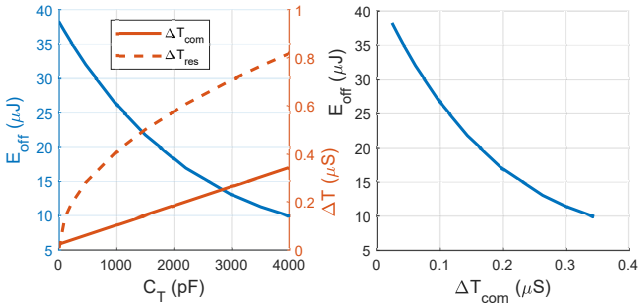

Fig. 6. Switching time, loss, and $C_{DS,eq}$ tradeoffs. (a): turn-off energy E_{off} vs. additional drain-source capacitance C_T. (b): E_{off} vs. switching time ΔT_{com}.

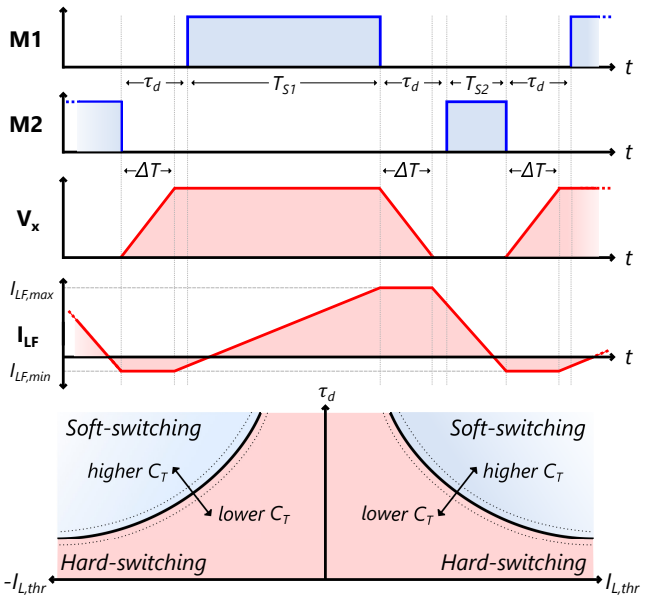

Fig. 7. Critical soft-switching boundaries. The top four plots show the FET gate signals, node V_x voltage, and filter inductor current values. The bottom plot shows the relationship between dead time τ_d, critical threshold current $I_{L,thr}$, and external FET drain-source capacitance C_T with respect to hard vs. soft-switching.

and the benefits of the additional drain-source capacitance can be fully leveraged as the converter will ideally never incur a turn-on loss. Turn-on losses are typically much greater than turn-off losses, further emphasizing the need to avoid hard-switching.

The Variable Frequency Critical Soft-Switching (VFCSS) scheme uses the switching frequency to control the filter inductor L_F ripple current. Soft-switching can be achieved if the peaks and valleys of the L_F current satisfy the soft-switching boundary condition of dead time τ_d and peak/valley inductor current. By controlling the switching frequency, the peaks and valleys of the L_F inductor current can be precisely placed such that this boundary condition is always satisfied.

The desired placement of the peak and valley points of the L_F inductor currents are set such that the valley point of the inductor current reaches a predetermined value of inductor threshold current $I_{L,thr}$. $I_{L,thr}$ is set in accordance with the aforementioned boundary condition which can be derived from the FET's total output capacitance $C_{DS,eq}$.

As discussed in Section III, the value of $C_{DS,eq}$ will effect the switching transient time ΔT. The dead time must be greater than the switching transient time ΔT to allow for zero voltage switching to occur before the complementary FET is turned on. If this does not occur, and the complementary FET turns on before the transient is complete, the FET will incur a partial hard turn-on loss and soft-switching will not be maintained.

The relationship between $I_{L,thr}$, ΔT, and the required dead time τ_d can be seen in Fig. 7. In the lowest plot of Fig. 7, soft-switching areas are highlighted in blue and hard-switching in red. The blue regions represent the areas of operation where there is sufficient time and current for commutating the output capacitances of the FETs before the complementary switch is

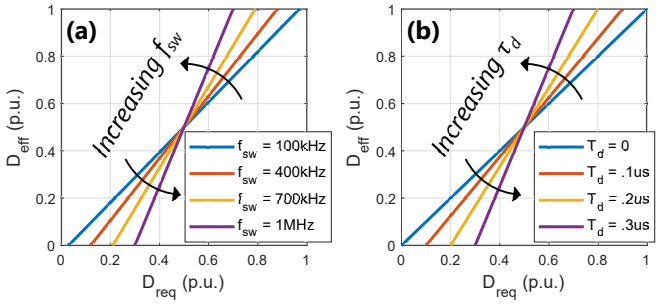

Fig. 8. Duty cycle distortion for a 1MHz switching frequency with a range of (a) switching frequency f_{sw} and (b) dead time τ_d values.

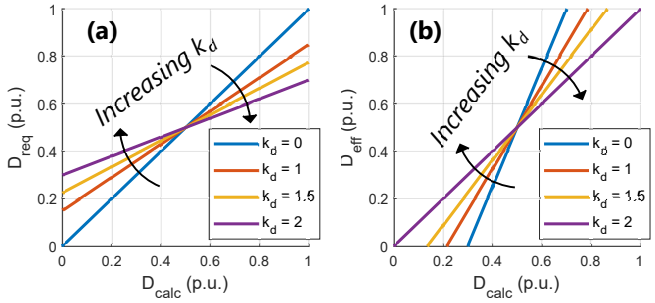

Fig. 10. Compensated duty cycle. (a): The requested duty cycle D_{req} as a function of calculated duty cycle D_{calc} and (b): the effective actuated duty cycle D_{eff} as a function of D_{calc} for varying k_d.

actuated.

For positive values of average L_F inductor current, the required current ripple needs to be set such that the valley point is lower than the negative threshold current level $-I_{L,thr}$. The negative inductor current will discharge the upper switch output capacitance in the turn-off transient period of the lower switch. Similarly, for negative values of average inductor current, the required current ripple needs to be set to ensure the peak inductor current point is higher than the positive threshold current $I_{L,thr}$. Soft-switching of the lower switch will be achieved if the lower switch output capacitance is fully discharged by the positive inductor current during the turn-off transient of the upper switch. The switching frequency to achieve the required current ripple for any arbitrary $I_{L,thr}$ value can be calculated with

$$f_{sw} = \frac{(1-D)DV_{dc}}{2(|I_{L,avg}| + I_{L,thr})L_f}, \tag{3}$$

where D is the duty cycle and $I_{L,avg}$ is the average value of the inductor L_F current. Over the entire grid cycle where the duty cycle and the average inductor current are dynamic, the value of inductor L_F will define the minimum switching frequency and hardware capability will define the maximum allowable switching frequency.

Practical implementations will require a relatively precise measurement of L_f. (3) is repetitively calculated by the controller in order to actuate the correct switching frequency to achieve critical soft-switching. If the value of L_f used in calculations is less than the actual value, the calculated f_{sw} will be higher than it needs to be, ultimately resulting in an inductor current ripple that is lower than it should be. The opposite is true for a measurement of L_f that is higher than it actually is. An inductor current that is smaller than desired can result in exiting the soft-switching region of operation and a subsequent (and potentially substantial) increase in loss. For this reason it is advisable to use the upper bound of the measurement range of L_f (in lieu of a precise L_f measurement) so VFCSS can be maintained despite any inaccuracies in the measurement of L_f.

When VFCSS is fully leveraged, it is often the case that the required f_{sw} is high for certain operating conditions. Simultaneously, the additional drain-source capacitance C_T increases the switching transient time ΔT, requiring large dead times. The combination of large dead times and high switching frequencies will result in a distortion. The following section describes a duty cycle compensation scheme which mitigates this distortion.

V. Duty Cycle Compensation Scheme

The additional output capacitance C_T will drive up the required dead time to maintain soft-switching. Simultaneously, the VFCSS scheme allows for a significant increase in switching frequency. Implementing both of these techniques simultaneously has the potential to significantly distort the actuated duty cycle. For a given dead time τ_d, a higher switching frequency will result in more of the switching cycle being allocated to the dead time. This causes a higher degree of distortion and an effective duty cycle that increasingly differs from the requested duty cycle. This effective duty cycle can be approximated with

$$T_{S1} = (D_{req}T_{sw}) - \tau_d, \tag{4a}$$
$$T_{S2} = ((1-D_{req})T_{sw}) - \tau_d, \tag{4b}$$
$$D_{eff} = T_{S1}/(T_{S1}+T_{S2}), \tag{4c}$$

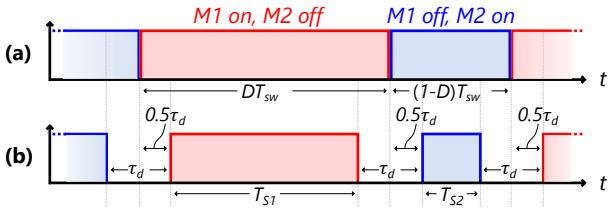

Fig. 9. Switching states and symmetric dead time used for the proposed duty cycle compensation scheme.

TABLE I
Inverter Design Specifications

Specification	Grid 1	Grid 2	Grid 3
Grid voltage ($V_{L-L,RMS}$)	208V	400V	480V
Grid current (A_{RMS})	36A	36A	36A
Grid frequency (Hz)	60Hz	50Hz	60Hz
DC link voltage (V)	450V	800V	930V
Rated Power (kVA)	13kVA	22kVA	22kVA
Peak Power (kVA)	13kVA	25kVA	30kVA

where T_{S1} is the *on* time of the upper switch, T_{S2} is the *on* time of the lower switch, D_{req} is the requested undistorted duty cycle, τ_d is the dead time, and D_{eff} is the effective distorted duty cycle that is ultimately actuated by the switches. These timings can be visualized in Fig. 9. Symmetric rise and fall dead time is assumed.

As the switching frequency is increased, the difference between D_{req} and D_{eff} also increases, and the duty cycle becomes further distorted. This can be visualized in Fig. 8, where both the dead time and switching frequencies are varied and the requested duty cycle D_{req} and effective duty cycle D_{eff} compared. It can be seen that both high frequencies and large dead times significantly distort the duty cycle.

Fig. 8 also shows that, despite the high distortion, it is possible to achieve the entire duty cycle range even at high frequencies with relatively large dead times. This means that it is possible to at least partially compensate for this distortion through a straightforward first order compensation scheme. As shown in [57], typical duty cycle compensation schemes have to consider the different operating regions of the converter e.g. hard-switching, soft-switching, partial hard and soft-switching, etc. The proposed inverter exclusively soft-switches and only one operating region needs to be considered, which simplifies the duty cycle compensation.

A duty cycle compensation scheme is proposed as

$$D_{req} = D_{calc} - k_d \frac{\tau_d}{T_{sw}}(D_{calc} - .5), \tag{5}$$

where D_{calc} is the duty cycle that is calculated by the controller and k_d is a user adjustable duty cycle compensation coefficient. The controller calculates the duty cycle D_{calc}, which is then used in (5) to calculate the requested duty cycle D_{req}. D_{req} is then sent to the PWM module to actuate the duty cycles.

Using the approximation of the effective duty cycle in (4a)-(4c), Fig. 10 shows the effect of the duty cycle compensation scheme on the difference between D_{req} and D_{eff}. It can be seen that tuning the value of k_d will result in an elimination of the duty cycle distortion. In reality, the equations of (4a)-(4c) are approximated, and keeping k_d as an adjustable constant is necessary for more precise duty cycle compensation. The efficacy of this duty cycle compensation scheme is shown in section VII.

VI. Design

The design requirements for the proposed inverter converter can be seen in Table I. There are three grid types that the inverter interfaces with. The maximum grid current, regardless of grid type, is $36A_{RMS}$ and this defines the peak power level for each grid voltage. The design maintains capability of 30kW but is optimized for 15kW operation when interfacing with grid Type 3 ($18A_{RMS}$ per phase) and can sustain extended operating time at this power level.

A. $\eta\rho$ Optimization

There are a multitude of converter parameters that need to be balanced during the design process. This is a challenge as many of these parameters have interdependencies and non-linear effects on both the overall efficiency (η) and power density (ρ) of the converter. In order to optimize for both η and ρ simultaneously, it is necessary to have models that describe how each of the design parameters effect loss and volume.

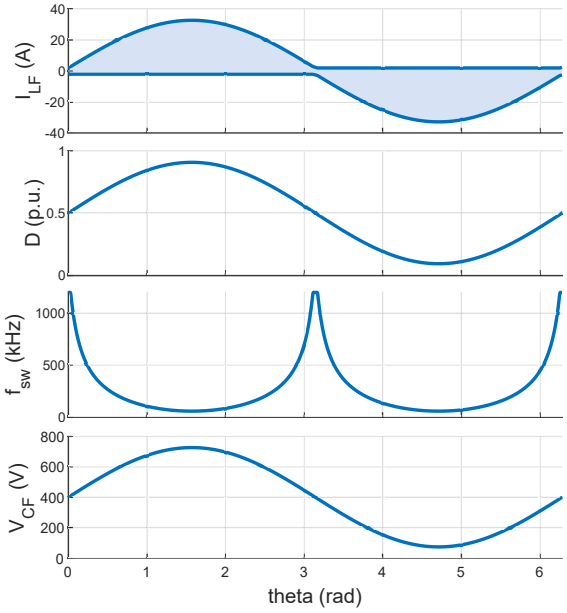

Fig. 11. From top to bottom: filter inductor L_F current envelope, duty cycle D, switching frequency f_{sw}, and capacitor voltage V_{CF} over one cycle of the grid for one phase of the converter.

1) Loss Calculations: In the context of circuit analysis and loss calculations it is convenient to view this converter topology as three separate half-bridge converters where each half-bridge converter services one phase. The loss of each phase can be calculated individually and its efficiency considered representative of the converter as a whole.

It is important to note that the output of each individual half-bridge converter is an AC waveform and therefore its operating point changes over one cycle of the grid. As the instantaneous loss over one cycle of the grid can change dramatically, it is therefore important to consider the range of operating points that the converter spans over the entire grid cycle when calculating loss.

This can be seen in Fig. 11, where the switching frequency f_{sw}, duty cycle D, filter capacitor C_f voltage, grid current I_g, and filter inductor L_f ripple current $I_{L,p-p}$ envelope are shown over one cycle of the grid for the rated power listed in Table I and a filter inductance value of $L_f = 17\mu$H while interfacing with grid Type 2.

Losses over one cycle of the grid can then be calculated in accordance with these varying operating points. Converter loss can be split into four components: FET conduction loss, FET switching loss, inductor winding loss, and inductor core loss. Capacitor losses are considered to be negligible. FET conduction loss can be calculated with

$$P_{cond}(\theta) = R_{on}\left(I_{out}(\theta)^2 + \left(\frac{1}{2\sqrt{3}} I_{L,p-p}(\theta)\right)^2\right), \tag{6}$$

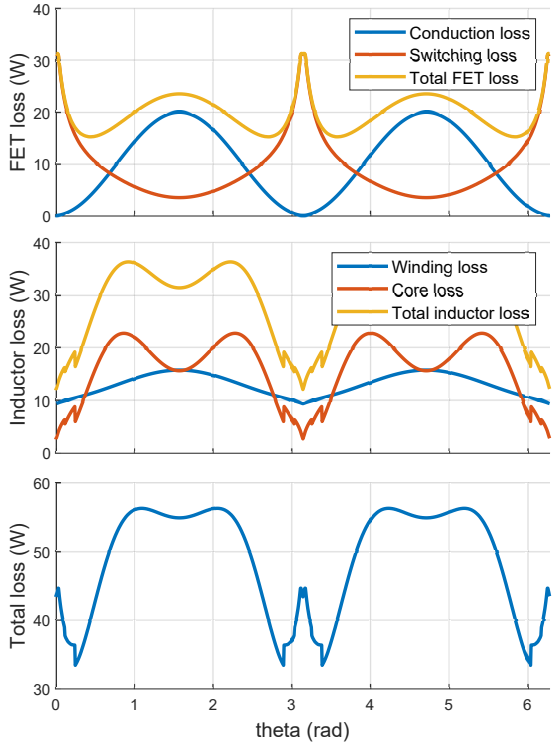

Fig. 12. FET loss and inductor loss mechanisms over one cycle of the grid.

where values that are functions of θ denote values that change over the cycle of the grid. FET switching loss can be found using

$$E_{sw}(\theta) = E_{off}(V_{bus}, I_a(\theta)) + E_{off}(V_{bus}, I_b(\theta)) \tag{7a}$$

$$I_a(\theta) = I_{DC} - \frac{I_{L,p-p}(\theta)}{2} \tag{7b}$$

$$I_b(\theta) = I_{DC} + \frac{I_{L,p-p}(\theta)}{2}, \tag{7c}$$

where $E_{off}(V_{ds}, I_d)$ is the turn-off switching energy as a function of FET drain-source voltage V_{ds} and current I_d. V_{ds} is equal to the DC link voltage and I_d is equal to the peak and valley of the inductor current ripple as described in (7b) and (7c). It is important to note that (7a) only applies to soft-switched inverters, hard-switched and partially hard/soft-switched inverters will have different equations for E_{sw}. $E_{off}(V_{ds}, I_d)$ can be found using double-pulse tests and a partial mapping of this can be seen in Fig. 4.

Inductor core loss is calculated using the Steinmetz equation

$$P_{core}(\theta) = k(\theta) f_{sw}(\theta)^{a(\theta)} B_{pk}(\theta)^{b(\theta)}, \tag{8a}$$

$$B_{pk} = \frac{L I_p(\theta)}{N A_c}, \tag{8b}$$

where $k(\theta)$, $a(\theta)$, and $b(\theta)$ are the frequency dependent steinmetz coefficients of the chosen material (3F36 [58]) which vary over the cycle of the grid. L is the value of the inductor, N is the number of turns of the inductor, A_c is the cross sectional area of the magnetic core of the inductor, and $B_{pk}(\theta)$ is the peak value of the flux density through that core.

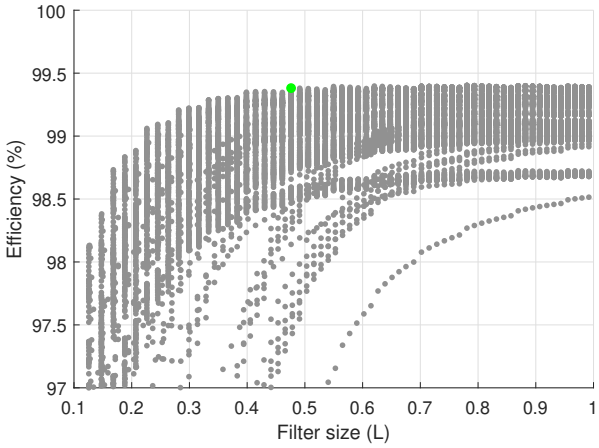

Fig. 13. Loss vs. volume Pareto Frontier with the chosen operating point highlighted in green.

Lastly, the winding loss P_{cu} of the inductor is calculated according to its frequency dependant resistance

$$P_{Cu}(\theta) = R_{DC} I_{out}(\theta)^2 + R_{PWM}(\theta) \left(\frac{1}{2\sqrt{3}} I_{L,p-p}(\theta) \right)^2. \tag{9}$$

It is assumed that there are exclusively two frequencies of current within the inductor, the grid frequency and the switching frequency, and that the winding resistance at the grid frequency and the winding resistance at DC are equal. The frequency dependant resistance of the winding is found using the techniques described in [59], [60] which take into account the skin effect and winding pattern of the Litz wire.

The four loss mechanisms over a cycle of the grid while interfacing with grid Type 2 at 15kW and with a filter inductor value of $L_f = 17\mu$H can be seen in Fig. 12. Over one cycle of the grid the loss varies significantly and no single point can be considered representative of the converter's performance as a whole. This is rectified by averaging the loss over the cycle of the grid according to

$$\begin{aligned} P_{Loss} &= \frac{1}{2\pi} \int_0^{2\pi} (P_{cond}(\theta) \\ &+ P_{sw}(\theta) + P_{core}(\theta) + P_{Cu}(\theta)) d\theta. \end{aligned} \tag{10}$$

This loss modeling approach is used in the following sections find the η of the $\eta\rho$ a Pareto Frontier upon which an optimal converter design is derived.

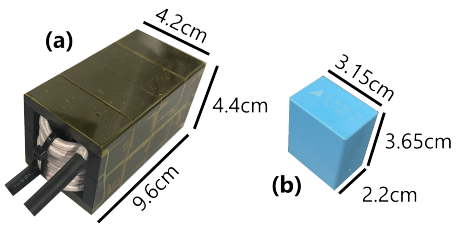

Fig. 14. Reference 50μH inductor and 12μF capacitor used for volume estimation.

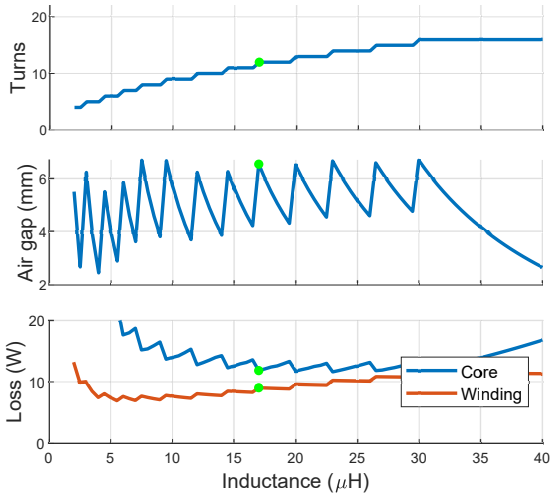

Fig. 15. Lowest loss inductor design parameters vs. specified inductance.

2) Volume Estimations: The last component required for the $\eta\rho$ optimization is the ρ. The sizing of the output filter can be estimated through its component values by using scaling laws [61]. Inductor volume scales with

$$\frac{Y_L}{Y_L^*} = \left(\frac{E_L}{E_L^*}\right)^{\frac{3}{4}} = \left(\frac{0.5LI^2}{0.5L^*I^2}\right)^{\frac{3}{4}} = \left(\frac{L}{L^*}\right)^{\frac{3}{4}}, \qquad (11)$$

where Y_L and E_L are inductor volume and energy, respectively. Capacitor volume scales in a similar manner according to

$$\frac{Y_C}{Y_C^*} = \left(\frac{E_C}{E_C^*}\right) = \left(\frac{0.5CV^2}{0.5C^*V^2}\right) = \left(\frac{C}{C^*}\right), \qquad (12)$$

where Y_C and E_C are capacitor volume and energy, respectively. The * superscript denotes values relating to a reference device using the same technology.

The reference capacitor and inductor can be seen in Fig. 14. The capacitor is a TDK B32774D8126 12μF film capacitor. The inductor is a 50μH airgapped inductor of 3F36 E42-21-20 ferrite core material and 2625/44 Litz wire. The resulting designed inverter uses as similar technology as possible to maintain accuracy between the experimental prototype and these volume estimations.

3) Pareto Frontier Generation: The application of practical components to the theory of the previous loss and volume estimation sections results in the generation of a Pareto frontier. The $\eta\rho$ Pareto frontier balances the following parameters:

- FET brand/model
- C_T capacitance value
- Filter inductance L_f
- Filter inductance turns N
- Filter inductance air gap L_g
- Filter inductance core quantity
- Upper switching frequency bound $f_{sw,u}$

under the constraint of using 3F36 E42-21-20 ferrite cores and 2625/44 Litz wire as these are used in the references for the volume estimation. The loss and volume for all allowable combinations of parameters is calculated. This gives a Pareto frontier of loss vs volume upon which a desirable operating parameters can be chosen. This Pareto can be seen in Fig. 13. However, just considering the final Pareto frontier obfuscates any potential trends with respect to parameter values.

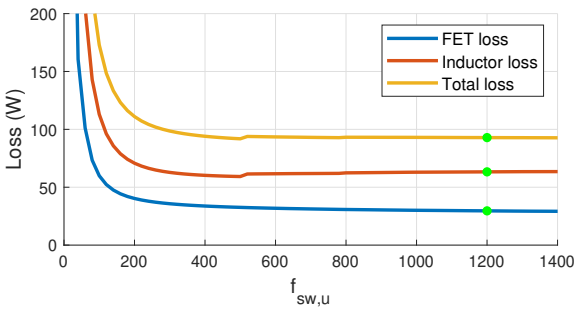

Fig. 16. Inductor and FET loss vs. upper switching frequency $f_{sw,u}$.

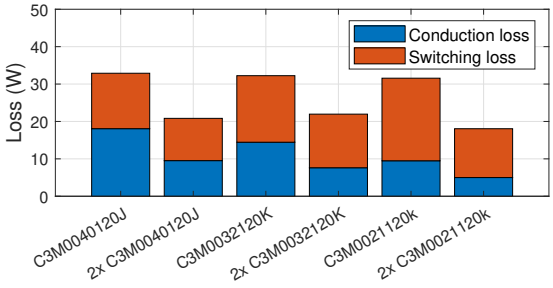

Fig. 17. Loss for different FET choices and configurations.

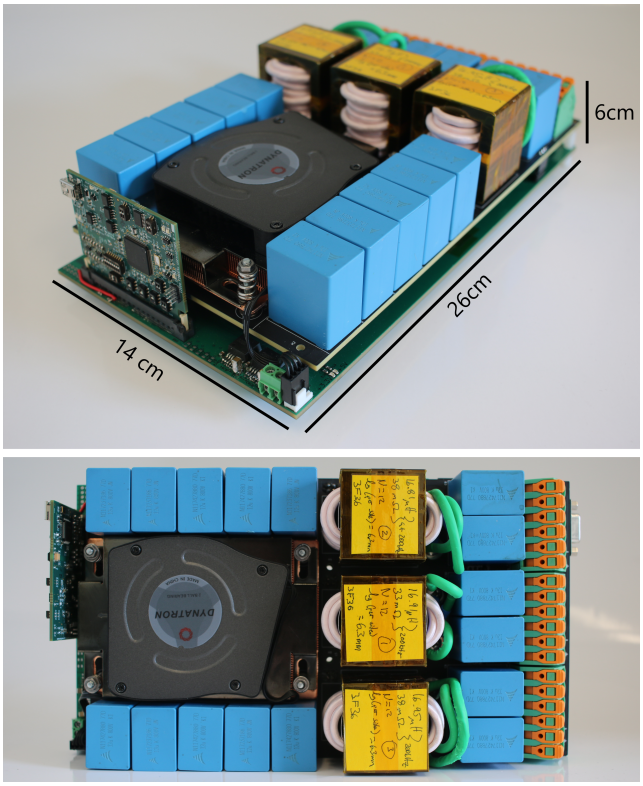

Fig. 18. Constructed experimental inverter prototype.

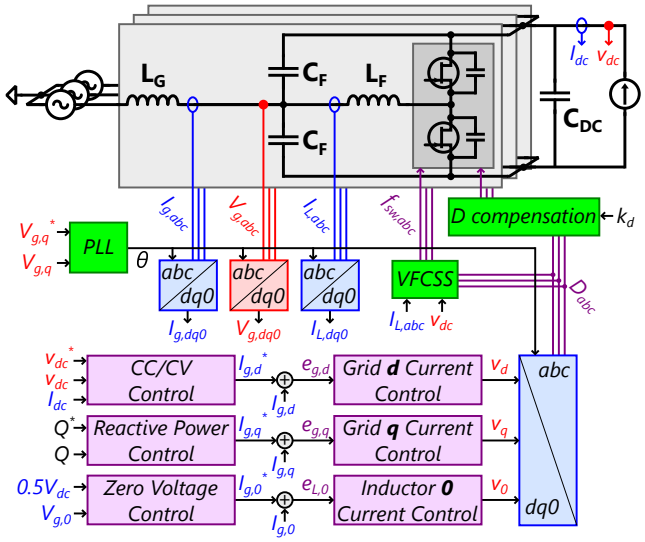

Fig. 19. High-level control topology of the proposed soft-switching inverter when used as the AC/DC stage of a 2-stage EV battery charger.

For the sake of trend observation the Pareto frontier can be broken up into intermediate components. One notable trend is the effect the upper bound of the switching frequency $f_{sw,u}$ has on the FET loss. Fig. 16 shows the calculated total loss as a function of the upper switching frequency bound when interfacing with a Type 3 grid at 15kW. This shows that, due to the variable frequency nature of this design, the upper switching frequency bound becomes largely irrelevant beyond a point. This is because the higher the upper bound, the proportionally smaller time the converter spends at that switching frequency. Ultimately, the limit of this value comes from the constructed hardware capabilities.

The optimal inductor design as a function of specified inductance is shown in Fig. 15. For Fig. 15, a static upper switching frequency value of 1.2MHz is chosen along with two parallel sets of EE E42/21/20 3F36 cores. For each specified inductance value, the number of turns and airgap that result in the lowest average loss over the cycle of the grid are stored and shown. The trend that can be seen here is that a certain airgap range is optimal and the number of turns is adjusted to keep the inductor in this optimal air gap range for a given specified inductance.

Lastly, the different FET choices/configuration and how they impact loss as a function of inductance can be seen in Fig. 17. SiC FET manufactures typically offer a family of FETs where within the family there is an internal tradeoff between switching loss and on resistance. Fig. 17 shows that for this application, the lower on resistance and higher switching loss FET variants are more favorable.

The final resulting $\eta\rho$ Pareto frontier of Fig. 13 shows that there are a range of suitable operating points with the chosen highlighted in green. This operating point denotes a filter inductor value of $L_F = 17\mu$H, upper switching frequency of $f_{sw,u} = 1.2$MHz, and an external drain-source capacitance value of $C_T = 220$pF, and two parallel C3M0032120k FETs for each switching device. It is optimized for 15kW operation while maintaining capability up to 30kW.

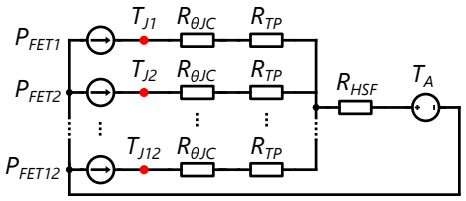

Fig. 20. Steady-state thermal circuit of the proposed inverter.

B. Control

A brief discussion on the control design of the converter is included in this section as the control design is not the highlight of this paper. More information on the control of this converter can be found in [46]. The control diagram of the inverter is shown in Fig. 19. A phase-locked loop (PLL) is configured to convert the voltage and current values among abc and dq reference frames. The active and reactive power are controlled in d and q reference frames, respectively.

The constant current (CC) and constant voltage (CV) controllers are cascaded with the d and q components of grid current to adjust the active/reactive power between the DC link and the grid. Shown in fig. 19 is the control scheme with the inverter operating as the AC/DC grid interface of a two-stage battery charger. In this configuration, the DC/DC interface sets the DC-link current and the AC/DC grid interface adjusts the d component current to a desired DC-link voltage. For applications where the DC-link voltage is controlled externally, the d and q components of the grid current can be set with individual active and reactive power controllers, respectively.

The zero-sequence controller is leveraged to step up the output capacitor voltage with an offset of $0.5V_{dc}$. The frequency of each phase is controlled individually with a feedforward term, which is calculated according to (3) with a predetermined and static $I_{L,min}$ value. Lastly, the duty cycle is compensated with an additional feedforward term according to (5), again with a static and predetermined k_d value.

C. Experimental Prototype

The experimental prototype constructed given the operating parameters found in section VI-A can be seen in Fig. 18. The prototype has a volume of 2.19L which is calculated considering the smallest rectangular bounding box that will encompass the proposed soft-switched inverter. The mass is 2.95kg. Both the mass and volume include all magnetic components. The resulting power density is 13.7kW/L and 10.16kW/kg. A Texas Instruments microcontroller TMDSC-NCD280049C control card is used to execute the control, calculate the duty cycles and switching frequencies of each phase, actuate the gate signals, and read the sensor values. The control period is 40μs (20kHz). NCV57000 gate driver ICs are used to drive the pair of C30032120k FETs at switching frequencies up to 1.2MHz. The filter capacitor C_F and DC link capacitances have values of 24μF and 240μF, respectively. The grid-side inductance L_G is a 2μH surface-mount component placed on the PCB.

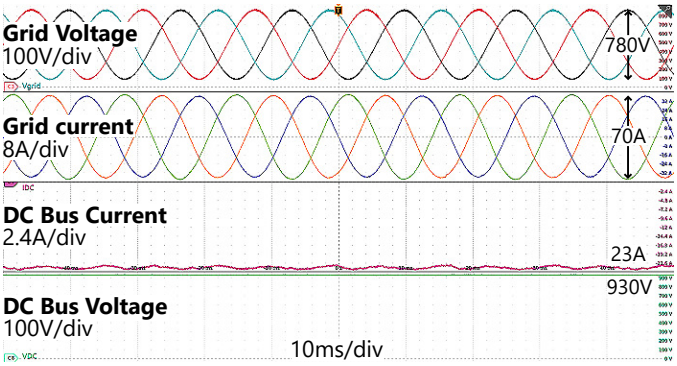

Fig. 21. 3-phase grid voltage and current waveforms.

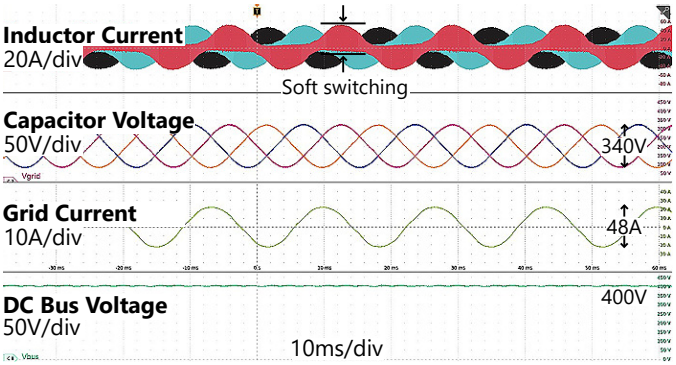

Fig. 22. VFCSS waveforms.

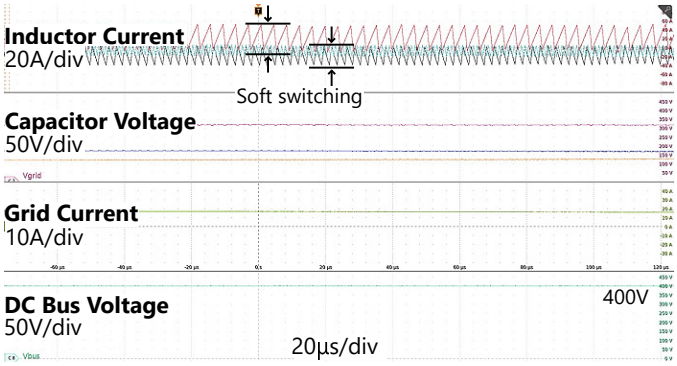

Fig. 23. Zoomed-in VFCSS waveforms.

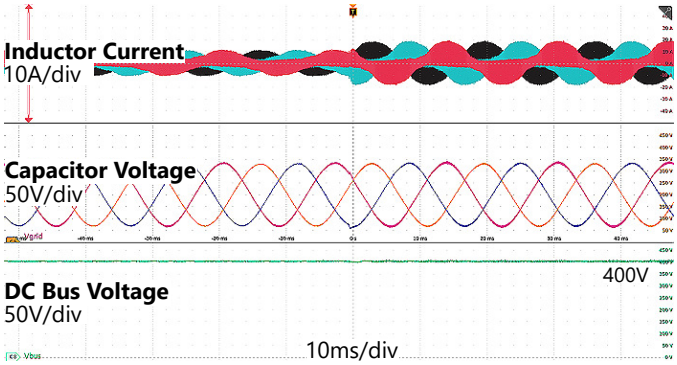

Fig. 24. Inductor current, grid voltage, and DC link voltage during 4A load step.

The DC link voltage when interfacing with the Type 3 grid is 930V and the chosen FETs are 1200V devices. This leaves little margin for FET drain-source overshoot before the device is damaged. This is not optimal for reliability, however, the proposed converter exclusively soft-switches and therefore there is minimal FET drain-source overshoot and tolerable reliability is maintained.

Lastly, a single Dynatron A31 CPU server heatsink with a thermal resistance R_{HSF} of 0.247°C/W is used to cool all 12 FETs [62]. 1mm thick Fujipoly XR-m thermal pads with an approximate mounting pressure of 50PSI interface the FETs and the heatsink. The resistance of each thermal pad R_{TP} is approximately 0.4°C/W [63]. The thermal resistance of the junction to case of the FET $R_{\theta JC}$ is 0.45°C/W. The resulting steady-state thermal circuit can be seen in Fig. 20. For an ambient temperature T_A of 40°C and a junction temperature T_J of 125°C, the total tolerable loss that can be dissipated by the heatsink is 267W or approximately 20W per FET. The operating loss in the FETs is within this limit, as described in Section VII-D.

VII. Results

Testing results are shown in this section. A grid emulator is used to create the 3-phase source with its source inductance set to 0. A DC power supply in constant voltage mode powers the DC link. Both AC and DC sources are bidirectional. Basic 3-phase voltage and current values can be seen in Fig. 21 where clean waveforms can be observed. Soft-switching waveforms are shown Figs. 22 and 23 where the envelope of the inductor current shows that soft-switching is controlled through the switching frequency.

A. Transient Steps

A 4A load step is performed in Fig. 24. Fluctuations in both the DC link voltage and capacitor voltage are minimal during this transient. Furthermore, during this load transient, it can be seen that soft-switching is maintained.

B. Duty cycle compensation

Duty cycle compensation results can be seen in Fig. 25. The THD for Fig. 25-(a), 25-(b), and 25-(c) are 14.57%, 8.388%, and 2.427%, respectively. This shows that the duty cycle distortion caused by the combination of high frequency and large dead times, inherent to soft-switching converters

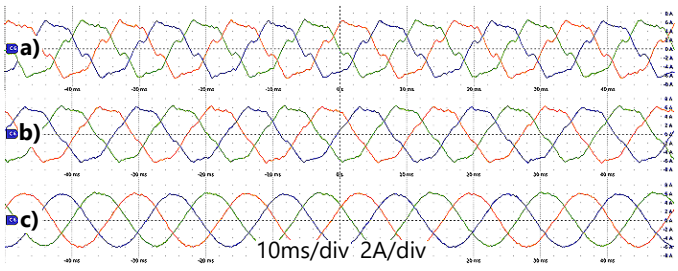

Fig. 25. Grid current waveforms for different degrees of duty cycle compensation. (a): $k_d = 0$. (b): $k_d = 0.1$. (c): $k_d = 0.25$.

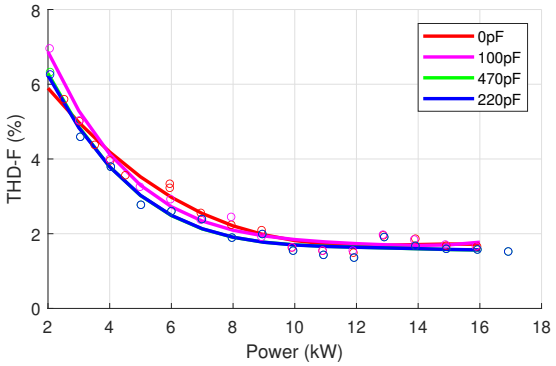

Fig. 26. Grid current THD-F for $800V_{DC}$ bus and $400V_{AC}$ grid for a range of C_T values.

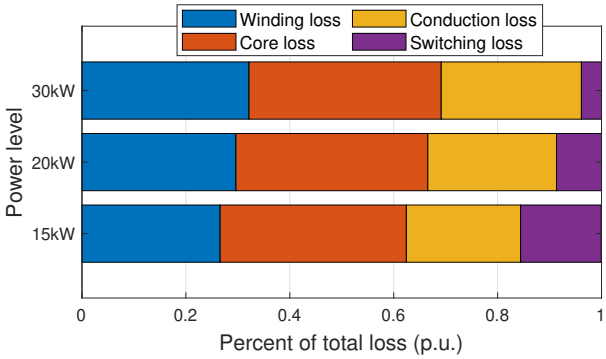

Fig. 28. Loss breakdown of the proposed inverter when interfacing with a Type 3 grid for three different power levels.

of the proposed technologies, can be compensated for with the straightforward open-loop compensation scheme shown in section V.

C. Total Harmonic Distortion

The THD-F of the output grid current can be seen in Fig. 26. As the power increases the THD-F levels off at around 2%. Experiments with four values of additional C_T capacitance values are included to show that they do not significantly effect the grid current THD.

D. Thermals and Loss

Fig. 28 shows the loss breakdown of the proposed inverter operating over a range of output powers when interfacing with Type 3 grid. The loss mechanisms maintain mostly the same ratio over the range of power levels except for the switching loss, which constitutes a smaller proportion of the total loss as the power level increases. This is a result of the VFCSS scheme, as the output current increases, the switching frequency range decreases, and the switching loss takes up a proportionally smaller amount of the total loss despite the increase in switching energy per cycle.

Fig. 27 shows the inductor temperature when operating at 20kW while interfacing with a Type 3 grid after the temperature has stabilized (approximately 20 minutes). The ambient temperature is 21°C. The windings closet to the air gap are the hottest parts of the transformer, suggesting that fringing flux around the air gap drives loss in the winding. At this operating point the total FET loss is approximately 30W, which results an approximate junction temperature of 35°C when using the values given in Section VI-C.

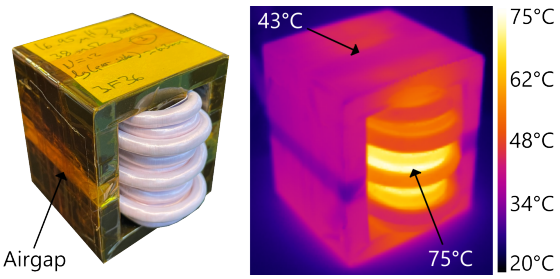

Fig. 27. Inductor temperature when operating at 20kW with Type 2 grid.

E. Inductor L_F Current Frequency Spectrum

Fig. 29 shows the frequency spectrum of the current through inductor L_F for two different power levels while interfacing with a Type 3 grid connection with a DC link voltage of 930V.

It can be seen that the 10kW spectrum has more, higher frequency components than the 20kW spectrum. This is because higher power operation, for a given grid interface, has higher peaks and lower valleys of grid current compared to those of lower power operations. The higher peaks and lower valleys require a higher inductor current ripple to maintain soft-switching according to the VFCSS scheme. Higher current ripple is implemented by reducing the switching frequency according to (3).

This shifting in frequency can be visualized in the current spectrum of inductor L_F which shows that higher powers have stronger lower frequency components and vice versa.

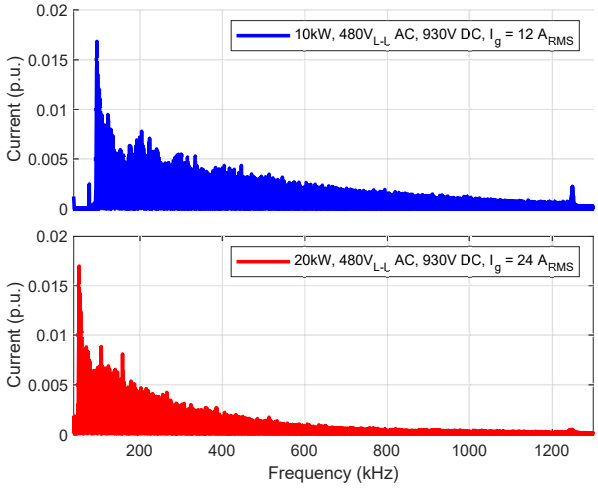

Fig. 29. Frequency spectrum of the current through filter inductor L_F for two different power levels when interfacing with Type 3 grid connection. The spectrum is normalized to the fundamental (60Hz) component of the inductor current.

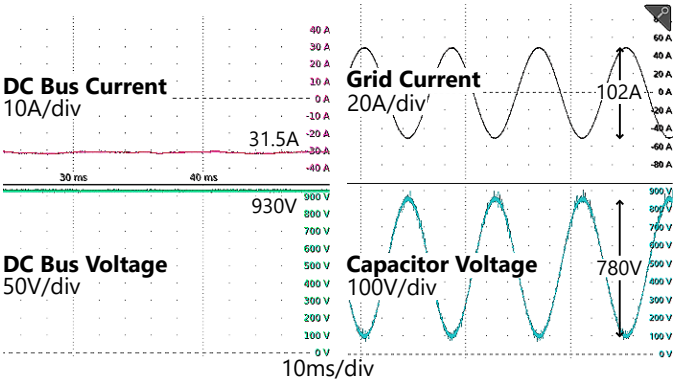

Fig. 30. Grid voltage, grid current, DC link voltage, and DC link current during 30kW operation.

F. Maximum Power

Fig. 30 shows a single phase of the converter operating at the peak power of 30kW. Clean signals can be noted on the current and voltage waveforms for both the AC and DC sides of the inverter.

G. Efficiency

Efficiency is measured experimentally using a Tektronix MSO58 8-channel oscilloscope power analyzer, where three channels are used for the grid current, three channels for the grid voltage, one channel for the DC link voltage, and one channel for the DC link current. Tektronix P5200A voltage probes and TCP0030A current probes are used. Multiple measurements are taken at each data point at both positive and negative power flows and subsequently averaged to compensate for measurement noise. The loss incurred on the low voltage supply rails is recorded separately and subtracted from the output power of the converter. It is worth noting that this loss is insignificant relative to the loss of the power electronics components.

The efficiency curves can be seen in Figs. 31 and 32. The calculated efficiency closely matches but slightly overestimates the measured efficiencies. This can be attributed to the loss

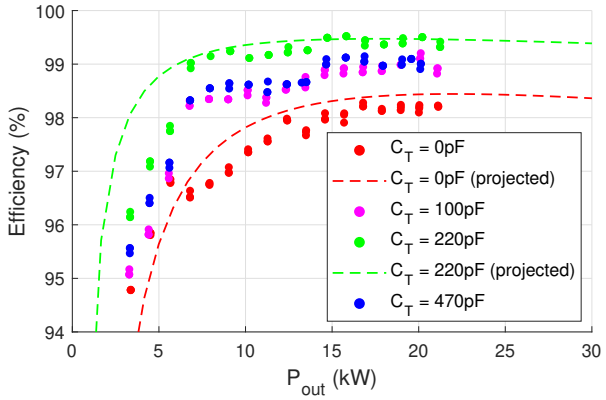

Fig. 31. Measured and projected efficiency of the proposed soft-switched inverter operating at maximum design voltage of $V_{DC} = 930V$ and $V_{grid} = 480V_{l-l}$.

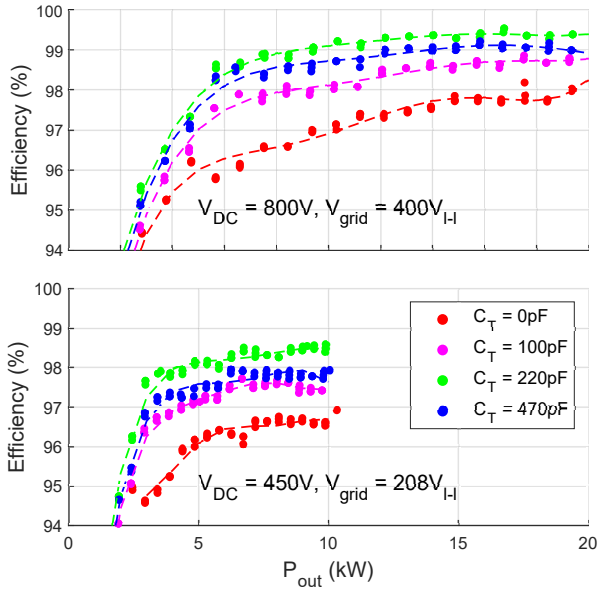

Fig. 32. Measured efficiency of the proposed soft-switched inverter when interfacing with $400V_{l-l}$ and $208V_{l-l}$ grids.

within the grid-side inductor L_g which is not included in the loss calculations of section VI and fringing flux loss within the windings as a relatively large air gap is used. Efficiency curves are relatively flat beyond 6kW, denoting the effectiveness of the variable frequency scheme to maintain soft-switching.

Four different values of C_T are used to demonstrate the effectiveness of the additional capacitance on reducing the switching loss. This also shows that excessive sizing of this capacitor will reduce the efficiency due to the increased dead time and $I_{L,min}$ values that they necessitate. Peak efficiency for all grid configurations is reached with a C_T value of 220pF. The maximum measured efficiency of $\geq$99.5% occurs with a $480V_{l-l}$ grid and $930V_{dc}$ bus.

VIII. Conclusion

This work shows the design and experimental realization of a soft-switched grid-tied inverter with high efficiency ($\geq$99.5%), high power density (13.7kw/L and 10.17kW/kg), and high switching frequency (1.2MHz). This is achieved through the groupings of three technologies. First is the VFCSS scheme that allows for soft-switching and the exchange of turn-on losses for turn-off losses over all operating points of the inverter. Second is the additional drain-source capacitance placed on each FET which slows down the switching transient and allows for a $\geq$40% reduction in turn-off losses and increased leverage of the VFCSS scheme. Lastly is the open-loop duty-cycle compensation scheme, which effectively mitigates the distortion caused by the high switching frequency and slow switching transients. The end result is an inverter that improves upon the state-of-the art with respect to efficiency and power density.

Acknowledgments

This research is based in part upon work supported by the National Science Foundation under Grant Number 1653574.

REFERENCES

[1] Samira Hosseini and Abdulsalam Yassine. A novel v2v charging scheme to optimize cost and alleviate range anxiety. In *2022 IEEE Electrical Power and Energy Conference (EPEC)*, pages 354–359, 2022.

[2] Matthew Jahnes, Liwei Zhou, Michael Eull, Weizhong Wang, and Matthias Preindl. Design of a 22-kw transformerless ev charger with v2g capabilities and peak 99.5% efficiency. *IEEE Transactions on Industrial Electronics*, 70(6):5862–5871, 2023.

[3] Zhengyang Liu, Bin Li, Fred C. Lee, and Qiang Li. High-efficiency high-density critical mode rectifier/inverter for wbg-device-based on-board charger. *IEEE Transactions on Industrial Electronics*, 64(11):9114–9123, 2017.

[4] Dong-Hee Kim, Min-Jung Kim, and Byoung-Kuk Lee. An integrated battery charger with high power density and efficiency for electric vehicles. *IEEE Transactions on Power Electronics*, 32(6):4553–4565, 2017.

[5] Berker Bilgin, Pierre Magne, Pawel Malysz, Yinye Yang, Vera Pantelic, Matthias Preindl, Alexandre Korobkine, Weisheng Jiang, Mark Lawford, and Ali Emadi. Making the case for electrified transportation. *IEEE Transactions on Transportation Electrification*, 1(1):4–17, 2015.

[6] Michael Eull, Liwei Zhou, Matthew Jahnes, and Matthias Preindl. Bidirectional nonisolated fast charger integrated in the electric vehicle traction drivetrain. *IEEE Transactions on Transportation Electrification*, 8(1):180–195, 2022.

[7] Ashkan Barzkar and Mona Ghassemi. Electric power systems in more and all electric aircraft: A review. *IEEE Access*, 8:169314–169332, 2020.

[8] Bulent Sarlioglu and Casey T. Morris. More electric aircraft: Review, challenges, and opportunities for commercial transport aircraft. *IEEE Transactions on Transportation Electrification*, 1(1):54–64, 2015.

[9] Arber Haxhiu, Ahmed Abdelhakim, Sami Kanerva, and Jostein Bogen. Electric power integration schemes of the hybrid fuel cells and batteries-fed marine vessels—an overview. *IEEE Transactions on Transportation Electrification*, 8(2):1885–1905, 2022.

[10] Espen Skjong, Rune Volden, Egil Rødskar, Marta Molinas, Tor Arne Johansen, and Joseph Cunningham. Past, present, and future challenges of the marine vessel's electrical power system. *IEEE Transactions on Transportation Electrification*, 2(4):522–537, 2016.

[11] Jingang Yi, Jingliang Li, Jianbo Lu, and Zhaodu Liu. On the stability and agility of aggressive vehicle maneuvers: A pendulum-turn maneuver example. *IEEE Transactions on Control Systems Technology*, 20(3):663–676, 2012.

[12] H. Mazumder, M. Ektesabi, and A. Kapoor. Effect of mass distribution on cornering dynamics of retrofitted ev. In *2012 IEEE International Electric Vehicle Conference*, pages 1–6, 2012.

[13] J. W. Kolar, J. Biela, S. Waffler, T. Friedli, and U. Badstuebner. Performance trends and limitations of power electronic systems. In *2010 6th International Conference on Integrated Power Electronics Systems*, pages 1–20, 2010.

[14] Dominik Neumayr, Dominik Bortis, and Johann Walter Kolar. The essence of the little box challenge-part a: Key design challenges & solutions. *CPSS Transactions on Power Electronics and Applications*, 5(2):158–179, 2020.

[15] Yanjun Shi, Lu Wang, Ren Xie, and Hui Li. Design and implementation of a 100 kw sic filter-less pv inverter with 5 kw/kg power density and 99.2% cec efficiency. In *2018 IEEE Applied Power Electronics Conference and Exposition (APEC)*, pages 393–398, 2018.

[16] Madhu Chinthavali, Zhiqiang Jack Wang, Steven Campbell, Tong Wu, and Burak Ozpineci. 50-kw 1kv dc bus air-cooled inverter with 1.7 kv sic mosfets and 3d-printed novel power module packaging structure for grid applications. In *2018 IEEE Applied Power Electronics Conference and Exposition (APEC)*, pages 133–140, 2018.

[17] Jon Azurza Anderson, Eli J. Hanak, Lukas Schrittwieser, Mattia Guacci, Johann W. Kolar, and Gerald Deboy. All-silicon 99.35% efficient three-phase seven-level hybrid neutral point clamped/flying capacitor inverter. *CPSS Transactions on Power Electronics and Applications*, 4(1):50–61, 2019.

[18] Ning He, Min Chen, Junxiong Wu, Nan Zhu, and Dehong Xu. 20-kw zero-voltage-switching sic-mosfet grid inverter with 300 khz switching frequency. *IEEE Transactions on Power Electronics*, 34(6):5175–5190, 2019.

[19] Jianliang Chen, Deshang Sha, Jiankun Zhang, and Xiaozhong Liao. An sic mosfet based three-phase zvs inverter employing variable switching frequency space vector pwm control. *IEEE Transactions on Power Electronics*, 34(7):6320–6331, 2019.

[20] Qingyun Huang, Alex Q. Huang, Ruiyang Yu, Pengkun Liu, and Wensong Yu. High-efficiency and high-density single-phase dual-mode cascaded buck–boost multilevel transformerless pv inverter with gan ac switches. *IEEE Transactions on Power Electronics*, 34(8):7474–7488, 2019.

[21] Hongwu Peng, Zhao Yuan, Dereje Lemma Woldegiorgis, Asif Imran Emon, Balaji Narayanasamy, Yusi Liu, Fang Luo, Alan Mantooth, and Haider Ghazi Mhiesan. Practical design and evaluation of a high-efficiency 30-kva grid-connected pv inverter with hybrid switch structure. In *2020 IEEE Energy Conversion Congress and Exposition (ECCE)*, pages 3670–3676, 2020.

[22] Hongyi Lin, Ziming Wang, Xiao Guo, Zhongyin Lin, and Guozhu Chen. A 380 v/50 kvar sic-svg achieving a power density of 1.652 kvar/l with the optimization of heatsink and output filter volume. *IEEE Journal of Emerging and Selected Topics in Power Electronics*, 10(4):4634–4649, 2022.

[23] Lanhua Zhang, Rachael Born, Xiaonan Zhao, and Jih-Sheng Lai. A high efficiency inverter design for google little box challenge. In *2015 IEEE 3rd Workshop on Wide Bandgap Power Devices and Applications (WiPDA)*, pages 319–322, 2015.

[24] Rajesh Ghosh, Miao-xin Wang, Srikanth Mudiyula, Uday Mhaskar, Radoslava Mitova, David Reilly, and Damir Klikic. Industrial approach to design a 2-kva inverter for google little box challenge. *IEEE Transactions on Industrial Electronics*, 65(7):5539–5549, 2018.

[25] Chongwen Zhao, Bradford Trento, Ling Jiang, Edward A. Jones, Bo Liu, Zheyu Zhang, Daniel Costinett, Fei Fred Wang, Leon M. Tolbert, John F. Jansen, Reid Kress, and Rick Langley. Design and implementation of a gan-based, 100-khz, 102-w/in3 single-phase inverter. *IEEE Journal of Emerging and Selected Topics in Power Electronics*, 4(3):824–840, 2016.

[26] Akanksha Singh, Madhu Chinthavali, Scott Sudhoff, Kevin Bennion, Kumaraguru Prabakar, Xuhui Feng, Zhiqiang Wang, and Steven Campbell. Development and validation of a sic based 50 kw grid-connected pv inverter. In *2018 IEEE Energy Conversion Congress and Exposition (ECCE)*, pages 6165–6172, 2018.

[27] Yanjun Shi, Lu Wang, Ren Xie, Yuxiang Shi, and Hui Li. A 60-kw 3-kw/kg five-level t-type sic pv inverter with 99.2% peak efficiency. *IEEE Transactions on Industrial Electronics*, 64(11):9144–9154, 2017.

[28] Yanjun Shi, Lu Wang, Ren Xie, and Hui Li. Design and implementation of a 100 kw sic filter-less pv inverter with 5 kw/kg power density and 99.2% cec efficiency. In *2018 IEEE Applied Power Electronics Conference and Exposition (APEC)*, pages 393–398, 2018.

[29] Roman Bosshard and Johann W. Kolar. All-sic 9.5 kw/dm3 on-board power electronics for 50 kw/85 khz automotive ipt system. *IEEE Journal of Emerging and Selected Topics in Power Electronics*, 5(1):419–431, 2017.

[30] Gibong Son and Qiang Li. Control techniques for crm-based high-frequency soft-switching three-phase inverter under unbalanced grid conditions. *IEEE Transactions on Power Electronics*, 37(6):6613–6624, 2022.

[31] Bret Whitaker, Adam Barkley, Zach Cole, Brandon Passmore, Ty McNutt, and Alexander B. Lostetter. High-frequency ac-dc conversion with a silicon carbide power module to achieve high-efficiency and greatly improved power density. In *2013 4th IEEE International Symposium on Power Electronics for Distributed Generation Systems (PEDG)*, pages 1–5, 2013.

[32] Y. Li, Y. Zhang, X. Yuan, L. Zhang, Z. Song, M. Wu, F. Ye, Z. Li, Y. Li, Y. Xu, and Z. Wang. 500 kw forced air-cooled silicon carbide (sic) three-phase dc/ac converter with a power density of 1.246 mw/m3 and efficiency $>$98.5%. *IEEE Transactions on Industry Applications*, 57(5):5013–5027, 2021.

[33] Daifei Zhang, Danqing Cao, Jonas Huber, Jordi Everts, and Johann W. Kolar. Non-isolated three-phase current dc-link buck-boost ev charger with virtual output midpoint grounding and ground current control. *IEEE Transactions on Transportation Electrification*, pages 1–1, 2023.

[34] Rajesh Ghosh, Miao-xin Wang, Srikanth Mudiyula, Uday Mhaskar, Radoslava Mitova, David Reilly, and Damir Klikic. Industrial approach to design a 2-kva inverter for google little box challenge. *IEEE Transactions on Industrial Electronics*, 65(7):5539–5549, 2018.

[35] Li Lei, Ning Puqi, Tai Xiang, Wen Xuhui, and Zhang Dong. A genetic algorithm high power density converter system packing method. In *2017 19th European Conference on Power Electronics and Applications (EPE'17 ECCE Europe)*, pages P.1–P.10, 2017.

[36] Bret Whitaker, Zach Cole, Brandon Passmore, Daniel Martin, Ty McNutt, Alex Lostetter, M. Nance Ericson, S. Shane Frank, Charles L. Britton, Laura D. Marlino, Alan Mantooth, Matt Francis, Ranjan Lamichhane, Paul Shepherd, and Michael Glover. High-temperature

sic power module with integrated sic gate drivers for future high-density power electronics applications. In *2014 IEEE Workshop on Wide Bandgap Power Devices and Applications*, pages 36–40, 2014.

[37] Tong Wu, Zhiqiang Wang, Burak Ozpineci, Madhu Chinthavali, and Steven Campbell. Automated heatsink optimization for air-cooled power semiconductor modules. *IEEE Transactions on Power Electronics*, 34(6):5027–5031, 2019.

[38] Matthew Jahnes, Michael Owen, W. Wesley Pennington, and Matthias Preindl. Direct contact jet impingement cooling with non-conductive fluid for power converters that enables increased power density. In *2022 IEEE Transportation Electrification Conference & Expo (ITEC)*, pages 807–812, 2022.

[39] Zhiqiang Wang, Madhu Chinthavali, Steven L. Campbell, Tong Wu, and Burak Ozpineci. A 50-kw air-cooled sic inverter with 3-d printing enabled power module packaging structure and genetic algorithm optimized heatsinks. *IEEE Transactions on Industry Applications*, 55(6):6256–6265, 2019.

[40] Sadeq Ali Qasem Mohammed and Jin-Woo Jung. A state-of-the-art review on soft-switching techniques for dc–dc, dc–ac, ac–dc, and ac–ac power converters. *IEEE Transactions on Industrial Informatics*, 17(10):6569–6582, 2021.

[41] Yenan Chen and Dehong Xu. Review of soft-switching topologies for single-phase photovoltaic inverters. *IEEE Transactions on Power Electronics*, 37(2):1926–1944, 2022.

[42] Rayna Alizadeh and H. Alan Mantooth. A review of architectural design and system compatibility of power modules and their impacts on power electronics systems. *IEEE Transactions on Power Electronics*, 36(10):11631–11646, 2021.

[43] B.J. Baliga. Trends in power semiconductor devices. *IEEE Transactions on Electron Devices*, 43(10):1717–1731, 1996.

[44] C.P. Henze, H.C. Martin, and D.W. Parsley. Zero-voltage switching in high frequency power converters using pulse width modulation. In *APEC '88 Third Annual IEEE Applied Power Electronics Conference and Exposition*, pages 33–40, 1988.

[45] R. Watson, F.C. Lee, and G.C. Hua. Utilization of an active-clamp circuit to achieve soft switching in flyback converters. *IEEE Transactions on Power Electronics*, 11(1):162–169, 1996.

[46] Liwei Zhou, Matthew Jahnes, and Matthias Preindl. Modular model predictive control of a 15-kw, kilo-to-mega-hertz variable-frequency critical-soft-switching nonisolated grid-tied inverter with high efficiency. *IEEE Transactions on Power Electronics*, 37(10):12591–12605, 2022.

[47] Dominik Bortis, Dominik Neumayr, and Johann W. Kolar. $\eta\rho$-pareto optimization and comparative evaluation of inverter concepts considered for the google little box challenge. In *2016 IEEE 17th Workshop on Control and Modeling for Power Electronics (COMPEL)*, pages 1–5, 2016.

[48] Oleksandr Husev, Dmitri Vinnikov, Carlos Roncero-Clemente, Andrii Chub, and Enrique Romero-Cadaval. Single-phase string solar qzs-based inverter: Example of multi-objective optimization design. *IEEE Transactions on Industry Applications*, 57(3):3120–3130, 2021.

[49] Qingyuan Gao, Xu Yang, Gaohao Wei, Kangping Wang, and Qiaoliang Chen. Three degree-of-freedom optimization of high efficiency high power density llc converter. In *2022 IEEE International Power Electronics and Application Conference and Exposition (PEAC)*, pages 474–478, 2022.

[50] C. Marxgut, J. Biela, and J. W. Kolar. Interleaved triangular current mode (tcm) resonant transition, single phase pfc rectifier with high efficiency and high power density. In *The 2010 International Power Electronics Conference - ECCE ASIA -*, pages 1725–1732, 2010.

[51] Bharat Agrawal, Matthias Preindl, and Ali Emadi. Turn-off energy minimization for soft-switching power converters with wide bandgap devices. In *2017 IEEE International Conference on Industrial Technology (ICIT)*, pages 236–241, 2017.

[52] Ioan Serban. Power decoupling method for single-phase h-bridge inverters with no additional power electronics. *IEEE Transactions on Industrial Electronics*, 62(8):4805–4813, 2015.

[53] Michael Eull and Matthias Preindl. A soft switching inverter minimizing bearing currents in 800v electric vehicle drives. In *2021 IEEE 13th International Symposium on Diagnostics for Electrical Machines, Power Electronics and Drives (SDEMPED)*, volume 1, pages 457–463, 2021.

[54] Liwei Zhou, Michael Eull, Weizhong Wang, and Matthias Preindl. Modular model-predictive control with regulated third-harmonic injection for zero-sequence stabilized inverter. *IEEE Transactions on Industry Applications*, 58(6):7634–7647, 2022.

[55] Yi Tang, Wenli Yao, Poh Chiang Loh, and Frede Blaabjerg. Highly reliable transformerless photovoltaic inverters with leakage current and pulsating power elimination. *IEEE Transactions on Industrial Electronics*, 63(2):1016–1026, 2016.

[56] Matthew Jahnes and Matthias Preindl. Novel upper capacitor for half-bridge switching converter topologies that reduces emi and capacitor ripple current. In *2022 IEEE Transportation Electrification Conference & Expo (ITEC)*, pages 37–42, 2022.

[57] Chengmin Li, Yunjie Gu, Wuhua Li, Xiangning He, Zuyi Dong, Guodong Chen, Chengbin Ma, and Luhua Zhang. Analysis and compensation of dead-time effect considering parasitic capacitance and ripple current. In *2015 IEEE Applied Power Electronics Conference and Exposition (APEC)*, pages 1501–1506, 2015.

[58] Ferroxcube. *3F36, Improved performance at low temperature*, 2022.

[59] New England Wire Technologies. *PRODUCT SELECTION GUIDE*, 2022.

[60] William I. Orr. *Radio Handbook*. Newnes, 1997.

[61] Michael Eull and Matthias Preindl. Bidirectional three-level dc-dc converters: Sum-difference modeling and control. In *2017 IEEE Transportation Electrification Conference and Expo (ITEC)*, pages 573–578, 2017.

[62] Dynatron. *A41*, 2021.

[63] Fujipoly. *SARCON XR-m*, 2009.