Non-Dissipative Battery Cell Balancing Using Half-Bridge Switching Circuit

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***Abstract*—Cells in an electric vehicle battery pack tend to become out of balance after several charging and discharging cycles, resulting in capacity under-utilization and over-sizing of battery packs to achieve extended driving range. This makes it necessary to have a cell balancing mechanism onboard of the battery management system. This paper introduces a half-bridge DC/DC switching circuit for the balancing of lithium-ion cells, and highlights its advantages over existing cell balancing techniques. Furthermore, details on planar transformer design, control feedback, simulation results in MATLAB/Simulink, and experimental observations are included, showing greater controllability and improvement in efficiency in comparison with existing systems.**

***Index Terms*—Electric vehicles, half-bridge converter, high efficiency, individual cell current control, redistributive cell balancing.**

I. Introduction

Cells in a battery pack are not identical, and may vary in their state-of-charge (SOC), self-discharge rate, capacity, internal impedance, and temperature characteristics after many charging and discharging cycles. These variations may occur due to manufacturing differences, columbic efficiency, and capacity, which limits the charging and discharging ability of battery packs [1, 2]. Since the weakest cell defines the operating condition of the entire pack, the battery management system (BMS) may limit charging in case one of the cells in a series-connected system reaches its over-voltage or under-voltage cut-off limit [3]. This results in a lower effective battery pack capacity, forcing manufacturers to over-size battery packs, and effects related costs and warranty issues. Exceeding cut-off limits may result in temperature and pressure build-up, which might cause severe battery damage or cell explosion. A cell balancing system serves to extend battery run time as well as remaining useful life for a system utilizing multiple such cells in series. In order to maximize the use of a battery pack, one must provide a method of balancing the amount of charge in each cell using a closed loop controller, similar to one shown in [4].

Cell balancing aims at equalizing cell voltages or SOC amongst cells in a series-connected system, and is mainly categorized into two types dissipative and non-dissipative (or redistributive). The simplest of the methods, dissipative cell balancing, also known as resistor bleeding balancing, is highly inefficient, as it selectively shunts the charging current and dissipates the energy in resistors for high-voltage cells to reach equilibrium with the lowest cell voltage [5]. Since the dissipated energy is converted into additional losses in the resistors, such dissipative equalization approaches are suited to low power applications and low charge/discharge currents as shown in [6, 7]. This necessitates use of redistributive cell balancing techniques, which remove charge from higher energy cells and deliver it to lower energy cells through the use of energy storage elements, resulting in greater efficiency and minimal effect on battery run-time.

As discussed in [8], redistributive cell balancing is generally performed using methods such as line/ring shunting, capacitive/inductive energy storage methods, or common/individual cell to stack topologies. Charge shunting schemes use external energy storage devices to transfer energy between adjacent cells. There are three classifications of shunting topologies [5, 7, 9]: switched capacitor topology, single switched capacitor topology, and double-tiered capacitor topology [10]. Charge shunting techniques are effective during both charging and discharging. However, these schemes have poor efficiency, since energy needs to move through intermediate cells, and may become expensive for batteries operating in mid-SOC range [5]. Cell balancing methods using energy storage devices such as inductors and transformers are proposed in [5–7, 9]. Inductive storage element topology is limited as the charge can only be moved between two cells at a time [8].

To improve on existing techniques, the proposed system makes use of a cell-to-stack topology, where charge is either removed from one cell and distributed evenly to all cells, or removed evenly from all cells and fed back into only one. Such a converter could be implemented using various power topologies: Flyback, ramp, full-bridge, and quasi-resonant

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converters. In this paper, flyback converter in a cell to stack topology is replaced with a half-bridge switching circuit. Li-ion cells are balanced using a novel, isolated, DC/DC half bridge switching circuit, including an amalgamation of a low-level and a high-level closed-loop control for maintaining all series connected cells at the same SOC. While a half-bridge power converter could be used for bidirectional energy transfer, a unidirectional system is implemented here, for simplicity. Cell voltage and SOC are monitored, with control feedback modulating corresponding switch duty cycles to regulate current discharged from individual cells and transfer energy back to the series-connected cell stack.

Half-bridge circuit offers multiple advantages over flyback [11], such as reduction in switch voltage stress, recirculation of energy stored in transformer leakage inductance, smaller inductor size, higher efficiency, requirement of only one coupled inductor for every two cells, and the ability to control currents drawn from individual cells in ratio of corresponding duty cycles. This paper excludes discussion of SOC estimation techniques and assumes use of an existing, sufficiently accurate battery model and estimation strategies, as discussed in [12–14]. Equations governing the relationship between duty cycles, input/output voltages and input/output currents are determined, the system is simulated in MATLAB/Simulink, and the individual phases are implemented in hardware.

II. Proposed Half-bridge Cell Balancing and Operation

This section introduces the proposed DC-DC half-bridge topology and its operation, including optimization of feedback control gains for design stability.

A. DC-DC Half-bridge Topology

A novel, isolated, DC-DC half-bridge switching circuit is used to implement 25W non-dissipative cell balancing of a system using lithium-ion cells. This circuit implements a cell-to-stack balancing mechanism, with excess energy from a cell at higher SOC withdrawn and fed back to a series-connected chain of cells in a battery pack. Existing SOC estimation techniques [12], which use cell current and terminal voltage to predict SOC, are used to determine an unbalanced condition. This system offers high efficiency and many advantages over other power topologies.

Fig. 1 shows the representative schematic for a six-cell system balanced using non-dissipative half-bridge switching circuit [15, 16] . Circuit operation resumes when cells at terminal voltages V_{Cell1} and V_{Cell2}, respectively, are detected to be at different SOCs. It is assumed that $SOC(V_{Cell1}) > SOC(V_{Cell2})$ for this section. When FET1 is ON, voltage V_{Cell1} is applied across transformer primary winding, resulting in the dot-ends being at a positive potential relative to the no-dot ends. Diode D_{Sec1} conducts stored energy, simultaneously, to the output inductor and battery stack. Similarly, when FET2 is ON, a negative voltage V_{Cell2} is applied across primary, resulting in the dot-ends being at a negative potential relative to the no-dot ends, and secondary diode D_{Sec2} conducts current

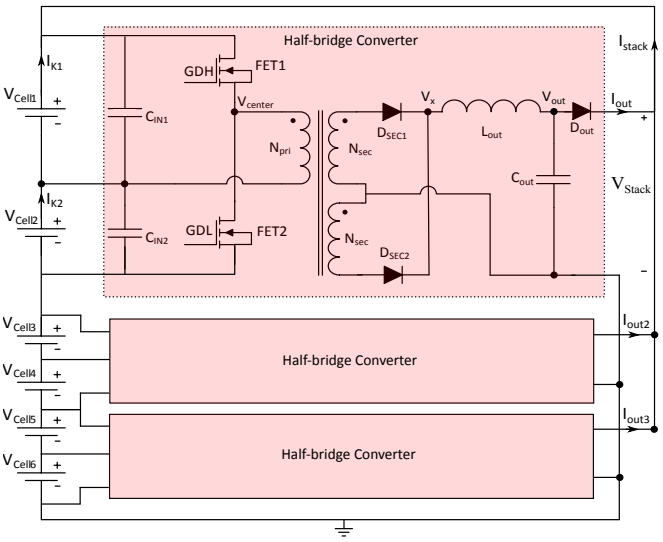

Fig. 1. Representative schematic for Half-Bridge non-dissipative cell balancing system

to the output. When gate-drive of corresponding switches (i.e. FET1 and FET2) is removed, during off-time, transformer primary magnetizing inductance is de-energized using FET body diodes, while half of secondary winding current (at the instant of turn-off) flows through each of the secondary diodes.

Half-bridge switching involves energy transfer to transformer secondary winding during on-time, against initial energy storage and transfer only during off-time in flyback converters, thereby reducing transformer size. A half-bridge circuit stresses transistors to a voltage equal to DC input voltage (i.e. cell voltage for this application) and recirculates energy stored in leakage inductance back to input DC supply. This is an advantage as compared with flyback, push-pull and forward converters, which need higher voltage rating switches and dissipate leakage energy in snubber, thereby reducing efficiency. Half-bridge circuit applies only DC cell-voltage on transformer primary winding, against double the voltage at input of a push-pull or addition of secondary voltage reflected to primary in a flyback converter, thus reducing the minimum required number of turns and scope for thicker windings and larger currents. Planar transformer is designed for optimal efficiency. This system is lower in cost, requiring one half-bridge section for a pair of cells, dissimilar to flyback design requiring a power converter for every cell.

Assuming ideal switching elements (i.e. FETs, FET1 and FET2) and output rectifier diodes (D_{Sec1} and D_{Sec2}) with zero forward voltage drops during turn-on, the relationship between switch duty cycles D_1 and D_2 corresponding to switches FET1 and FET2, respectively, is obtained as:

$$V_{out} = V_{Cell1} D_1 \frac{N_{sec}}{N_{pri}} + V_{Cell2} D_2 \frac{N_{sec}}{N_{pri}} \tag{1}$$

Since,

$$V_{Cell1} \simeq V_{Cell2} \tag{2}$$

Assuming,

$$V_C = \frac{V_{Cell1} + V_{Cell2}}{2} \tag{3}$$

and,

$$D_\Sigma = D_1 + D_2 \tag{4}$$

$$\Rightarrow V_{out} = \frac{N_{sec}}{N_{pri}} V_C D_\Sigma \tag{5}$$

where V_{out} is the output voltage (equal to cell-stack voltage), V_{Cell1} and V_{Cell2} are terminal voltages of Cell 1 and Cell 2, respectively, and N_{pri} and N_{sec} are transformer primary and half-secondary winding turns, respectively. This relation governs the minimum turns-ratio required between transformer primary to secondary windings, in order to generate required output voltage at minimum input cell voltages and maximum allowed duty cycles (D_1 and D_2). A primary-secondary turns ratio of 12 is chosen here for balancing Panasonic's NCR18650A six Li-Ion cells in series, with nominal stack voltage of 25V, approximately.

This half-bridge balancing circuit offers flexibility to command currents out of the two cells, I_{K1} and I_{K2} , which are related with the output current , I_{out}, by the relations:

$$I_{K1} = \frac{N_{sec}}{N_{pri}} D_1 I_{out} \tag{6}$$

and,

$$I_{K2} = \frac{N_{sec}}{N_{pri}} D_2 I_{out} \tag{7}$$

$$\Rightarrow \frac{I_{K1}}{I_{K2}} = \frac{D_1}{D_2} \tag{8}$$

Thus, the duty cycle ratio determines the ratio of discharge currents of the two unbalanced cells. Here, this ratio is equal to 10 for the MATLAB/Simulink simulation.

B. Transformer Design

Redistributive cell balancing systems aim to transfer energy between cells with minimum loss of energy (i.e. high efficiency of energy transfer). A planar transformer is most suitable for such applications, with switching frequency (F_s) of $100kHz$ and primary inductance (L_{pri}) of $4.3\mu H$.

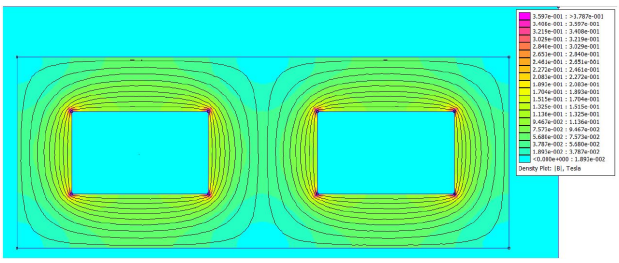

Fig. 2. Primary winding flux density

From Equation (5), it is required to obtain maximum V_{out} at minimum V_C and maximum sum of primary switch duty cycles (D_Σ) of 0.8, giving:

$$\overline{V}_{out} = \frac{N_{sec}}{N_{pri}} \underline{V_C}\ \overline{D}_\Sigma \tag{9}$$

$$\Rightarrow \frac{N_{sec}}{N_{pri}} = 12.5 \tag{10}$$

where $\overline{V}_{out}$ and $\overline{D}_\Sigma$ represent the maximum values for V_{out} and D_Σ, respectively, and $\underline{V_C}$ represents the minimum value for V_C. An integral primary-secondary turns ratio of 12 is chosen for these specifications. The FEMM tool is used to solve for transformer operation, and the primary winding is energized with a small current as shown in Fig. 2. With equations given in [17] and FEMM simulation, a primary inductance of $4.14\mu H$ and leakage inductance of $0.354nH$ is obtained. A transformer with primary inductance of $4.3\mu H$ is realized using EE14 core and 3F3 material (B_{sat} of $0.4T$ at room temperature). Fig. 3 shows the 2-PCB EE-core planar transformer used to test the experimental hardware.

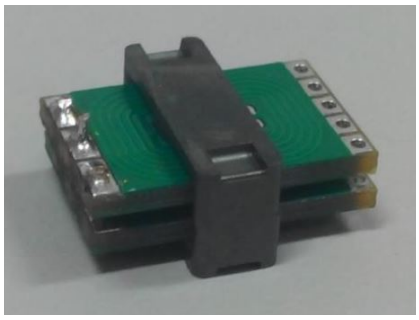

Fig. 3. Experimental hardware 2-PCB planar transformer

III. DC-DC Half-bridge Feedback Control

The goal of the proposed feedback control is to regulate a constant current into the cell-stack, while withdrawing more energy from cells at greater SOCs, using switches. The system detects if any cell is out of balance and enables the control loop. The basic control strategy is represented in the block diagram of Fig. 4 [15, 18].

It is required to break the control feedback loop at the output to see the frequency response of the open-loop system. The output current is fed back with unit gain and subtracted from the user-input current reference. This introduces a phase shift of -180 Degrees. Thus, for the unity gain feedback, we have:

$$\text{Gain} = 1\ ;\ \text{Phase} = -180^\circ \tag{11}$$

The transfer function for the proportional-integral controller is given by:

$$G_{PI} = K_p + \frac{K_i}{s} \tag{12}$$

where K_p is the proportional compensation gain and K_i is the gain for integral path. Next, modulator gain for secondary voltage V_X input and D_Σ output is given as:

$$G_{MOD} = \frac{1}{V_C} \frac{N_{pri}}{N_{sec}} \tag{13}$$

The voltage difference across output inductor induces average inductor current, which is also equal to the output current, and

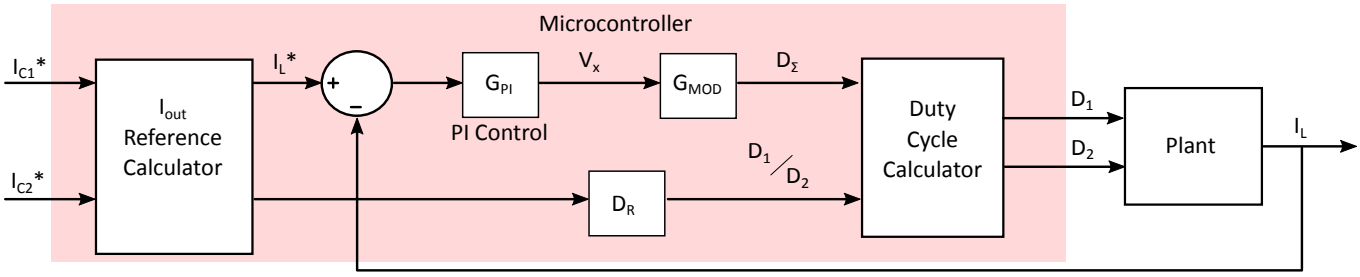

Fig. 4. Block diagram for closed-loop system

represented by the transfer function:

$$G_{plant} = \frac{N_{sec}}{N_{pri}} \frac{V_C(1 - D_\Sigma)}{sL_{out}} \; ; \; Phase = -90^\circ \qquad (14)$$

where L is the output inductance. Multiplication of these gains (or additional in log10 scale) gives the open-loop transfer function for the system, used here for stability analysis. It is required that gain curve in bode diagram crosses 0dB level with -20dB/decade slope, while maintaining phase margin at this gain crossover of at least 45 degrees for stability. Assuming $\overline{D}_\Sigma$ of 0.8 and V_{Cell} of 3.6V (nominal voltage for Panasonic's NCR18650A), the following gains for PI control ensure feedback stability:

$$K_p = 1.4 \; ; \; K_i = 100 \qquad (15)$$

The bode diagram of Fig. 5 is used to determine above values for K_p and K_i for negative feedback loop stability.

IV. Results

A. Simulation Results

The Half-Bridge switching circuit is simulated in MATLAB/Simulink for initial investigation. Fig. 6 shows switching and output current waveforms for one phase from the Simulink model of cell balancing in a six-cell series connected system for the batteries' initial SOCs shown in Table 1.

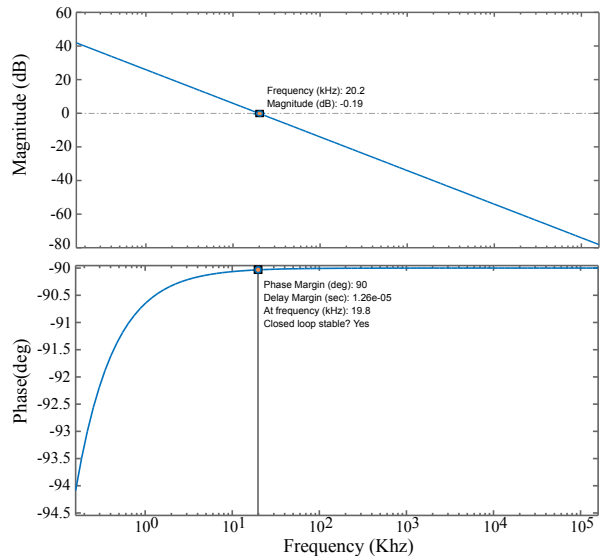

Fig. 5. Bode plot for feedback loop stability

TABLE I
Initial State of Charge for Series-Connected Cells

Cell #	1	2	3	4	5	6
Initial State of Charge (%)	84	79	74	69	66	61

It is observed that the average output current per phase reaches the user input current reference value. From equation (8), the discharge current from a cell is proportional to duty cycle of switch corresponding to a given cell. Hence, a cell at a higher SOC is discharged with a greater duty value to balance the cell SOCs in the system. For given specifications in simulation (unequal switch duty cycles), the feedback loop achieves duty cycles of 0.5 and 0.05 for D_1 and D_2, respectively. Fig. 7 depicts the implementation of a rule-based control strategy for cell balancing of a six-cell series connected system, with initial SOCs indicated above, and termination of simulation when all the cells reach equal SOC value. It is observed that the cell at lowest SOC is only being charged, while, initially, all other cells at higher SOC are being discharged with a considerable current and charged with a relatively smaller stack current. As the cells being discharged reach the minimum SOC of the system (one-by one), corresponding discharge action stops, hence reducing the stack current and the rate of increase of charge of the cells at minimum SOC. The simulation results for one phase of cell balancing in a six cell series connected system are shown in Table 2.

B. Experimental Setup

The experimental board for cell balancing of a six lithium-ion cells series-connected system is shown in Fig. 8. The PCB on the left implements three half-bridges for SOC based cell-balancing of a six cell system, with gate drive

TABLE II
Simulation Performance for One Phase of Cell Balancing in a Six-Cells Series Connected System

V_{Cell}	I_{in}	D_1	D_2	V_{out}	I_{out}	Efficiency (%)
4.03V	770mA	0.25	0.25	23.22	256mA	95.8

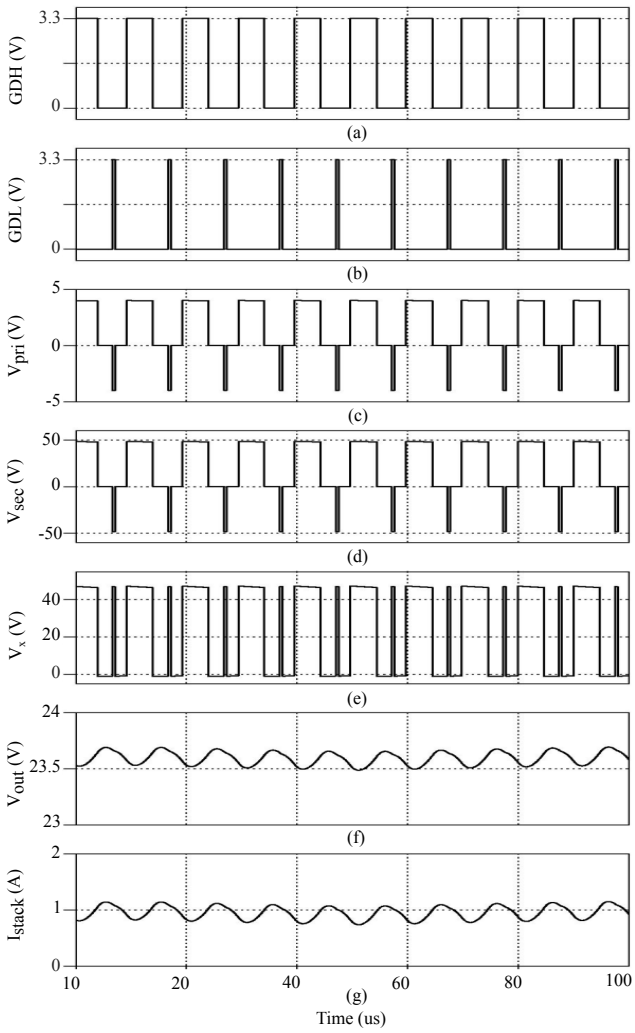

Fig. 6. Switching waveforms of half-bridge cell balancing system simulation in MATLAB/Simulink: (a) Gate-drive HS FET (b) Gate-drive LS FET (c) Transformer primary winding voltage (d) Transformer secondary winding voltage (e) Secondary diode cathode voltage (f) Output voltage (g) Output current into cell stack

logic and control feedback loop implemented in software on the Spectrum Digital eZdsp F28335 board, shown on the right. Execution code generated from MATLAB/Simulink is programmed on the TMS320F28335 controller from Texas Instruments Inc., a 32-bit micro-controller designed for control applications within the embedded space. C2000 MCU provides high resolution gate drives for power electronics and feedback control applications. Fig. 9 shows the primary switches' gate drives and V_{Center} potentials from the experimental board.

TABLE III
EXPERIMENTAL HARDWARE PERFORMANCE FOR BALANCING IN A SIX-CELLS SERIES CONNECTED SYSTEM

V_{Cell}	I_{in}	D_1	D_2	V_{out}	I_{out}	Efficiency (%)
4.03V	770mA	0.25	0.25	23.09	256mA	95.3

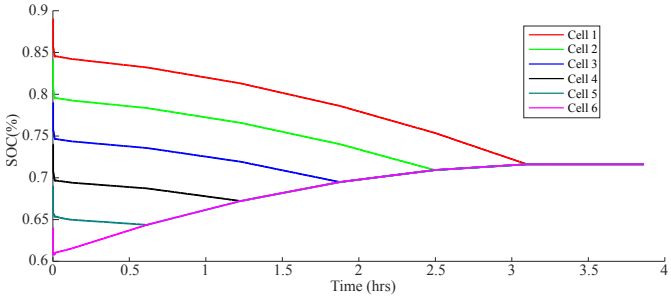

Fig. 7. Variation of cell SOC with time

Table 3 shows experimental results for one phase of cell-balancing in a six cell system. Efficiency of simulated system exceeds performance of experimental board by 0.5% due to assumption of ideal inductor coupling in MATLAB/Simulink. A coupled inductor design with nearly 1% primary to secondary coupling efficiency loss (experimental board) achieves similar results in simulation and hardware implementation.

V. CONCLUSION

This paper introduces a new DC/DC, isolated, half-bridge switching circuit for cell balancing of a series connected six cell system. Various advantages over existing systems and other power topologies are highlighted. The procedure to design a control feedback loop and planar transformer is discussed and validated. Cell balancing for a six cell (three-phase) system is simulated and implemented in hardware, with similar performance at nearly 95.3% power conversion efficiency. An effective cell balancing scheme thus realized helps in better battery capacity utilization with lesser components, smaller size, greater cell balancing efficiency and flexibility to choose individual cell discharge currents, thereby helping to improve on existing techniques.

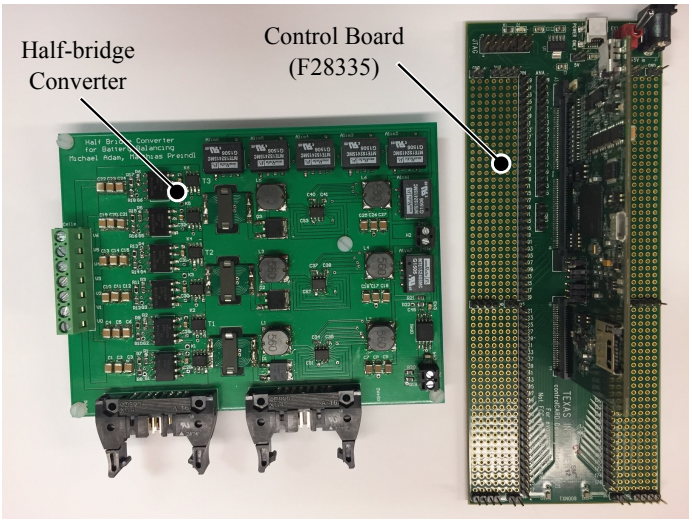

Fig. 8. Experimental board

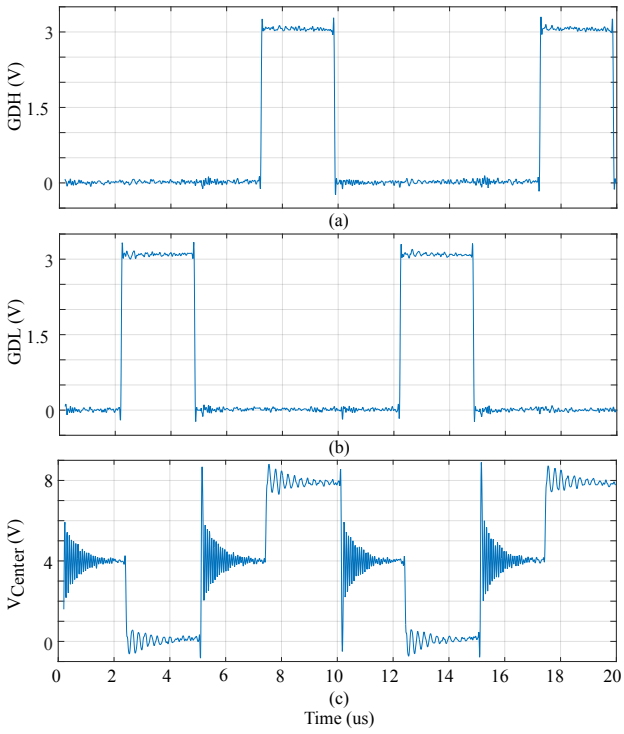

Fig. 9. Experimental switching waveforms: (a) Gate drive high (b) Gate drive low (c) Center node voltage (indicated in Fig. 1).

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