Estimating Switching Losses for SiC MOSFETs with Non-Flat Miller Plateau Region

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Abstract—Power loss calculations are critical to a power converter design, helping with estimation of efficiency, switch selection and cooling system design. Moreover, power losses in a MOSFET may limit the maximum switching frequency in a power converter. Switching energy values aren’t always available in MOSFET datasheets at all operating points, and calculation of voltage and current rise-time and fall-time is needed. This paper introduces a method to obtain an estimate of switching transition times and power losses, using datasheet parameters, for SiC MOSFETs with non-flat gate-plateau region. Three methods are discussed here, two existing and a proposed method. These methods are used to evaluate a certain MOSFET product, and calculated values are compared with results from PLECS simulation and double pulse test experiment. The proposed method is shown to yield improved accuracy.

Index Terms—Non-flat gate plateau region, SiC MOSFETs, switching loss estimation, switching transition time.

I. INTRODUCTION

Metal-oxide semiconductor field effect transistor (MOSFET) power loss estimation is critical for estimation of efficiency, thermal management and cooling system design. With advancements towards use of higher switching frequencies for power dense designs, the switching losses begin to dominate the conduction losses in MOSFETs. While conduction losses are relatively easier to calculate, switching energies may not be provided at all operating points in MOSFET datasheets. Switching losses in a device are a result of overlap of voltage ($V_{ds}$) across the device and current ($I_{ds}$) through the device [1–3]. In order to estimate switching energies, it is required to calculate rise-time and fall-time for both $V_{ds}$ and $I_{ds}$.

There exist a variety of methods for estimation of switching losses. The physical models use finite-element simulations and report best results, but could take a few days to run [4]. The behavioral models use circuit simulation softwares, such as SPICE, are faster than physical models, but exhibit long run times due to small time step. On the other hand, MOSFET switching losses can be calculated easily using analytical models, which are mathematical models based on equivalent circuits, and use values from the product datasheets. While on one hand, current rise-time ($t_{ru}$) and fall-time ($t_{fu}$) are relatively easier to calculate using MOSFET input capacitance ($C_{iss}$), on the other hand, computation of voltage rise-time ($t_{ru}$) and fall-time ($t_{fu}$) uses reverse transfer capacitance ($C_{rss}$), which varies significantly as $V_{ds}$ reduces from its maximum ($V_{ds,max}$) to its minimum ($V_{ds(on)}$) value during turn-on, and vice-versa during turn-off [5]. An existing method estimates $t_{ru}$ and $t_{fu}$ using an approximate value for $C_{rss}$, which does not represent the reverse transfer capacitance well in the whole transition interval, introducing large errors. Another method divides the transition intervals into very small sub-intervals, assumes $C_{rss}$ remains constant in each of these intervals, and calculates transition times for each of these periods [6]. These values are later added together to determine the total rise- and fall-time as $V_{ds}$ varies between its initial and final values.

A characteristic feature of few silicon carbide (SiC) MOSFETs is their non-flat miller plateau voltage ($V_p$) [7, 8]. During $t_{fu}$, when $V_{ds}$ is dropping towards $V_{ds(on)}$, almost all of the gate current flows through $C_{rss}$, but the gate-source voltage ($V_{gs}$) also increases slightly for SiC devices. This makes it difficult to determine a $V_p$ value to calculate switching transition times and switching losses using existing methods. This paper introduces an improved method for estimation of $t_{ru}$ and $t_{fu}$ for SiC MOSFETs with non-flat miller plateau region. These values are then used to compute the switching energies during turn-on ($E_{on}$) and turn-off ($E_{off}$). Assuming that $V_{gs}$ and $V_{ds}$ vary linearly during these switching transitions, the switching interval is divided into small sub-intervals, $t_{ru}$ and $t_{fu}$ calculated for each of these periods, and then added to obtain the total switching transition timings. This method is computationally inexpensive and uses values available in the product datasheets to arrive at estimates for switching energies.

This paper begins with a discussion of switching behavior in SiC MOSFETs and their comparison with Si devices in Section II, followed by a discussion of existing and proposed methods in Section III. Section IV outlines the double pulse test procedure used for experimental validation of CAS300M12BM2 SiC half-bridge module from Cree Inc., and compares switching energy values from experiment, PLECS simulation and various estimation strategies. Significant improvement in switching energy estimation is demonstrated, and conclusions presented in Section V.
to the specification $I_{ds}$ during $t_{ri}$, till $V_{gs}$ reaches $V_p$. The gate voltage now remains constant at $V_p$, while $V_{ds}$ reduces from $V_{ds,max}$ to switch-on value, $V_{ds(on)}$, during $t_{fu}$. $V_{ds(on)}$ is the product of MOSFET on-state resistance, $R_{ds(on)}$, and $I_{ds}$.

Next, the gate voltage increases further to gate driver supply level, fully saturating the MOSFET. At the time of turn-off, as shown in Fig. 1(b), $V_{ds}$ first increases from $V_{ds(on)}$ to $V_{ds,max}$ during $t_{ru}$, while gate-source voltage is at $V_p$, followed by reduction in $I_{ds}$ to zero during $t_{fi}$, as $V_{gs}$ reduces to $V_{th}$ and zero, later.

The switching behavior is different for a few of the SiC MOSFETs, such as CAS300M12BM2 from Cree Inc. As shown in Fig. 1(c) and Fig. 1(d), SiC MOSFETs exhibit a non-flat gate-plateau voltage region, with $V_{gs}$ increasing from $V_{p1}$ to $V_{p2}$, while $V_{ds}$ reduces to $V_{ds(on)}$ during turn-on, and vice-versa during turn-off, which makes it difficult to calculate switching losses, as given in [10]. The existing methods assume a constant $V_p$ to calculate $t_{ru}$ and $t_{fu}$ using (1) and (2), for the MOSFET equivalent circuit of Fig. 2.

$$t_{ru} = \left( V_{ds,max} - V_{ds(on)} \right) \frac{R_g C_{rss}}{V_p - V_{drive}} \quad (1)$$

$$t_{fu} = \left( V_{ds,max} - V_{ds(on)} \right) \frac{R_g C_{rss}}{V_{drive} - V_p} \quad (2)$$

where $R_g$ is the gate resistance. Since there does not exist a single value of $V_p$ for SiC devices, this makes it necessary to use the proposed method for an accurate estimation of transition timings, and switching losses.

### III. EXISTING AND PROPOSED METHODS

Switching transition times can be computed using (1) and (2). As mentioned earlier, these equations require $V_p$ and $C_{rss}$ values, where $C_{rss}$ varies significantly with change in $V_{ds}$ between $V_{ds,max}$ and $V_{ds(on)}$. There exist methods for approximation of $C_{rss}$ value and computation of transition times and the proposed method for SiC MOSFETs with non-flat gate plateau region.

#### A. Existing Methods

The existing methods help to determine an approximate value of $C_{rss}$ for computation of $V_{ds}$ transition times [6]. A
conventional approach, referred to as Method 1 in remainder of this text, approximates \( C_{rss} \) as the average of reverse transfer capacitance values, \( C_{rss,n} \) and \( C_{rss,1} \) in Fig. 3, at \( V_{ds,max} \) and \( V_{ds(on)} \), respectively.

\( K_2 = \frac{V_{p1}V_{ds(on)} - V_{p2}V_{ds,max}}{V_{ds(on)} - V_{ds,max}} \) (5)

Considering the MOSFET equivalent circuit of Fig. 2, (6) and (7) represent the gate current \( I_{gate} \). Since a MOSFET is a voltage controlled device [11], and offers very high input impedance, drive current from the gate driver through \( R_g \) flows through gate-source and gate-drain parasitic capacitances, \( C_{gs} \) and \( C_{gd} \) respectively, to charge and discharge them at turn-on and turn-off, respectively. Eliminating \( I_{gate} \) in (6) and (7), along with (8), (9) and (10), leads to (11), which is one of the equations used to estimate current and voltage transition times during device turn-on and turn-off [12].

\[
I_{gate} = \frac{V_{drive} - V_{gs}}{R_g} \quad (6)
\]

\[
I_{gate} = C_{gs} \frac{dV_{gs}}{dt} + C_{gd} \frac{dV_{gd}}{dt} \quad (7)
\]

but,

\[
V_{gd} = V_{gs} - V_{ds} \quad (8)
\]

and,

\[
C_{iss} = C_{gs} + C_{gd} \quad (9)
\]

\[
C_{rss} = C_{gd} \quad (10)
\]

\[
\frac{V_{drive} - V_{gs}}{R_g} = C_{iss} \frac{dV_{gs}}{dt} - C_{rss} \frac{dV_{ds}}{dt} \quad (11)
\]

Equations (3) and (11) are solved below for each of the transition intervals [9, 12], with boundary conditions known for each interval, and parameter values from the datasheet.

1) Drain-Source Current Rise-Time (\( t_{ri} \)): Fig. 1(c) shows the turn-on transient for a SiC MOSFET. In the interval \( t_{ri} \), \( V_{gs} \) increases from \( V_{th} \) to \( V_{p1} \), and \( I_{ds} \) increases from zero to its final value, \( I_{ds,max} \). Since \( V_{ds} \) remains unchanged during this time, its derivative with time becomes zero, to give (12) from (11):

\[
\int_{0}^{t_{ri}} dt = \int_{V_{th}}^{V_{p1}} \frac{R_gC_{iss}}{V_{drive} - V_{gs}} dV_{gs} \quad (12)
\]

\[
t_{ri} = R_gC_{iss}\log_{e}\frac{V_{drive} - V_{th}}{V_{drive} - V_{p1}} \quad (13)
\]

2) Drain-Source Voltage Fall-Time (\( t_{fu} \)): Once \( I_{ds} \) reaches \( I_{ds,max} \), \( V_{gs} \) increases from \( V_{p1} \) to \( V_{p2} \) and \( V_{ds} \) reduces from specification \( V_{ds,max} \) to \( V_{ds(on)} \). \( I_{ds} \) remains unchanged during this interval, indicated as \( t_{fu} \) in Fig. 1(c). From (11),

\[
\int_{0}^{t_{fu}} dt = \int_{V_{p1}}^{V_{p2}} \frac{R_gC_{iss}}{V_{drive} - V_{gs}} dV_{gs} - \int_{V_{ds(max)}}^{V_{ds(on)}} \frac{R_gC_{rss}}{V_{drive} - V_{gs}} dV_{ds} \quad (14)
\]
From (3) and (14),

\[
t_{fu} = R_g C_{iss} \log_e \frac{V_{drive} - V_{p1}}{V_{drive} - V_{p2}} + \frac{R_g C_{rss} \log_e V_{drive} - K_2 - K_1 V_{ds(on)}}{K_1} \frac{V_{drive} - K_2 - K_1 V_{ds(on)}}{V_{drive} - K_2 - K_1 V_{ds,max}} (15)
\]

3) Drain-Source Voltage Rise-Time ($t_{ru}$): During MOSFET turn-off, similar transitions happen for $V_{gs}$, $I_{ds}$ and $V_{ds}$ as during device turn-on, but in reverse order. Fig. 1(d) shows the waveforms for device turn-off. When $V_{gs}$ reduces from $V_{p2}$ to $V_{p1}$, $V_{ds}$ increases from $V_{ds(on)}$ to $V_{ds,max}$, giving (16) from (11):

\[
\int_{0}^{t_{ru}} dt = \int_{V_{p2}}^{V_{p1}} \frac{R_g C_{iss}}{V_{drive} - V_{gs}} dV_{gs} - \int_{V_{ds(on)}}^{V_{ds,max}} \frac{R_g C_{rss}}{V_{drive} - V_{gs}} dV_{ds} (16)
\]

From (3) and (16),

\[
t_{ru} = R_g C_{iss} \log_e \frac{V_{drive,off} - V_{p2}}{V_{drive,off} - V_{p1}} + \frac{R_g C_{rss} \log_e V_{drive,off} - K_2 - K_1 V_{ds,max}}{V_{drive,off} - K_2 - K_1 V_{ds(on)}} (17)
\]

4) Drain-Source Current Fall-Time ($t_{fi}$): Similar to calculation for $t_{ru}$, $I_{ds}$ reduces from $I_{ds,max}$ to zero during $t_{fi}$, while $V_{ds}$ remains constant at $V_{ds,max}$, giving (18) from (11):

\[
\int_{0}^{t_{fi}} dt = \int_{V_{p1}}^{V_{th}} \frac{R_g C_{iss}}{V_{drive} - V_{gs}} dV_{gs} \quad (18)
\]

\[
t_{fi} = R_g C_{iss} \log_e \frac{V_{drive,off} - V_{p1}}{V_{drive,off} - V_{th}} \quad (19)
\]

It should be noted that Term 1 in (15) and (17) is independent of $C_{rss}$ and $V_{ds}$, whereas Term 2 includes these factors, which vary significantly during these transition intervals. A technique similar to one proposed in [6] is used here, by dividing drain-source voltage transition interval into small sub-intervals, as shown in Fig. 3, calculating $\Delta t_{f_1}$ and $\Delta t_{f_2}$ in each of these sub-intervals, and adding them together to determine the total transition time. Let us assume there exists only one intermediate level, $V_{ds,mid}$, for simplicity of understanding. Consider Term 2 in (15), given by:

\[
t_{fu,Term2} = \frac{R_g C_{rss} \log_e V_{drive} - K_2 - K_1 V_{ds(on)}}{K_1} \frac{V_{drive} - K_2 - K_1 V_{ds(max)}}{V_{drive} - K_2 - K_1 V_{ds,mid}} (20)
\]

\[
t_{ru,Term2} = \frac{R_g C_{rss1} \log_e V_{drive,off} - K_2 - K_1 V_{ds(max)}}{K_1} \frac{V_{drive,off} - K_2 - K_1 V_{ds(mid)}}{V_{drive,off} - K_2 - K_1 V_{ds(on)}} (22)
\]

where $C_{rss1}$ and $C_{rss2}$ are the approximate values of reverse transfer capacitance, assumed constant for each of the sub-intervals, and represent $C_{rss}$ well if these sub-intervals are infinitesimally small. Similar procedure is repeated for calculating $t_{ru}$, to give (23) from (17),

\[
t_{ru,Term2} = \frac{R_g C_{rss1} \log_e V_{drive,off} - K_2 - K_1 V_{ds(max)}}{K_1} \frac{V_{drive,off} - K_2 - K_1 V_{ds(mid)}}{V_{drive,off} - K_2 - K_1 V_{ds(on)}} (23)
\]

IV. SIMULATION AND EXPERIMENTAL RESULTS

Switching times calculated above are used to estimate switching energy values given by [10, 13],

\[
E_{on} = V_{ds,max} I_{ds} \frac{t_{ru} + t_{fu}}{2} \quad (24)
\]

\[
E_{off} = V_{ds,max} I_{ds} \frac{t_{ru} + t_{fi}}{2} \quad (25)
\]

SiC schottky diodes being majority carrier devices with insignificant reverse recovery charge, SiC MOSFETs offer advantage of low reverse recovery losses from their body diodes, and the same is neglected in above equations [14, 15]. The additional term to account for effect of charging/discharging of MOSFET $C_{oss}$ is ignored, since experimental results indicate a good cancellation between $E_{on}$ and $E_{off}$ values [12]. The existing methods and proposed method is used to estimate switching energies from corresponding transition times, and compared with double pulse test experiment [16] and simulation values given by manufacturer’s models in MATLAB/Simulink with PLECS blockset for Cree’s CAS300M12BM2 SiC half-bridge MOSFET module. Since MOSFET junction thermal time constants are of the order of a few msec, the double pulse test does not increase junction temperature noticeably, and a value of 25°C Celsius is assumed for this analysis [17].
Fig. 4. Comparison of switching energy values and errors from proposed model, Method 2 and PLECS simulation at indicated $I_{ds}$ values, $V_{gs}=20/-5V$, $R_{g,ext}=2.5\Omega$ (a) Turn-on energy at $V_{ds}=300V$ (b) Turn-off energy at $V_{ds}=300V$ (c) Turn-on energy estimation error at $V_{ds}=300V$ (d) Turn-off energy estimation error at $V_{ds}=300V$ (e) Turn-on energy at $V_{ds}=800V$ (f) Turn-off energy at $V_{ds}=800V$.

Fig. 5. Comparison of switching energy values and errors from proposed model, Method 2 and double pulse test experiment at indicated $I_{ds}$ values, $V_{ds}=300V$, $V_{gs}=21/-4.44V$, $R_{g,ext}=2.5\Omega$ (a) Turn-on energy (b) Turn-off energy (c) Turn-on energy estimation error (d) Turn-off energy estimation error.
A. Simulation Results

The double pulse test circuit of Fig. 6 is simulated using manufacturer’s models in PLECS blockset of MATLAB/Simulink. Since this is an ideal system, it does not take into account effect of PCB parasitics, discussed in later sections, and results from PLECS model closely resemble switching energy values given in product datasheet. Fig. 4(a)-(f) show a comparison of switching energy values from simulation in PLECS, with results obtained using existing and proposed models for drain-source voltage of 300V and 800V. Method 1 and Method 2 are used for calculations with $V_p$ approximated as the average of $V_{p1}$ and $V_{p2}$. Method 1 clearly overestimates switching energy values, by a minimum of 140% and 400% for $V_{ds}$=300V and 800V, respectively, and hence is not reported in figures. The proposed method exhibits smaller errors from PLECS models, as compared with Method 2, which underestimates switching energies and exhibits greater errors at majority of the operating points. For $V_{ds}$=300V, Method 2 underestimates $E_{on}$ values by a minimum of 42%, with a maximum deviation of nearly 60% from PLECS simulation. The proposed model, on the other hand, exhibits a worst case estimation error of nearly 35%, with values of $E_{on}$ and $E_{off}$ cancelling each other to give total switching energy very close to PLECS values. For $V_{ds}$=800V, the estimation errors from the proposed model and Method 2 approach a maximum of 30% and 50%, respectively. The estimation accuracy of the proposed model is found to improve significantly at higher values of $I_{ds}$, as the relative magnitude of $C_{oss}$ charge/discharge current reduces with respect to $I_{ds,max}$.

B. Experimental Results

The double pulse test is used for capturing the switching transitions at the time of device turn-on and turn-off. Fig. 6 shows the double pulse test schematic and waveforms for MOSFET $M_2$. Table I lists details of equipment and components used to perform this test. In this experiment, $M_2$ is first turned ON for time $\Delta t_1$, during which inductor current $I_L$ ramps up to specification $I_{Lp}$. During this time, $I_L$ equals $I_{ds,M2}$, as shown in Fig. 6(c). MOSFET $M_1$ is permanently OFF, with $V_{gs}$ of -5V applied between its gate-source terminals. Once $I_L$ reaches $I_{ds,max}$, $M_2$ is turned OFF for time $\Delta t_2$ (2.5$\mu$s here), short enough to allow only negligible decline in $I_{ds}$ due to freewheeling of body diode of $M_1$ and circulation of $I_L$ in the indicated conduction path. On completion of $\Delta t_2$, $M_2$ is turned ON again for time $\Delta t_3$ (2.5$\mu$s here), before $M_2$ is finally turned OFF. Due to the benefits of SiC devices, the reverse recovery losses from body diode of $M_1$ are negligible at the turn-on of $M_2$, and hence ignored in calculations. The turn-off and turn-on instants at the beginning of $\Delta t_2$ and $\Delta t_3$, respectively, are used to calculate the turn-off ($E_{off}$) and turn-on ($E_{on}$) switching energies for $M_2$, respectively. Switching energy loss occurs due to the overlap of voltage ($V_{ds}$) across a device and current ($I_{ds}$) through it at the time of transition, and is the product of $V_{ds}$, $I_{ds}$ and time-step (0.4ns here). For computation of $E_{off}$, this product is evaluated from the last instant when $V_{ds}$ exits 0V, to the first time $I_{ds}$ reaches 0A, and vice-versa for $E_{on}$. These calculations of switching energies take into consideration delays of voltage probe and current transducer.

Fig. 5(a)-(d) show comparisons of switching energy values from experimental hardware with estimations using Method 2 and the proposed model. It is seen that $E_{on}$ and $E_{off}$ values from proposed model are closer to experimental results, with overestimations (by max. 30%) providing for safety margin during cooling system design. Method 2 underestimates switching losses at majority of the operating points, by nearly 20%. It may be noted that switching energy values from experiment are larger than those given in the datasheet. Fig. 7 shows the turn-off and turn-on transitions for $V_{ds}$=300V and $I_{ds}$=200A. A significant ringing is observed in waveforms for both $V_{ds}$ and $I_{ds}$ due to stray inductance of the bus bars and the half-bridge module under test, resulting in greater losses [16]. Since the proposed model does not account for effects of stray inductance, the switching times and energy loss values

**TABLE I**

<table>
<thead>
<tr>
<th>Type</th>
<th>Specification</th>
</tr>
</thead>
<tbody>
<tr>
<td>Gate Driver</td>
<td>Cree CGD15HB62P1, 9A, 1200V, 2-Ch</td>
</tr>
<tr>
<td>MOSFET</td>
<td>CAS300M12BM2, 1200V, 5 mΩ half-bridge module</td>
</tr>
<tr>
<td>$R_{q,est}$</td>
<td>2.5 Ohm</td>
</tr>
<tr>
<td>Inductor</td>
<td>80 µH</td>
</tr>
<tr>
<td>$C_{oss}$</td>
<td>5 * 500µF, 450V, B25655P4507K000, Epcos</td>
</tr>
<tr>
<td>Oscilloscope</td>
<td>Tektronix MD30324, 200MHz/2.5Gs/s</td>
</tr>
<tr>
<td>Voltage Probe</td>
<td>Tektronix P5200A, 50MHz, Differential Probe</td>
</tr>
<tr>
<td>Current Probe</td>
<td>PEM CWTUM/3/B Rogowski Current Transducer</td>
</tr>
</tbody>
</table>
are calculated for the actual $V_{ds}$ and $I_{ds}$ transition limits from hardware. The estimation errors are attributed to the initial approximation of linear variation of $V_{ds}$ with $V_{gs}$, and presence of parasitics, which could be minimized by following the recommended guidelines of layout/PCB design.

V. CONCLUSION

This paper presents an improved method for estimation of switching energies during turn-on and turn-off of SiC MOSFETs with non-flat miller plateau region. In order to validate results from proposed model, double pulse test circuit is implemented at various drain-source currents, in both PLECS simulation and hardware. It is observed that the proposed model overestimates switching energies, with values closer to actual device characteristics, in comparison with existing methods. The estimation errors are attributed to $V_{gs}$-$V_{ds}$ linear approximation and overshoots due to stray inductance in the circuit. The estimation accuracy is improved at higher values of drain-source current. The proposed method could be used for estimation of switching energies for SiC MOSFETs in cases where these values are not available in the datasheet at all required operating points.

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REFERENCES