Turn-off Energy Minimization for Soft-Switching Power Converters with Wide Bandgap Devices

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***Abstract*—The advent of Silicon-Carbide and Gallium-Nitride MOSFETs offers potential to realize higher energy density power converters operating at increased switching frequencies. The maximum switching frequency in a power converter is limited by the ability of the switching device package to dissipate its switching and conduction losses. At a given value of drain-source voltage and current, the turn-on losses in a MOSFET are usually greater than the turn-off losses. This paper introduces a soft-switching technique for power converters using wide bandgap devices to replace the larger turn-on losses with smaller turn-off losses and thus reduce the power dissipation of the overall system. The turn-off losses are further reduced with use of additional capacitance across the MOSFET drain-source terminals. Results from an analytical model, LTSpice simulation and experimentation are shown to match closely, with significant reduction in overall system losses.**

***Index Terms*—Additional output capacitance, negative inductor current, reduced turn-off losses, soft-switching.**

I. Introduction

The passive and mechanical components account for a majority of the total cost and volume of a power converter [1, 2]. Continuous efforts are being made to operate at higher switching frequencies to reduce the overall system size. Operation at high switching frequencies results in greater switching losses, making the cooling system volume larger [3]. The switching transitions involve charging and discharging of a MOSFET's parasitic capacitances. The advent of Silicon-Carbide (SiC) and Gallium-Nitride (GaN) technology based products offer lower switching losses than conventional Silicon (Si) substrate based devices. This is due to their smaller die size and reduced parasitic capacitances [4, 5]. This allows the power converters to operate at higher switching frequencies with use of these wide bandgap (WBG) devices. Despite these advantages, the maximum switching frequency is still limited by the maximum allowed junction temperature and the ability of a MOSFET package to dissipate its losses.

In order to operate at even higher switching frequency, a variety of soft-switching techniques are used to reduce the switching losses in a power converter. One of the methods, sometimes referred to as valley switching, forces the power inductor to run out of energy in every switching period to operate the converter in discontinuous conduction mode (DCM). The inductor and node capacitance resonate and the switch is turned-on at a valley in the voltage waveform [6]. This method is practical for use in low power applications, since operating in DCM for high output power results in large peak currents. Switching devices with large current ratings or paralleling of multiple devices is needed to support such large current values, which increases size and cost. A different approach eliminates the voltage and current overlap by forcing the switching current to zero before the switch voltage rises, also referred to as zero-current switching (ZCS) [7]. ZCS techniques suffer from sensitivities to line and load voltage change or excessive parasitic ringing across the power switches. Another approach uses an auxiliary resonant network connected in parallel with the switches, outside of the main power path, to implement zero-voltage switching in zero-voltage transition converters[8]. This method has utility for a limited voltage conversion range.

Given that the turn-on losses in a MOSFET are greater than the turn-off losses [9], this paper introduces a soft-switching technique to replace the higher FET turn-on and diode reverse recovery losses with smaller turn-off losses by maintaining at least slightly negative minimum inductor current. The turn-off losses are further reduced with use of an external capacitor across the MOSFET drain-source terminals, in addition to its intrinsic drain-source parasitic capacitance. The voltage clamping characteristic of a capacitor [10] serves to delay the rise in drain-source voltage at the time of turn-off. This reduces the area of overlap between voltage and current in a MOSFET and the turn-off switching energy.

There exist other methods including use of turn-off snubbers for reducing the turn-off losses in the switching devices. [11] discusses the use of a voltage controlled variable capacitor based snubber for reducing the switch turn-off loss. This technique has a demerit of moving the location of the power loss by dissipating energy of the switch output capacitors on a resistor. In another method, the use of a turn-off snubber across the output diode in the boost converter of [12] enables zero-voltage switching (ZVS) for the switching device, but results in relatively large output current ripple values. Other such techniques in [13, 14] include the use of auxiliary circuits

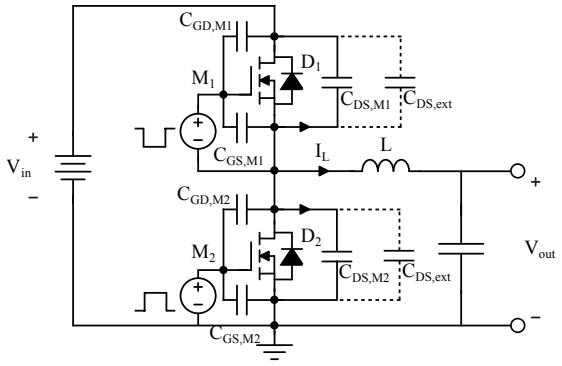

Fig. 1. Buck Converter Topology

with many additional components with the main power circuit. The proposed method only recirculates energy between the inductor and capacitors in the circuit with minimal dissipation in their parasitic resistances while using only a single additional capacitor at the output of each MOSFET.

This technique is delineated for the buck converter topology in Section II, followed by its validation using an analytical model in Section III. Section IV compares the results from the analytical model, LTSpice simulation using MOSFET models from Cree Inc., and experimentation. Section V presents the conclusion for reduction in switching losses and opportunities to operate at higher switching frequency to realize more energy dense power converter designs.

II. Proposed Soft-Switching Method

Switching losses in a MOSFET result from the overlap of the voltage V_{DS} across the device and the current I_{DS} through it at the time of turn-on (E_{on}) and turn-off (E_{off}) [15, 16]. A dead-time is included between the conduction periods of the complimentary devices in a half-bridge to prevent cross-conduction. The body diode of a MOSFET may conduct due to freewheeling action during this time, which may incur diode reverse recovery losses in case of a hard turn-on.

For a conventional buck converter shown in Fig. 1, the MOSFETs M_1 and M_2 switch complementary to each other, with a small dead time, as discussed earlier. The indicated directions of the currents in the inductor I_L and drain-source capacitors I_{CDS} are assumed positive for the remainder of this analysis. Since in a buck converter, the input voltage V_{in} is greater than the output voltage V_{out}, I_L increases while M_1 is conducting during on-time T_{on} and reduces while M_2 is conducting during off-time T_{off}, according to (1) and (2), respectively.

$$\left(\frac{dI_L}{dt}\right)_{T_{on}} = \frac{V_{in} - V_{out}}{L} \tag{1}$$

$$\left(\frac{dI_L}{dt}\right)_{T_{off}} = \frac{-V_{out}}{L} \tag{2}$$

where L is the inductance. For a buck converter, V_{out} is given in terms of V_{in} and duty cycle D according to (3),

$$V_{out} = D.V_{in} \tag{3}$$

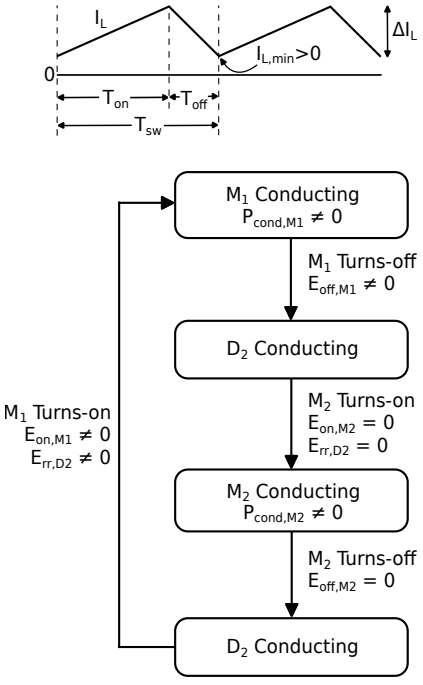

Fig. 2. Sources of power loss during a switching cycle for a buck converter with $I_{L,min} > 0$

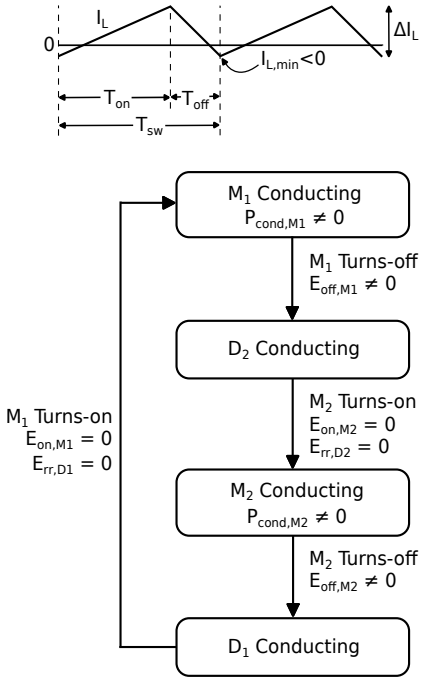

Fig. 3. Sources of power loss during a switching cycle for a buck converter with $I_{L,min} < 0$

From (1) and (3), the inductor current ripple is given by,

$$\Delta I_L = \frac{V_{in} D(1-D)}{L F_{sw}} \tag{4}$$

where F_{sw} is the switching frequency. Since ΔI_L is inversely proportional to the value of L, a buck converter with an inductance large enough such that the minimum inductor current $I_{L,min}$ is greater than zero will exhibit a switching sequence and power losses as indicated in Fig. 2. A buck converter using a smaller L, such that $I_{L,min}$ is negative, will follow a switching sequence and exhibit power losses as given in Fig. 3.

From Fig. 1, the output capacitance of the MOSFETs is given by (5),

$$C_{oss} = C_{DS} + C_{GD} \tag{5}$$

From Fig. 2, it is seen for cases when $I_{L,min}$ is positive that the energy stored in the effective output capacitance $C_{oss,M1}$ is dissipated in the FET channel at the time of turn-on, resulting in high turn-on loss $E_{on,M1}$. Reverse recovery loss $E_{rr,D2}$ also occurs at this switching instant when the conducting body diode D_2 is forced into reverse bias. Assuming 20% inductor current ripple, the losses in this system are given as [17],

$$\begin{cases} E_{cond,M1} = I_L^2 R_{ds,on} T_{on} \\ E_{off,M1} = 0.55 V_{in} I_L (t_{fi} + t_{ru}) \\ E_{cond,M2} = I_L^2 R_{ds,on} T_{off} \\ E_{on,M1} = 0.45 V_{in} I_L (t_{ri} + t_{fu}) \\ E_{rr,D2} = Q_{rr} V_{in} \end{cases} \tag{6}$$

where E_{cond} represents the conduction energy loss in the FETs and $E_{rr,D2}$ is the loss in M_1 due to flow of reverse recovery charge of D_2. The values of current and voltage rise and fall times (t_{ri}, t_{fi}, t_{ru}, t_{fu}) vary with V_{DS} and I_{DS} in a FET. For Cree's C2M0025120D SiC FET product, E_{on} is nearly twice the value of E_{off} at an operating point. If E_{off} for this device for its turn-off from (V_{in}, I_L) is equivalent to α, then the total switch energy losses for a switching period are given by,

$$E_T = I_L^2 R_{ds,on} T_{sw} + Q_{rr} V_{in} + 2.9\alpha \tag{7}$$

where,

$$\alpha = 0.5 V_{in} I_L (t_{fi} + t_{ru}) \tag{8}$$

Alternatively, the proposed method with negative $I_{L,min}$ replaces the higher sum of FET turn-on and diode reverse recovery losses with a few orders of magnitude smaller FET turn-off loss $E_{off,M2}$ (and negligible losses due to diode reverse recovery), as shown in Fig. 3. The losses for such a system with minimally negative $I_{L,min}$ are given by,

$$\begin{cases} E_{cond,M1} = 1.33 I_L^2 R_{ds,on} T_{on} \\ E_{off,M1} = V_{in} I_L (t_{fi} + t_{ru}) \approx 2\alpha \\ E_{cond,M2} = 1.33 I_L^2 R_{ds,on} T_{off} \\ E_{off,M2} \approx 0 \end{cases} \tag{9}$$

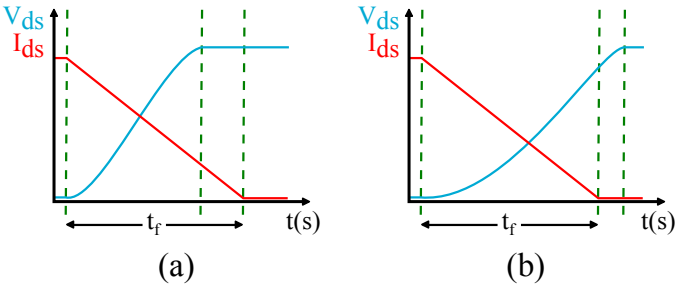

Fig. 4. Representative waveforms for voltage across and current through M_2 at turn-off (a) Without $C_{DS,ext}$ (b) With $C_{DS,ext}$.

This results in total switch energy losses for a switching period:

$$E_T = 1.33 I_L^2 R_{ds,on} T_{sw} + 2\alpha \tag{10}$$

Given that the WBG devices have a small $R_{ds,on}$, the total switch losses when $I_{L,min} < 0$ are smaller that the losses with $I_{L,min} > 0$. The ratio E_{on}/E_{off}, at a particular operating point, is even higher for some devices, such as Cree's CAS120M12BM2, enabling greater benefits with use of the proposed method. In a system with varying V_{in} and V_{out} (and hence duty cycle), the feedback loop will vary F_{sw} in order to maintain at least a small negative value for $I_{L,min}$ according to (4), while following the characteristics of Fig. 3. The turn-off losses $E_{off,M1}$ and $E_{off,M2}$ in M_1 and M_2 respectively, can further be reduced with use of additional capacitance $C_{DS,ext}$ across the MOSFETs' drain-source terminals, as shown in Fig. 1. Fig. 4 shows representative waveforms for V_{DS} and I_{DS} during the turn-off of a MOSFET. While on one hand, reduction in I_{DS} is controlled by the gate-source voltage V_{gs}, on the other hand, the increase of V_{DS} is also determined by the magnitude of M_1 and M_2's effective output capacitance, $C_{oss,M1}$ and $C_{oss,M2}$, respectively. Due to the voltage clamping property of a capacitor, addition of $C_{DS,ext}$ reduces the rate of rise of V_{DS}, reducing the energy loss due to the voltage/current overlap during turn-off. This is equivalent to a reduction in the multiplication factor of 0.5 assumed while calculating switching losses for ideal switching behavior in [17]. The non-linear behavior of V_{DS} at the beginning and end of turn-off transition is due to the variation of the FET C_{oss} with V_{DS}, with large values in nF range for small values of V_{DS}. The addition of $C_{DS,ext}$ does not induce additional turn-on losses in the FETs due to the nature of the waveforms and recirculation of energy between the inductor and the capacitors for the case when $I_{L,min}$ is negative. The value of $C_{DS,ext}$ is limited by the operating F_{sw}, to ensure that the longer turn-off time does not occupy a majority of the switching period. An analytical approach to model this behavior is introduced in later sections and its results are compared with simulations using Cree's LTSpice models for discrete FET product C2M0025120D and experimentation, to verify the proposed technique of reduction in turn-off losses.

III. The Analytical Model

A soft-switching technique to reduce the switching losses in presence of negative $I_{L,min}$ and use of $C_{DS,ext}$ was discussed earlier.

A linear recursive model to mimic the FET turn-off characteristic and the effect of use of additional $C_{DS,ext}$ is presented here. Fig. 5 shows the current flow path at various time instants during the turn-off of M_2. Let us assume that the effective output capacitance of M_1 and M_2, including additional $C_{DS,ext}$, is represented by $C_{DS,M1}$ and $C_{DS,M2}$, respectively. Initially, I_L is negative and M_2 is conducting, as shown in Fig. 5 (a). Fig. 5 (b) shows the current path at the moment of initiation of turn-off of M_2, when $V_{gs,M2}$ begins to reduce from its ON-level of 20V. Since an inductor opposes a change in flux (and hence current through it) according to Faraday's Law [18], let us assume I_L remains unchanged during the small turn-off interval of the order of a few $nsec$. As $I_{DS,M2}$ reduces from its peak value, currents $I_{CDS,M1}$ and $I_{CDS,M2}$ of total magnitude equal to the difference of I_L and $I_{DS,M2}$ flow through $C_{DS,M1}$ and $C_{DS,M2}$ repectively, increasing $V_{DS,M2}$, according to (11),

$$I_L = I_{DS,M2} + I_{CDS,M1} + I_{CDS,M2} \tag{11}$$

$$I_{CDS,M1} = -C_{DS,M1}\frac{dV_{DS,M1}}{dt} \tag{12}$$

But,

$$V_{DS,M1} = V_{in} - V_{DS,M2} \tag{13}$$

From (12) and (13),

$$I_{CDS,M1} = -C_{DS,M1}\frac{d(V_{in} - V_{DS,M2})}{dt} \tag{14}$$

Since V_{in} is instantaneously constant,

$$I_{CDS,M1} = C_{DS,M1}\frac{dV_{DS,M2}}{dt} \tag{15}$$

$$I_{CDS,M2} = C_{DS,M2}\frac{dV_{DS,M2}}{dt} \tag{16}$$

from (11), (15) and (16),

$$I_L = I_{DS,M2} + (C_{DS,M1} + C_{DS,M2})\frac{dV_{DS,M2}}{dt} \tag{17}$$

According to (17), the output capacitance of the two FETs are equivalent to be placed in parallel for the inductor current distribution. Assuming that $I_{DS,M2}$ reduces linearly with drop in $V_{gs,M2}$, $V_{DS,M2}$ rises towards V_{in} (for an ideal body diode D_1). Once $V_{DS,M2}$ exceeds V_{in}, D_1 begins to conduct while $I_{DS,M2}$ continues to reduce to zero. With addition of a large $C_{DS,ext}$, it is possible for $I_{DS,M2}$ to reach zero before $V_{DS,M2}$ reaches V_{in}, as shown in Fig. 4 (b). In this case, for the remainder of the time from the instant $I_{DS,M2}$ hits zero till $V_{DS,M2}$ reaches V_{in}, the output capacitors are charged by the nearly constant I_L, as shown in Fig. 5 (d), followed by conduction of D_1 marking the completion of I_L commutation from M_2 to M_1, as shown in Fig. 5 (e). A similar process is repeated during current commutation from M_1 to M_2 with positive maximum inductor current, $I_{L,max}$.

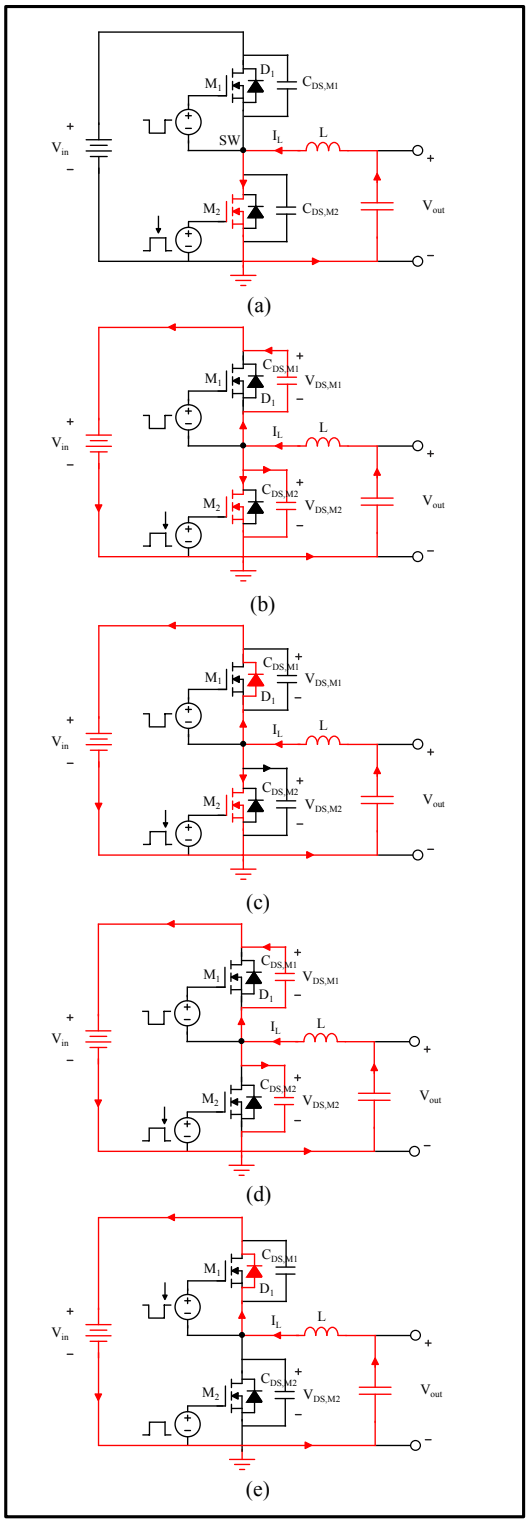

Fig. 5. Switching sequence and current paths during turn-off of M_2 for the buck converter of Fig. 1 (a) Before initiation of turn-off (b) While $I_{DS,M2}$ is reducing and output capacitors are charging (c) Case when $V_{DS,M2}$ reaches V_{in} before $I_{DS,M2}$ reaches 0 (d) Case when $I_{DS,M2}$ reaches 0 before $V_{DS,M2}$ reaches V_{in} (e) End of current commutation.

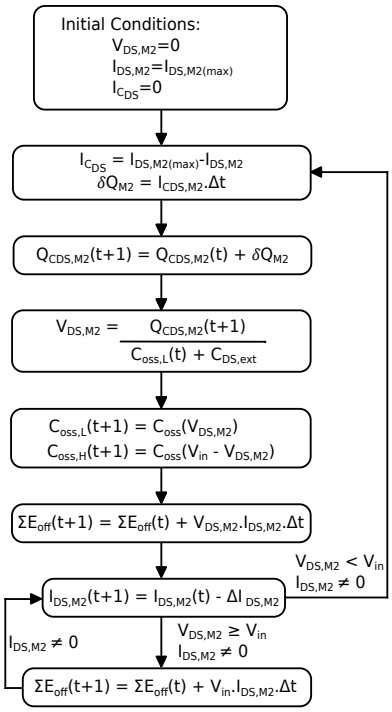

Fig. 6. Analytical recursive model implemented in MATLAB to assess turn-off behavior of FET M_2.

Fig. 6 shows the block diagram for the recursive model implemented in MATLAB. The model begins with M_2 conducting and $V_{DS,M2}$ and $I_{DS,M2}$ at their minimum and maximum values, respectively. For the infinitesimally small time interval Δt during the turn-off time of M_2 obtained from equations in [19] using the datasheet parameters, a small charge δQ is delivered to the output capacitors of the FETs due to the current $I_{C_{DS}}$ flowing through them. This charge builds incrementally on the capacitors. The new drain-source voltage is computed, and values of effective output capacitances are updated, owing to their non-linear behavior. The turn-off energies from each of the small intervals are added to the summation from the previous iterations, and the process repeats till $I_{DS,M2}$ reaches zero. The results of $E_{off,M2}$ computation using this model are presented in later sections.

IV. Simulation and Experimental Results

The proposed soft-switching technique is validated for the buck converter of Fig. 1, using the above analytical model, LTSpice simulation using device model for C2M0025120D from Cree Inc., and experimentation using hardware in [20]. The switching energy computations from experiment are compensated for the delays induced by the probe parasitics. Fig. 7 shows the variation in turn-off losses in M_2 for different values of additional capacitance across its drain-source terminals. The results using the three validation methods match closely. The losses from experimentation and simulation in LTSpice are slightly different from those predicted by the analytical model

TABLE I
Test conditions, components and equipments used for testing

Type	Specification
Input Voltage	200V
Output Voltage	100V (Duty cycle=0.5)
Switching Frequency	3 kHz
$I_{DS,max}$	34A
MOSFET	C2M0025120D,1200V/90A/25mΩ SiC MOSFET
Gate Driver	IXDN609SI, $R_{g,ext}$= 6.67 Ω
Inductor	256μH
Oscilloscope	Tektronix MDO3024, 200MHz/2.5GS/s
Voltage Probe	Tektronix TPP0250, 250MHz, 3.9pF/10MΩ
Current Sensor	PEM CWTUM/3/B Rogowski Current Transducer

since a linear variation in V_{DS} and I_{DS} is assumed during turn-off, which is not the real case.

This analysis uses test conditions, components and equipment listed in Table I. In order to observe the switching transitions and the degree of reduction in switching loss with use of large additional capacitance, the converter is operated at a switching frequency of 3kHz with a relatively large value of inductance. For the same value of output current, the value of switching losses without $C_{DS,ext}$ is lower to 68.9% of those with positive $I_{L,min}$. As the external capacitance is increased from zero to $5nF$, the turn-off losses in M_2 are reduced to 37.3% of their original value, helping to reduce the total switching losses to 25.5% of the case with positive $I_{L,min}$. The increase in the inductor losses due to larger current ripple with negative $I_{L,min}$, is minimal in comparison with switching energy savings in MOSFETs with use of this method. This offers an opportunity to go higher in switching frequency while staying within the device power dissipation limits to design a higher energy density system. Alternatively, operation at the same switching frequency would result in

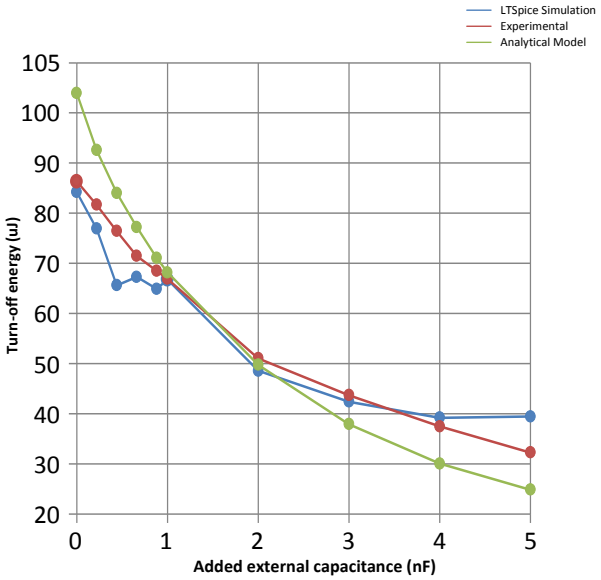

Fig. 7. Reduction in turn-off losses with addition of external capacitance across M_2 drain-source terminals.

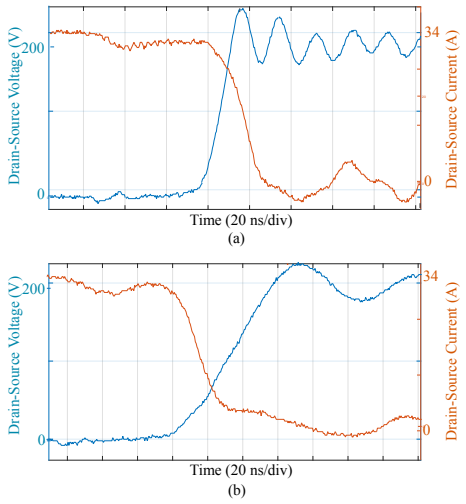

Fig. 8. Switching waveforms for turn-off of M_2 for test conditions given in Table I (a) Without external drain-source capacitance (b) With external drain-source capacitance of 5nF.

lower system losses with need for smaller heat sink of lower cost. It should be noted that external capacitance is added only to the output of M_2 for this analysis, and use of a capacitor at the output of M_1 would help to reduce losses further. Fig. 8 shows the waveforms for turn-off of M_2 for the case of zero and $5nF$ of external capacitance added across its drain-source terminals. It is seen that due to the voltage clamping characteristic of the additional capacitor, the voltage waveform is delayed and has a smaller rate of increase, reducing the voltage/current overlap to result in smaller switching energy loss. It also reduces the frequency of resonance between the stray inductance of the bus bars and FET output capacitances which appears as an overshoot in V_{DS}, making it easier to achieve EMI compliance.

V. Conclusion

This paper presents a soft-switching method to reduce system losses in a buck converter with negative minimum inductor current. The turn-off loss is diminished to 37% of its original value, and total switching losses to 25.5% of their value in a system with positive minimum inductor current and no additional output capacitance. Results from an analytical model proposed to validate this technique closely match the switching energy values obtained from simulation using manufacturer's device models in LTSpice and experimentation. With a majority of power converter topologies including a half-bridge, this technique can be extended to reduce losses in other such systems. It is planned to validate this soft-switching technique in hardware for a power converter operating at high power and switching frequency for an estimate of its advantages in terms of the losses and volume of the overall system.

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