Variable-Frequency Critical Soft-Switching of Wide-Bandgap Devices for Efficient High-Frequency Nonisolated DC-DC Converters

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***Abstract*—This paper derives a variable-frequency critical soft-switching control method for nonisolated DC/DC converters using wide-bandgap devices. The critical soft switching control technique under maximum frequency trajectory is introduced to maintain zero voltage switching over a wide range of modulation ratios according to the load variation. The concept prevents turn-on losses that are typically much larger than the turn-off losses in SiC and GaN FETs and the latter can be further reduced by adding external drain-source capacitors. We have derived the boundary conditions for critical soft switching operation. For the reduction of inductor value and volume, a maximum available switching frequency is applied to the converter within the constraints of device requirement and soft switching boundary conditions. We demonstrate experimentally that the proposed concept reduces the power losses in the wide-bandgap devices by a factor of approximately 3, enables an increase of the switching frequency by a factor of about 5, and a decrease of the main inductance by a factor of about 10. Then variable frequency critical soft switching control method is proposed with the constraints to maintain the maximum frequency within soft switching operation. Since our test bench uses off-the-shelf inductors, the inductors are subject to significant high frequency losses. Despite this, the converter efficiency increases by 1%.**

***Index Terms*—DC-DC power converters, electric variables control, pulse width modulation converters, soft-switching, zero voltage switching**

I. Introduction

Hybrid and electric vehicles require a range of power electronic converters. A typical drivetrain requires one (or two) inverters to interface electric machines, an optional DC-DC converter to interface the battery, an auxiliary power module to power the auxiliary 12V system and charge the low voltage lead-acid battery, and a battery charger [1]. Full-sized DC-DC converters tend to have a large volume and weight due to the DC filter requirements. Therefore, several drivetrain implementations omit a DC converter and interface the battery directly with the inverters. However, this approach requires the motor drive to operate with variable DC since the battery voltage can vary up to 40% between empty and full. Consequently, the motor drive needs to be designed such that it can provide the rated torque and power at minimum voltage resulting in higher-than-necessary current requirements and an increased VA rating of the motor drive.

Hence, the use of a DC-DC converter to interface the battery has advantages but improvements in terms of power density are required. The Department of Energy (DoE) and US automobile manufacturers specify the power density targets as >3.0kW/L for 2020 and 4.6kW/L for 2025 [2]. Typical strategies to increase the power density are 3-level converter designs [3], interleaving [4], or increasing the switching frequency, e.g. using wide-bandgap devices. Each approach results in challenges. Multilevel converters tend to increase the system complexity; interleaving reduces the size of the output capacitor requirements but does not affect the size of the filter inductor, which is typically the largest components; and large switching frequencies increase the power losses in the semiconductors that must be limited according to the thermal device limits. This paper proposes a variable-Frequency Critical Soft-Switching (VF-CSS) for nonisolated DC/DC converters using wide-bandgap devices. VF-CSS has the potential to significantly increase the switching frequency without causing significant losses in the switching devices.

Power electronic devices feature conduction and switching losses. Conduction losses result from the device on-state current and voltage, and are independent of the switching frequency. The switching losses, on the other hand, depend on the switching transition values for the device voltage and

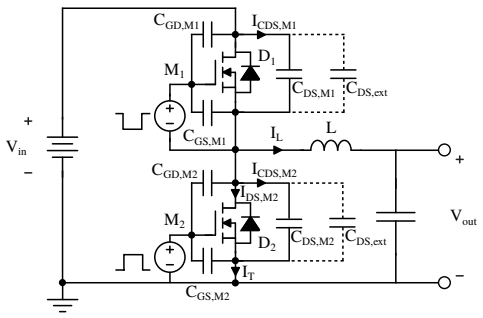

Fig. 1. FET buck converter topology with optional additional output capacitors for critical soft-switching.

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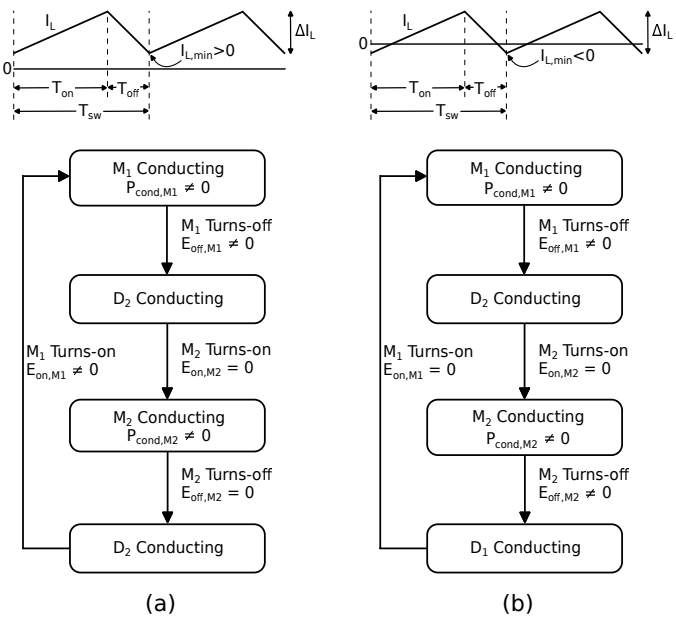

Fig. 2. Switching events and the associated losses during a switching time period in a buck converter with (a) $I_{L,min} > 0$ (b) $I_{L,min} < 0$.

current, and increase with switching frequency [5]. While the values and size of the passive components reduce with increase in switching frequency [6], the maximum switching frequency is limited by the ability of the device package to dissipate the losses occurring in it.

A transition from Silicon to Silicon-Carbide (SiC) or Gallium-Nitride (GaN) materials based wide bandgap (WBG) devices offers potential to go higher in switching frequency, with the given device power dissipation limits. This is due to the smaller die size and parasitic capacitances of the WBG devices which reduces the losses incurred in each of the switching transitions [7, 8]. In order to achieve operation at even higher switching frequencies, soft-switching techniques are used to reduce switching losses. These techniques reduce the voltage-current overlap by switching on/off the device at an instant when either of the device voltage or current is at a small value [9, 10, 11]. These techniques suffer from sensitivities to line or load voltage change or are restricted to a limited voltage conversion range. Alternative techniques use turn-off snubbers that move turn-off losses from the semiconductor to an external device [12, 13, 14, 15] and require auxiliary circuits that increase the system complexity and cost.

Variable-Frequency Critical Soft-Switching (VF-CSS) replaces the greater turn-on losses with smaller turn-off losses (FET turn-on losses tend to exceed the turn-off losses by a factor two to ten) in a switching cycle with negative minimum inductor current in a buck converter [16, 17, 18]. The existing methods either change the switching on/off instants of the device when the V-I overlap is small or introduce auxiliary circuits to transfer the switching losses from main circuit to external device. The former method may be influenced by the load variation and the latter method can increase the controlling complexity and system cost compared to the VF-CSS. Unlike many alternative soft-switching techniques [19],

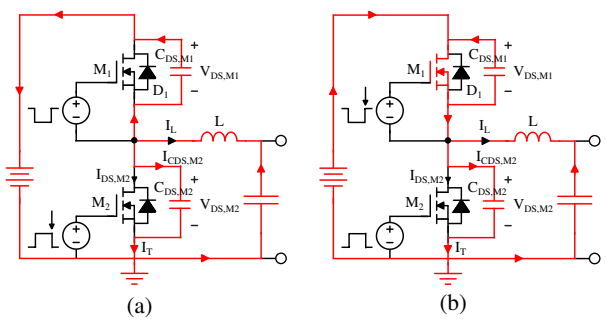

Fig. 3. FET buck converter hard switching due to insufficient time to discharge the output capacitors (a) current flow just before turn-on of M_1 (b) current flow after M_1 is turned-on with excessive losses.

the proposed method retains proportionality between duty cycle and output voltage such that traditional converter control techniques can be employed. Turn-off losses tend to be small due to the voltage clamping characteristic of the device output capacitor that can be further enhanced. An additional capacitor across the FET drain-source terminals further reduces the rate of increase of drain-source voltage and the resultant voltage-current overlap at the time of device turn-off. This soft-switching method requires use of minimum number of additional components with no added losses in the device channel at the time of turn-on, due to only recirculation of energy between the passive components in the dc-dc converter. Compared to the traditional methods, the controlling complexity of the VF-CSS is simpler because only extra maximum frequency control is needed to achieve a large constant current ripple. And the system cost is lower because only paralleled capacitors are added to further decrease the turn-off losses without extra circuit to deliver the switching losses. Lastly, because the variable frequency critical soft switching method applies the highest available freuqency within the critical soft switching boundary conditions, the inductor value can be further decreased and the power density can be accordingly improved.

This paper derives the boundary conditions and critical soft switching control method with maximum frequency control to reduce switching losses and operate a 1kW buck converter using GaN devices in the MHz range. In Section II, the paper begins with a discussion of the soft-switching method and design considerations for buck converter topology. In section III, the different working stages during the soft switching operation of the buck converter are shown in detail to illustrate the zero voltage turn-off soft switching mechanism from GaN Systems and the reduction in its turn-off losses with use of additional capacitance [17]. The derivation of boundary conditions for critical soft switching operation is analyzed. The VF-CSS boundary conditions are derived with dead time and peak/valley inductor current according to the device data sheet and integrations. Also, the soft switching ranges of typical GaN and SiC devices are shown for analysis and comparison. In Section IV, the VF-CSS controlling method is introduced based on the boundary conditions. The highest frequency can be achieved in every operating point to ensure the critical soft switching. Section V presents the results for the reduction

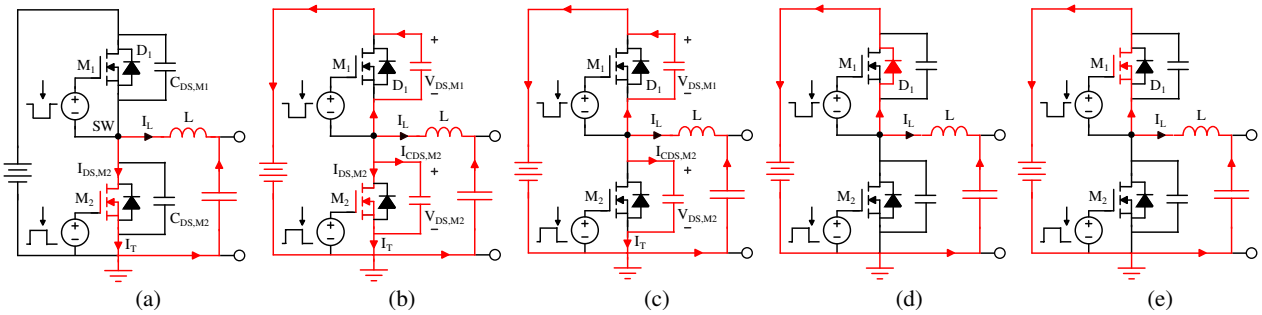

Fig. 4. FET buck converter critical soft switching: analytical representation of the different stages during M_2 turn-off shown on the right-hand side of Fig. 5: current conduction (a) before $t_{off,1}$ when M_2 is ON, (b) between $t_{off,1}$ and $t_{off,2}$ when $I_{DS,M2}$ is reducing and the output capacitors are charging, (c) between $t_{off,2}$ and $t_{off,3}$ when $I_{DS,M2}$ reaches zero while current flows through the additional capacitors, (d) between $t_{off,3}$ and $t_{off,4}$ completion of turn-off of M_2 and reverse conduction through M_1 , (e) current conduction after $t_{off,4}$ when M_1 is ON.

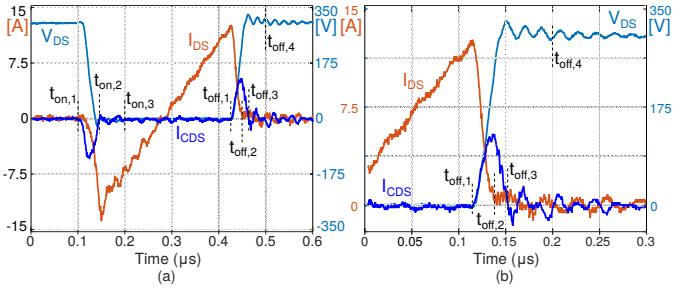

Fig. 5. Waveforms for the turn-on and turn-off of M_2 with use of additional 330pF capacitor with the FETs. V_{DS}, I_{DS} and I_{CDS} are the drain-source voltage, drain-source current and the current through the additional output capacitance with M_2, respectively.

in turn-off losses with added capacitance, calculated using the analytical model and validated in hardware. The critical soft-switching variable frequency control method is shown to enable operation at 1 MHz switching frequency with significantly reduced losses in the switching devices as compared to a traditional buck converter with positive minimum inductor current and hard-switching. The conclusions in Section VI summarize the benefits of the proposed control method and the potentials to develop in different applications.

II. Critical Soft-Switching Operating Mechanism

The FETs in the buck converter of Fig. 1 switch complementary to each other with a suitable dead-time to avoid cross-conduction. Since an inductor opposes an instantaneous change in its current according to Faraday's law, one of the FETs exhibit reverse conduction characteristic during the dead-time, resulting in zero-voltage switching (ZVS) on the corresponding device. GaN devices do not have an intrinsic body diode and the associated reverse recovery losses but are capable of reverse conduction with a relatively larger voltage drop equal to the sum of the gate threshold voltage and the negative gate drive voltage in off-state condition [16]. This reverse conduction characteristic of GaN FETs in the off-state condition is modeled and referenced as anti-parallel body diode operation in this paper. Depending on the value of the output current I_{out} (equal to the average inductor current $I_{L,0}$) and the inductance L, the minimum inductor current $I_{L,min}$ may be positive or negative. Fig. 2 shows the sequence of switching events and the associated losses during a switching cycle in a buck converter with positive and negative $I_{L,min}$. In the linear soft-switching (SSW) method, $I_{L,min}$ is intentionally made negative to enable ZVS behavior at turn-on for both the switches [17, 18]. The greater turn-on losses in M_1 are replaced with smaller turn-off losses in M_2 reducing the total losses per switching cycle. The degree of reduction in switching losses depends on the ratio of the turn-on and turn-off losses which varies between devices. The turn-on losses of the GaN Systems GS66516T GaN FET are nine times the turn-off losses at 400V/20A [16]. Similarly, the turn-on losses of the Wolfspeed C2M0025120D SiC FETs exceed the turn-off losses by a factor of three at 800V/20A. Turn-off losses can be further reduced with an additional capacitance across the FET drain-source terminals that reduces switching losses by 25% or more [17].

While a negative $I_{L,min}$ is needed to reduce the switching losses, this current should be sufficiently large to charge and discharge the FET output capacitors within the dead-time. A system with large additional FET output capacitors and a small switching dead-time would cause large instantaneous currents through the FET channel charging/discharging these capacitors, inducing excessive additional losses. Fig. 3 shows the current paths during the occurrence of such a phenomenon during the turn-off of M_2. Initially, the negative I_L is discharging M_1's output capacitance $C_{DS,M1}$ and charging M_2's output capacitance $C_{DS,M2}$ while M_2 drain-source current $I_{DS,M2}$ has reduced to zero, as shown in Fig. 3(a). M_2 drain-source voltage $V_{DS,M2}$ is at an intermediate value between zero and buck converter input V_{in}. At the turn-on instant of M_1, the remaining charge on $C_{DS,M1}$ is instantaneously removed through the M_1 channel. Another large current charges $C_{DS,M2}$ to V_{in} through M_1. Both these instantaneous currents cause excessive losses in M_1 and increase the system losses, opposite of what is intended with the use of the VF-CSS method. A similar phenomenon would occur during the turn-off of M_1. Thus, the degree of capacitive loading on the FETs and the benefits of reduction in switching losses are limited by the values of the dead-time and $I_{L,min}$.

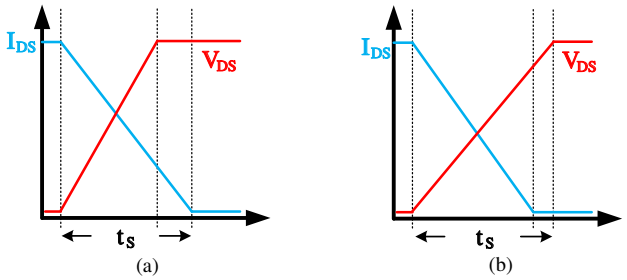

Fig. 6. Turn-off drain-source voltage and current with limited parasitic output capacitance: (a) inherent switching waveforms, (b) waveforms with additional output capacitor.

III. Derivation Of Boundary Conditions For Critical Soft Switching

A. Analytical Model

The different stages of the FET turn-off behavior are described with an analytical model [17] and depicted in Fig. 4 for the turn-off of device M_2. The black arrows and red arrows represent the reference directions and actual directions of the current flows. And the default directions of the drain-source output capacitor voltage and current are both from drain to source. For buck converters, the inductor current is approximately constant during a switching transition and has the value

$$I_L = -I_{DS,M2} - (C_{DS,M1} + C_{DS,M2})\frac{dV_{DS,M2}}{dt}, \qquad (1)$$

during the turn-off of M_2. The experimental GS66516T FET turn-off waveform is shown in Fig. 5. Initially, the buck converter is operated with 300V V_{in} and 200V V_{out} in no-load condition (i.e. $I_{L,0} = 0$) with inductor current varying between $\pm$13A. Turn-off of M_2 is initiated at time $t_{off,1}$, when $I_{DS,M2}$ begins to reduce from its peak value. $C_{DS,M1}$ and $C_{DS,M2}$ begin to discharge and charge, respectively, and $V_{DS,M2}$ increases, shown in Fig. 4(b). At time $t_{off,2}$, M_2 ceases to conduct, while there is still finite current through $C_{DS,M1}$ and $C_{DS,M2}$, shown in Fig. 4(d). Time $t_{off,3}$ marks the completion of the turn-off of M_2 with $I_{CDS,M2}$ reduced to zerom $V_{DS,M2}$ reaches V_{in}, and the reverse conduction through M_1 is shown in Fig. 4(e). Reverse current through M_1 during the $t_{off,3} - t_{off,4}$ interval involves much greater conduction losses, as discussed earlier. From (1), the value of inductor current I_L flowing through $C_{DS,M1}$ and $C_{DS,M2}$ is proportional to their respective values. In this analysis, equal values of additional capacitors are used across the drain-source terminals of the two FETs, resulting in equal currents through the capacitors at the time of turn-off. Since the soft-switching method results in a symmetrical system, the current $I_{CDS,M1}$ during the turn-off of M_2 is similar to $I_{CDS,M2}$ during the turn-off of M_1 between $t_{on,1} - t_{on,2}$, which have the same magnitude as $I_{CDS,M2}$ between $t_{off,1} - t_{off,3}$ when the magnitudes of $I_{L,max}$ and $I_{L,min}$ are equal. During the turn-on of M_2 in Fig. 5, $C_{DS,M2}$ first discharges to zero (represented by finite $I_{CDS,M2}$ during $t_{on,1} - t_{on,2}$), followed by reverse conduction through M_2 with a large on-state voltage drop between $t_{on,2} - t_{on,3}$.

Besides the VF-CSS method for ensuring the critical soft-switching operation, the additional capacitors in parallel with the switches can further decrease the turn-off losses. The mechanism of the additional capacitors is shown in Fig. 6. To reduce the turn-off losses, the overlap of drain-source current and voltage should be addressed. During the transient of turn-off, the decrease of drain-source current, I_{DS}, is mainly dependent on the gate-source voltage, Vgs. However, the increasing slope of the drain-source voltage, V_{DS}, is largely determined by the effective output capacitance of the switches, C_{oss}. By adding external capacitors, the effective switching capacitance can be increased. Thus, the increasing rate of the drain-source voltage, $\mathrm{d}V_{DS}/\mathrm{d}t = I_{CDS}/C_{oss}$, can be slowed down. So, the overlap of the I_{DS} and V_{DS} is decreased and the turn-off losses will be correspondingly reduced. However, the value of the additional capacitor cannot be too large because a big external capacitor can slow down the turn-off time of the switch. If the turn-off transient period is larger than the dead time, the soft switching operation will be influenced and extra losses may occur due to the failure of zero voltage soft switching. Thus, the value of the additional switch capacitor should be designed considering both the overlapping area of drain-source current/voltage and the dead time for critical soft switching operation. The critical soft switching is based on the boundary conditions of dead time and inductor current which will be analyzed in detail in section III. And the boundary conditions should be derived based the external capacitor and the intrinsic switch capacitance. For the additional capacitor design of this paper, the turn-off losses are mainly taken into consideration to guarantee the critical soft switching. In the following section, an optimal external capacitor value is shown for reference.

Fig. 7 shows the M_2 turn-off waveforms of GS66516T FETs. Adding an external drain-source capacitance $C_{DS,ext}$ with values from zero to 430 pF, the I_{DS} fall-time changes negligibly while the V_{DS} increase from zero to V_{in} is slower. The current I_{CDS} is zero in Fig. 7(a) due to absence of additional FET output capacitance. The magnitude of I_{CDS} increases with increase in value of $C_{DS,ext}$. A reduced rate of increase of V_{DS} due to the voltage clamping characteristic of the added capacitance reduces the voltage-current overlap (the overlap of cyan line and red line in Fig. 7) and the losses during the turn-off of a FET, as indicated by the analytical model. The analytical model in [17] is modified for the use of additional capacitors across the drain-source terminals of both the FETs in the buck converter, and shown in Fig. 8.

B. Boundary Conditions

The critical soft switching operation of the buck converter can be guaranteed by restricting the dead time and peak/valley inductor current to a certain range. As is shown in Fig. 4, for the turn-off switching transition period of M_2, a large current ripple is required to ensure negative valley inductor current to be lower than a threshold current level. When M_2 is turning off, the negative inductor current will discharge the output capacitor of upper switch, $C_{DS,M1}$. The zero voltage switching (ZVS) of the upper switch can be achieved

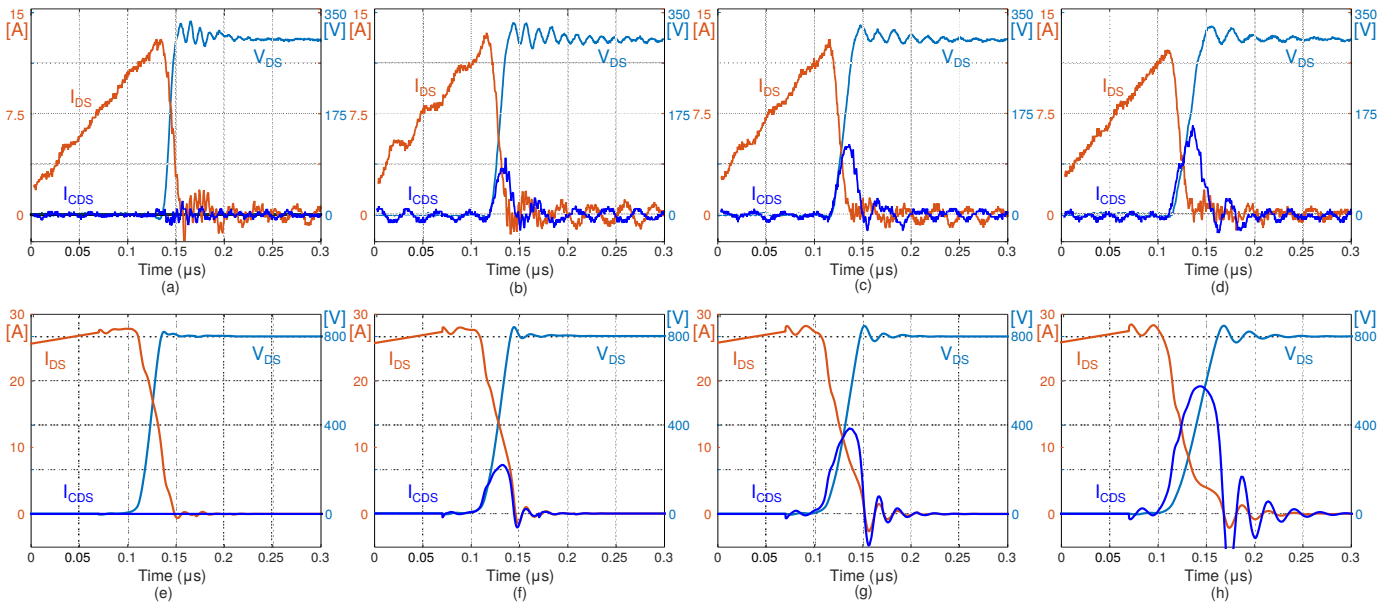

Fig. 7. GaN and SiC FET waveforms showing the turn-off of M_2 with use of additional capacitors across its drain-source terminals; GaN FET with (a) no $C_{DS,ext}$ (b) $C_{DS,ext} = 100pF$ (c) $C_{DS,ext} = 220pF$ (d) $C_{DS,ext} = 430pF$; SiC FET with (e) no $C_{DS,ext}$ (f) $C_{DS,ext} = 220pF$ (g) $C_{DS,ext} = 470pF$ (h) $C_{DS,ext} = 1nF$, V_{DS}, I_{DS}, and I_{CDS} are the drain-source voltage, drain-source current and the current through the additional output capacitance with M_2, respectively.

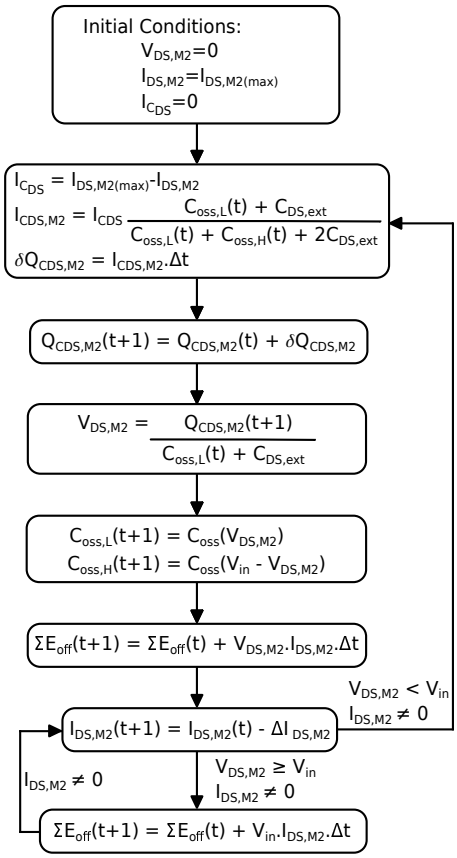

Fig. 8. Estimation of M_2 turn-off losses with zero and non-zero external drain-source capacitance $C_{DS,ext}$.

if the $C_{DS,M1}$ is fully discharged before it turns on. The ZVS operation depends on the interlock time between two switches and the value of inductor valley current. According to Fig. 4(b), the inductor valley current is

$$I_{L,min} = -I_{DS,M2} + I_{CDS,M1} - I_{CDS,M2}, \tag{2}$$

where $I_{DS,M2}$ is the drain current, $I_{CDS,M1}$ and $I_{CDS,M2}$ are the current through the switch output capacitance of switch M_1, M_2, respectively

$$I_{CDS,M1} = C_{DS,M1}\frac{dV_{DS,M1}}{dt}, \tag{3a}$$

$$I_{CDS,M2} = C_{DS,M2}\frac{dV_{DS,M2}}{dt}. \tag{3b}$$

Since ($V_{DS,M1}$+$V_{DS,M2}$) equals to the constant input source voltage V_{in}, $I_{L,min}$ is expressed as

$$I_{L,min} = -I_{DS,M2} - (C_{DS,M1} + C_{DS,M2})\frac{dV_{DS,M2}}{dt}. \tag{4}$$

The above current equations can be further analyzed by the integral calculation over time and V_{ds}, respectively.

$$\int_0^{T_d} I_{L,min} + I_{DS,M2}(t)\,dt = Q_{min} = \tag{5}$$
$$\int_0^{V_{in}} -C_{DS,M1}(V_{DS,M2}) - C_{DS,M2}(V_{DS,M2})\,dV_{DS,M2},$$

where $Q_{min} \leq 0$ is the total charge moved in the output capacitors. Assuming that I_{ds} is varying linearly with time, the left-hand side of (5) becomes

$$\int_0^{T_d} I_{L,min} - \left(I_{L,min} - \frac{I_{L,min}}{T_d}t\right)\,dt = \frac{1}{2}I_{L,min}T_d. \tag{6}$$

Therefore, the M_2 turn-off sequence shown in Fig. 4 achieves critical soft switching when

$$\tfrac{1}{2}I_{L,min}T_d \leq Q_{min} \leq 0. \tag{7}$$

Similar, the maximum positive inductor current for M_1 turn-off sequence is achieved when $\frac{1}{2}I_{L,max}T_d \geq Q_{max} > 0$, where $Q_{max} = |Q_{min}|$ and $I_{L,max} = -I_{L,min}$.

The design of the converter should satisfy the two inequalities to guarantee the critical soft switching operation. The integral of switch output capacitance to drain-source voltages can be calculated based on the datasheet provided by the device manufacturer.

Then, the model of critical soft switching method can be expressed with the function image in Fig. 9. It can be shown that the blue regions are the feasible soft switching range according to the constraints of inequalities (7) with the maximum and minimum dead time requirement. Also, the soft switching ranges of typical GaN and SiC devices are given in Fig. 9. During operating in the following sections, the dead time and peak/valley inductor current can be controlled within the critical soft switching region to reduce the switching losses with maximum frequency.

IV. Control Method

The operating principle of the VF-CSS is based on a double loop controller. As is shown in Fig. 10, the controlling block of the DC/DC converter includes a double loop voltage-current controller and a variable-frequency controller. In the double loop controller, the output voltage is adjusted with a reference value, V_o*. The error of the outer loop voltage controller will provide the reference for the inner loop inductor current, i_L*. The desired duty cycle, d*, will be calculated for PWM signal and the variable-frequency controller. The variable-frequency controller can tune the frequency to maintain a large constant current ripple based on the calculated duty cycle, sampled output voltage and pre-defined inductor current ripple. The calculation of frequency is based on equation (7) to ensure the critical soft switching. In the frequency controller, a maximum available frequency will be traced according to the boundary conditions of critical soft switching operation. The value of frequency is adjusted in every sampling period based on the marginal soft switching trajectory to meet the zero

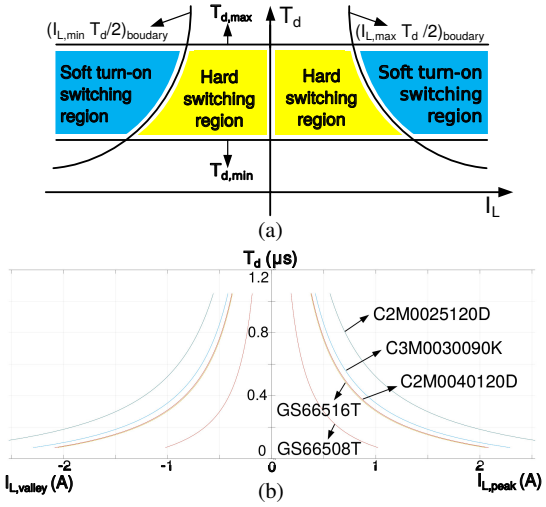

Fig. 9. (a) soft switching operation regions and (b) device characteristics

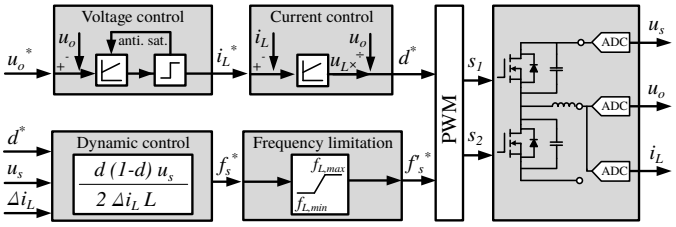

Fig. 10. The controlling blocks for the VF-CSS method.

voltage turn-off with high frequency. The frequency trajectory is shown in Fig. 11. Then, the calculated frequency will be limited within a range considering the device and switching loss requirements.

In this section, the proposed frequency control method is introduced. The control law is based on the critical soft switching boundary constraints derived in section IV and the rated operating condition with specific current parameters. The soft switching strategy is implemented to reduce the value of passive filter components by introducing a large current ripple, e.g. $\Delta i_L = 220\% - 300\%$. In the meantime, the high turn-on losses are replaced by the lower turn-off losses, thus the efficiency can be further improved. The following subsections show the detailed method of controlling the frequency to achieve soft switching based on the boundary conditions.

A. Feasible working regions for soft switching control with $f_{s,min}$ and $f_{s,max}$

The limitations of max/min frequency for control mainly include two parts: (a) peak/valley current constraints caused by the device limitation and soft switching threshold; (b) switching frequency constraints caused by the dead time and sampling requirement.

1) Peak/valley current constraints: For a given device, the peak/valley current cannot exceed the maximum current provided by the datasheet which is related to the ripple and the average current:

$$I_{L,peak} = I_{L,ave} + \frac{\Delta i_L}{2} \leq I_{L,max} \tag{8a}$$

$$I_{L,valley} = I_{L,ave} - \frac{\Delta i_L}{2} \geq -I_{L,max} \tag{8b}$$

$I_{L,peak/valley}$ is the peak/valley inductor current, and $I_{L,max}$ is the maximum allowable current for the device. Because the

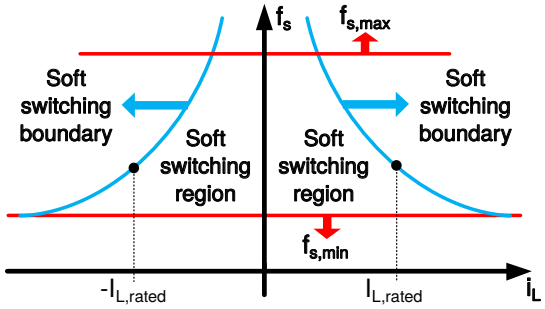

Fig. 11. Maximum frequency trajectory for critical soft switching control.

inductor current ripple is expressed as:

$$\Delta i_L = \frac{d(1-d)V_s}{f_s L} \tag{9}$$

So, the minimum allowable frequency can be derived as:

$$\Delta i_{L,max} = 2(I_{L,max} - I_{L,ave}),\ I_{L,ave} \geq 0 \tag{10a}$$

$$\Delta i_{L,max} = 2(I_{L,max} + I_{L,ave}),\ I_{L,ave} \leq 0 \tag{10b}$$

$$f_s \geq \frac{(1-d_{0.5})d_{0.5}V_s}{\Delta i_{L,max} L} \tag{11}$$

where $d_{0.5}$ is the midpoint of the duty $d_{0.5} = 0.5$.

The function between frequency and inductor current is reciprocal and the feasible region for frequency should be above the reciprocal curves. Because in every sampling point, our control law will choose the maximum frequency (minimum ripple) to meet the soft switching constraints, this lower boundary of reciprocal function can be easily satisfied. So, we just substitute the rated value in table (taking C2M0025120D as example) and the $f_{s,min}$ is calculated as 61 kHz.

For the soft switching operation, as is illustrated in the previous section, the minimum/maximum of the inductor current should be lower/higher than a specific threshold value, I_{th}:

$$I_{L,peak} = I_{L,ave} + \tfrac{\Delta i_L}{2} \geq I_{th} \tag{12a}$$

$$I_{L,valley} = I_{L,ave} - \tfrac{\Delta i_L}{2} \leq I_{th} \tag{12b}$$

where I_{th} is the threshold current derived from the soft switching constraints.

According to the soft switching constraints in Fig. 9, for a given device, if the dead time is known, then the minimum value of I_{th} can be derived. Thus, for the design of controlling blocks, the maximum allowable frequency, $f_{s,max}$, should satisfy the soft switching boundary of I_{th} with the rated current as is shown in Fig. 11:

$$\Delta i_{L,min} = 2(I_{L,ave} + I_{th}),\ I_{L,ave} \geq 0 \tag{13a}$$

$$\Delta i_{L,min} = 2(-I_{L,ave} + I_{th}),\ I_{L,ave} \leq 0 \tag{13b}$$

$$f_s \leq \frac{(1-d_{0.5})d_{0.5}V_s}{\Delta i_{L,min} L} \tag{14}$$

Similarly, the function between f_s and i_L is reciprocal and the feasible region for frequency should be lower than the reciprocal curve. According to the parameters of typical device, the $f_{s,max}$ is calculated as 612 kHz on the rated point. In this situation, a fixed ripple current is controlled by the frequency in the steady state when the average current is equal to rated value. If the frequency is constrained below the maximum frequency according to the soft switching boundary, the soft switching operation will always be satisfied within the rated current.

However, if we want to further expand the boundary of $f_{s,max}$, the soft switching boundary of I_{th} can be satisfied in a smaller value of average current within the rated bandwidth. So, as is shown in Fig. 12, if the converter is operating within a smaller current than the rated value, a smaller ripple current is needed by the soft switching constraints. Then the maximum frequency boundary will be increased to some extent. However, in this situation, the increment of $f_{s,max}$ is constrained by other factors: power dissipation, dead time and sampling requirement.

2) Switching transient and sampling constraints: Firstly, if the $f_{s,max}$ is to be increased, for the accuracy of duty cycle, the dead time should be decreased accordingly. However, in the proposed method of soft switching boundary conditions, the dead time is set to be constant. To limit the influence of switching transients on the effective duty cycle, the switching frequency is upper bounded to a maximum value:

$$f_s \leq f_{s,max} \tag{15}$$

The switching frequency is an integer multiple of the sampling frequency. A given control implementation requires a minimum sampling frequency that is achieved by lower-bounding the switching frequency:

$$f_s \geq f_{s,min} \tag{16}$$

In this working condition, the 100 kHz is set to be the minimum frequency, f_{smin}, which will satisfy the least requirement of sampling.

To conclude the above four types of frequency constraints, the allowable range of frequency is [100 kHz, 600 kHz] in the condition of fixed duty cycle (duty=0.5). If the converter is working under a wide range of output voltage, the duty cycle is becoming another variable for the constraints of frequency range. So, considering the above two main constraints that influence the frequency, every value of inductor current and duty cycle will determine a maximum and minimum allowable frequency. Thus, a 3D frequency constraint diagram is derived and shown in Fig. 13 according to the above inequanlities in this section:

After considering the variation of duty cycle, the allowable inductor average current is related to the frequency and ripple current according to equation (8)-(16) and the 3D diagram of the frequency range is shown in Fig. 13(a). For the purpose of illustrating the 3D ranges of frequency with the function

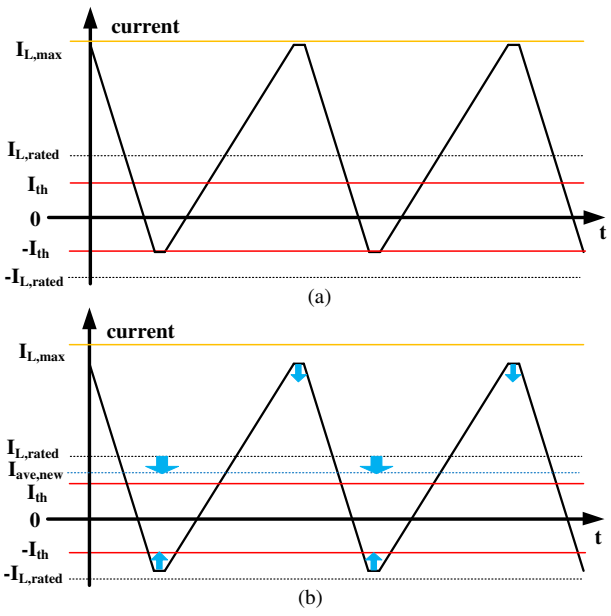

Fig. 12. (a) device constraints and lowest ripple maintaining the soft switching boundary at a given average current and (b) expanded frequency when the average current is lower than the rated value

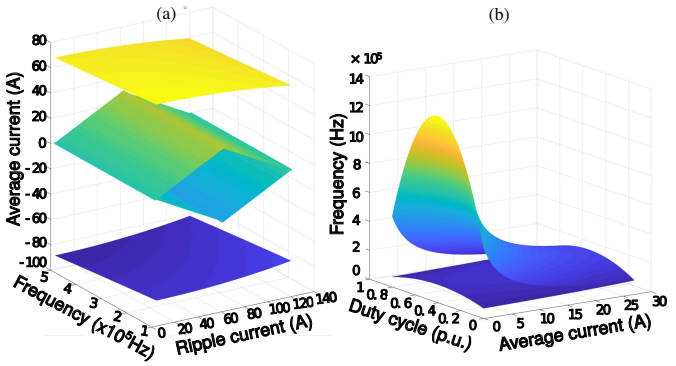

Fig. 13. The soft switching, frequency and device current constraints (a) of ripple current with the function of frequency and inductor average current (b) of frequency with the function of duty cycle and inductor average current.

of duty cycle and inductor average current, equation (9) is used for substituting the ripple current with duty cycle. The frequency 3D ranges are shown in Fig. 13(b). And the ranges in Fig. 13(b) are applied in the frequency controller to limit the frequency within the allowble level in every sampling period.

B. Control law for soft switching boundaries

For the proposed variable frequency controlling method, if the load has variations, the control law will check the minimum and maximum points of the inductor current according to the inequalities in each sampling period. In this situation, the controller will change the frequency based on the derived threshold current value and make the ripple current satisfy the boundary condition of soft switching.

$$f_s = \begin{cases} \frac{(1-d)dV_s}{2(i_{L,ave}+I_{th})L} & \text{if } i_{L,ave} - \frac{(1-d)dV_s}{2Lf_s} \geq -I_{th}, \\ \frac{(1-d)dV_s}{2(I_{th}-i_{L,ave})L} & \text{if } i_{L,ave} + \frac{(1-d)dV_s}{2Lf_s} \leq I_{th}. \end{cases} \quad (17)$$

In the meantime, the frequency is also constrained within a range based on Fig. 13(b) in every sampling period according to the inductor average current and duty cycle. It can be seen from the control law inequalities that the average inductor current has a reciprocal function with frequency according to the soft switching boundary as is shown in Fig. 11. So, when the load is changing, the frequency controller will check the peak/valley current values and find the minimum ripple (maximum frequency) to satisfy the soft switching boundary within the frequency ranges. The controlling blocks have been shown in Fig. 10 which include two parts: voltage and current control and frequency control.

V. Simulation and Experimental Results

The VF-CSS method is validated using the discussed analytical model and in hardware with the GaN Systems Inc. GS66516T-EVBDB daughter board used with the GS665MB-EVB motherboard in a buck converter topology. Fig. 15 shows the hardware used for testing the specifications of Table I. The system evaluated in open-loop with a duty cycle of 0.67 that generates a 200 V steady-state output from 300 V input voltage and 1 MHz switching frequency. The operation point is chosen as an intermediate between D=0.5 resulting in the highest switching frequency (1.13 MHz with the given setup), and duty ratios tending to 0 and 1 with significantly lower switching frequency (lower bounded to 100 kHz).

In terms of the test bench of 300/200V DC/DC converter, the main application is to interface the battery in the electric vehicle (EV). Between the battery and the traction inverter of the EV system, the voltage should be adjusted by a DC/DC converter to satisfy both the limitation of battery pack and DC link requirement of the inversion system. The proposed method and test bench applies large current ripple and small inductor value to achieve critical soft-switching. The power density and efficiency are improved which is of significance for the on-board EV system. The 300/200V converter is a general voltage range which can be adjusted further for the vehicle application. For example, the DC link voltage provided by a Li-Ion battery of BMW i3 is approximately 360V and varies between 270 to 400V. Also, the battery pack voltages of Prius or Prius plug in are 201V and 207V, respectively. So, the 300/200V converter can be suitable interface in the EV battery application.

The waveforms for the drain-source voltage V_{DS}, total M_2 switch position current I_T and the current through the added capacitance I_{CDS} are recorded. These waveforms are calibrated for the probe offsets and delays. Current through the M_2 channel I_{DS} is computed as the difference of I_T and I_{CDS}. It should be noted that I_{DS} still includes the current charging the parasitic output capacitance inherent to the device at the time of turn-off, but which does not contribute to the actual turn-off loss [20]. According to (1), since the current through the output capacitors varies in proportion to their instantaneous values, this current through the internal capacitance could be computed and subtracted from I_{DS} to get the actual current through the M_2 channel for a more accurate calculation of its turn-off losses. The losses from experiment are calculated as the time integral of the product of the instantaneous V_{DS} and I_{DS} for M_2.

Fig. 14 shows the variation in the turn-off losses with use of an additional capacitance between zero to 430pF across both the FETs in the buck converter. It is seen that the turn-off losses reduce on loading with additional capacitance according to both the analytical model and in hardware. The analytical model predicts a reduction of the the turn-off losses by a factor of approximately 4 (22.1%) using a $C_{DS,ext}$ = 430 pF.

TABLE I
Test conditions, components and equipment used for testing

Type	Specification
Input Voltage	300 V
Output Voltage	200 V (Duty cycle D = 0.67)
Switching Frequency	100 kHz to 1.13 MHz (1 MHz at D = 0.67)
Output Power	No-Load to 1 kW
FET	GS66516T, 650V/60A/25mΩ GaN FET
Gate Driver	SI8271GB-IS, $R_{g,ext}$(On/Off)= 10 Ω/2 Ω
Inductor	SER2915L-222KL, 2.2 μH
Capacitor	MKP1848C61280JK2, 12 μF
Oscilloscope	Tektronix MDO3024, 200MHz/2.5GS/s
Voltage Probe	Tektronix TPP0250, 250MHz, 3.9pF/10MΩ
Current Sensor	PEM CWTUM/3/B Rogowski Current Transducer

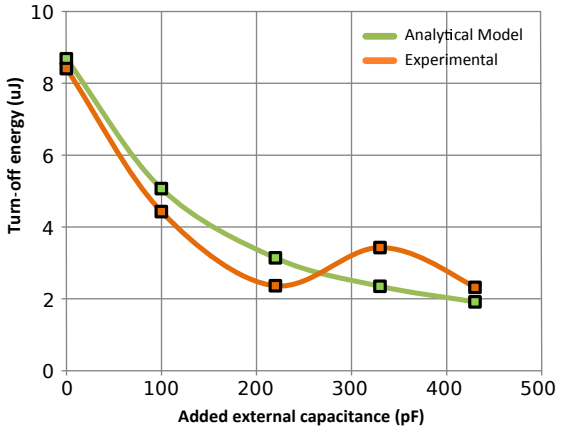

Fig. 14. Reduction in the turn-off losses using the analytical model and in experiment (with and without effect of current in the FET inherent parasitic capacitance) with addition of external capacitance across FET terminals.

The experimental losses are evaluated with double-pulse tests. The losses are shown to decrease from 8.41 μJ to 2.31 μJ by adding $C_{DS,ext}$ = 430 pF corresponding to approximately a loss reduction of a factor of 4 (27.6%). Furthermore, the measured losses follow closely the predicted values by the analytical model that confirms the ability to predict FET turn-off losses with and without $C_{DS,ext}$ using the proposed technique.

For the hardware setup, a GaN based GS665MB-EVB with GS66516T-EVBDB buck converter half bridge module and C2M0025120D SiC FET based Converter are tested for the proposed controlling method. The GaN setup is shown in Fig. 15. And SiC test bench is a three-phase two-level converter (3 phase legs) topology as is shown in Fig. 16. Only one phase is used for the DC/DC converter experiments. The SiC setup mainly includes: three-phase converter board, component board, three phase inductors micro-controller/interface board: (a) Converter board: The converter board is composed of SiC FET (C2M0025120D)*6, gate driver (CRD-001)*6, DC bus capacitors (B32774D8505K, 5μF)*9, DC voltage sensor (RP1215D) and inductor current sensor (CKSR15). (b) Component board: The component board includes three phase capacitors (B32774D8126K000, 12μF)*9, voltage sensor (RP1215D)*3, current sensor (CKSR 25-NP)*3, power relay (T9SV1K15-12)*3. Because only one phase is needed for the DC/DC experiments, one current sensor and voltage sensor are soldered for testing. (c) Inductor: A planar inductor is optimized using the Litz wire to improve the efficiency with high inductance and high DC bias current (0.08mH). (d) Micro-controller/interface board: The TMS320F28379D is used as the micro-controller to generate the PWM signals for the DC/DC converter. Because the gate driver of the SiC needs 15V input and the output PWM from the TI controller is 3.3V, an interface board is added in between to regulate the PWM voltage to satisfy the gate driver requirement.

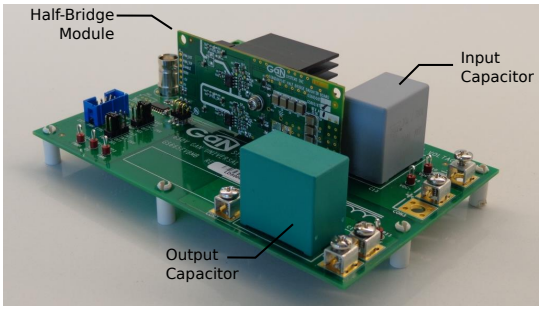

Fig. 15. Experimental hardware of the buck converter using GaN Systems GS665MB-EVB motherboard with GS66516T-EVBDB half-bridge module.

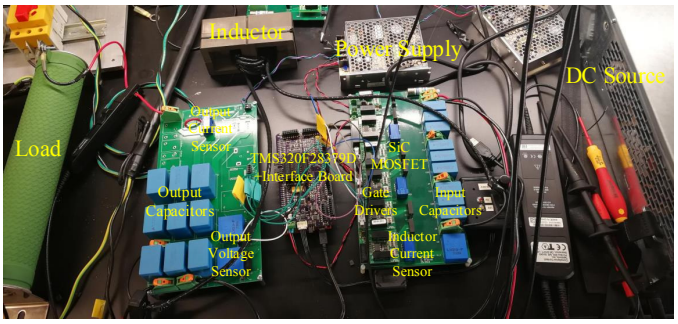

Fig. 16. Experimental hardware of the buck converter using C2M0025120D SiC FET.

Next, the GaN and SiC converters are tested with an output power P_{out} from 0 kW to 1 kW, respectively. The increase in P_{out} and $I_{L,0}$ reduces the magnitude of the negative $I_{L,min}$ from the no-load condition. Firstly, for the GaN based test bench, Fig. 17 shows the waveforms for M_2 with P_{out} of 1kW and 330pF additional capacitors with the FETs. Since the magnitude of $I_{L,max}$ is greater than $I_{L,min}$, the amplitude of I_{CDS} is greater at the turn-on instant than at the turn-off instant. This causes a faster commutation from M_1 to M_2 than from M_2 to M_1. The values for voltage and current are measured at the buck converter input and output terminals to determine the overall system losses with increase in P_{out}. In order to estimate the benefits with the use of the VF-CSS method, the buck converter is also tested with a larger 20.7 μH inductance (realized using 23 units of Coilcraft's SER2009-901MLB 0.9 μH inductors in series) and positive $I_{L,min}$ with hard-switching (HSW). Due to the large turn-on losses, the HSW system can be operated only up to 500W at the same 300 V input and duty cycle. For comparison reasons, the HSW results are extrapolated to 1 kW. The results are shown in Fig. 21. For the SiC based test bench, the drain-source voltage, gate source voltage inductor current and output current waveforms are shown in Fig. 19. A zoomed view of the switching transients are shown in Fig. 20. The observations can be derived as following:

1) The VF-CSS losses increase marginally with the load current, i.e. P_{out}, as shown in Fig. 21 (a) and (c). VF-CSS results in nearly constant losses since conduction losses tend to dominate the switch losses. Furthermore, the current at the FET turn-off instant varies within a limited interval as a function of the output current. This behavior is in contrast with HSW, where the device and converter losses significantly increase with P_{out}, as shown Fig. 21 (b) and (d).

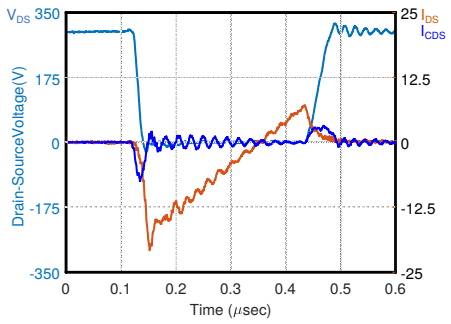

Fig. 17. GaN FET M_2 turn-on and turn-off waveforms with additional 330pF output capacitor at 1kW output power. V_{DS}, I_{DS} and I_{CDS} are the drain-source voltage, drain-source current and the current through the additional output capacitance with M_2, respectively.

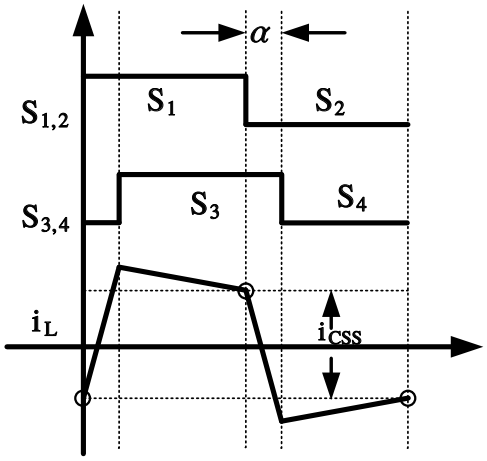

Fig. 18. VF-CSS waveforms of an isolated converter.

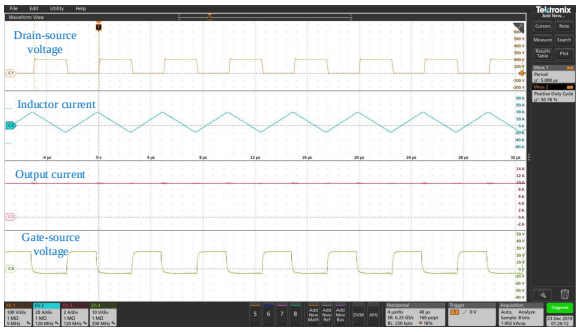

Fig. 19. SiC FET drain-source voltage, gate-source voltage, inductor current and output current under full load.

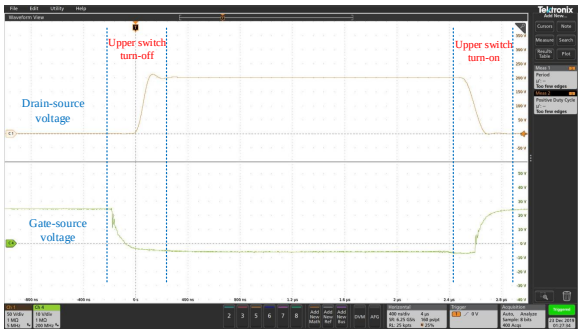

Fig. 20. SiC FET zoomed in switching transients.

2) VF-CSS results in significantly reduced losses in the switches (approximately a factor of 3) compared to HSW, as shown in Fig. 21 (a) and (b).
3) For small output powers ($P_{out} \leq 200$ W), HSW tends to zero current switching while VF-CSS retains the switching principle. Hence, the HSW losses decrease as the power decreases while the VF-CSS are approximately constant.
4) VF-CSS requires an inductance of L=2.1μH and HSW requires L=20.7μH. Hence, VF-CSS operates with an inductor that is approximately an order of magnitude smaller.
5) As outlined, the test-bench uses Coilcraft off-the-shelf inductors for simplicity. These inductors result in significant AC losses for large high-frequency ripples since they are operated outside their design specifications. Consequently, the inductor accounts for $\geq$ 50% of the total converter losses using VF-CSS. In contrast, the inductor accounts for about 10% of the losses using HSW. Hence, there is a strong potential to improve the VF-CSS converter losses of with a custom inductor. On the other hand, the HSW converter losses can be improved only marginally as the inductor operates in near-ideal conditions.
6) Despite the dominant inductor losses, the VF-CSS converter features a higher efficiency compared to the HSW converter above about 1/3 of the rated output power, as shown in Fig. 21 (c) and (d). At the rated output power, the VF-CSS is estimated to yield at least an 1% efficiency improvement (that can be further optimized with a dedicated inductor).
7) The VF-CSS switching losses can be reduced using an output capacitance, e.g. $C_{DS,ext}$ = 330 pF, as shown in Fig. 21 (a) and (c). However, since the turn-off loss does not dominate the switch losses, the improvement is not as evident as compared to the double-pulse tests.
8) An important loss mechanism of the GS66516T device is the reverse conduction loss during the dead-time interval due to a large reverse conduction voltage drop. This property can be mitigated with anti-parallel SiC Schottky diodes (Wolfspeed C3D10065E) with small junction capacitance. It is shown that such an addition can further reduce the switch losses and improves the system efficiency, as seen in Fig. 21 (a), (c) and (e). This result is obtained since the SiC Schottky diode results in a 60-70% smaller forward voltage across M_1 and M_2 during reverse conduction. It also removes the otherwise substantial dead-time conduction losses away from M_1 and M_2.
9) It is noted that VF-CSS distributes the already smaller switch losses between both M_1 and M_2 enabling even higher F_{sw}. On the other hand, HSW concentrates the losses in M_1 (for positive output currents), that further limits its performance.
10) Besides the non-isolated DC/DC converter, the VF-CSS can also be applied in the isolated topologies. The application of VF-CSS in dual-active half-bridge converter is

illustrated to generalize the proposed controlling method. A dual-active half-bridge (DAHB) converter can be controlled with the VF-CSS method to achieve the ZVS. The switching signals and inductor current are shown in Fig. 18. (S_1, S_2) and (S_3, S_4) are the upper and lower switches in the primary and secondary side of the DAHB converter, respectively. The phase shift angle between the primary and secondary side is α. So, four turn-on switching combinations, (S_1, S_4), (S_1, S_3), (S_2, S_3), (S_2, S_4), can generate four different sections of inductor current in each switching period. To guarantee the critical soft-switching, two key turning points in Fig. 18 have been circled. The first turning point is the transient between the switching combinations of (S_2, S_4) and (S_1, S_4). To guarantee the soft-switching turn-on of S_1, the inductor current should be negative to fully charge the drain-source capacitor before it is turned on. Similarly, the second circled turning point is the transient between the switching combinations of (S_1, S_3) and (S_2, S_3). The inductor current should be positive to guarantee soft-switching turn-on of S_2. So, to apply the VF-CSS in the dual-active half-bridge, the ripple current between the two turning points, Δi_{CSS}, should be large enough to make sure one is positive and the other one is negative. In this case, the frequency can be controlled to enlarge the Δi_{CSS} as a constant value to achieve the critical soft-switching:

$$\Delta I_{CSS} = \frac{(V_{in} + V_o/n)\alpha}{LF_{sw}} \tag{18}$$

11) The power density of VF-CSS is 2.7 times larger than the hard switching method. A large current ripple is introduced to achieve the critical soft switching operation to reduce the power loss. In the meantime, the inductor value is reduced by a factor of 10. The volume of converter board, GS66516T-EVBDB is 43.8 in^3. A 10 μH Coilcraft inductor, SER2915H-103KL is only 0.442 in^3, 1.06 oz. However, for the traditional hard switching operation, a 125 μH chassis mounted inductor, 196B50, from Hammond Manufacturing is 75.9 in^3, 464 oz. The inductor volume difference will cause the power density to be increased from 8.35W/in^3 to 22.6W/in^3.

The loss components are shown in Fig. 22 for VF-CSS system without anti-parallel SiC Schottky diodes (Fig. 22 (a) and (b)), VF-CSS system with anti-parallel SiC Schottky diodes (Fig. 22 (c) and (d)) and HSW (Fig. 22 (e) and (f)). The 1kW HSW operation point Fig. 22 (f) is infeasible and obtained through extrapolation assuming a linear variation of the turn-on losses with V_{DS}/I_{DS}.

The dominant losses of HSW are located in the device M_1. VF-CSS removes a significant amount of the losses from the semiconductor devices and the dominant losses result in the (non-optimized off-the-shelf) inductor. The remaining switch losses are dominated by the reverse conduction losses during the dead-times since the GS66516T has a high reverse conduction voltage drop as shown in Fig. 22(a) and Fig. 22(b). The addition of an anti-parallel SiC diodes with the FETs reduces the switch losses by 60% to 70% as shown in Fig. 22(c) and Fig. 22(d). These losses can be further optimized by adjusting

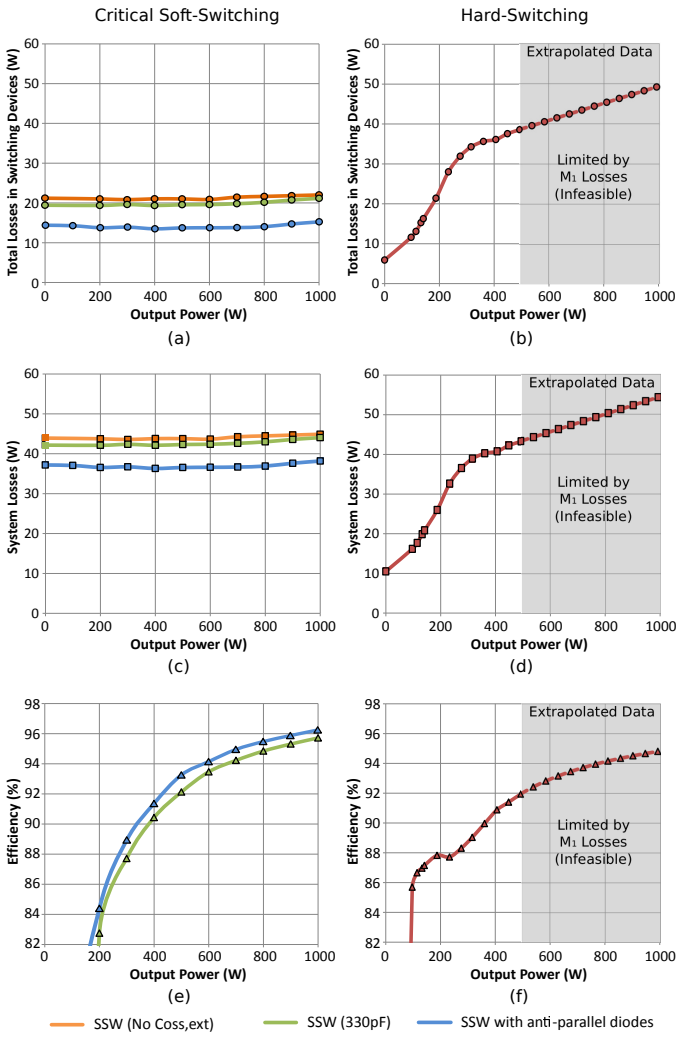

Fig. 21. Losses and efficiency in a buck converter at 1MHz switching frequency with linear soft-switching and hard-switching.

the dead-time values as a function of the operating points. We conclude that VF-CSS reduces the losses in M_1 by nearly 5 times compared to HSW at 500 W P_{out}. Hence, VF-CSS enables an increase in the switching frequency by the same ratio or an increase of efficiency.

Fig. 23(b) shows the steady state thermal image with forced air cooling at 27^oC ambient for the top-view of the VF-CSS buck converter of Fig. 23(a) using 2.1 μH inductor. The inductors reach a maximum temperature of 78.4^oC due to the large losses. The heat sink with the FETs is at 35.1^oC. Considering the half-bridge module, input/output capacitors and inductors which form the buck converter unit, the power density is 7.8 kW/L that exceeds the DoE target of 4.6kW/L for 2025 [2]. The HSW buck converter of Fig. 23(c) requires approximately 10 times the inductance value and results in similar losses at half the output power P_{out}. The HSW output power can be increased by decreasing the switching frequency, i.e. reducing the switching losses. However, decreasing the switching frequency requires an anti-proportional increase of the inductance, i.e. volume, to retain a constant ΔI_L.

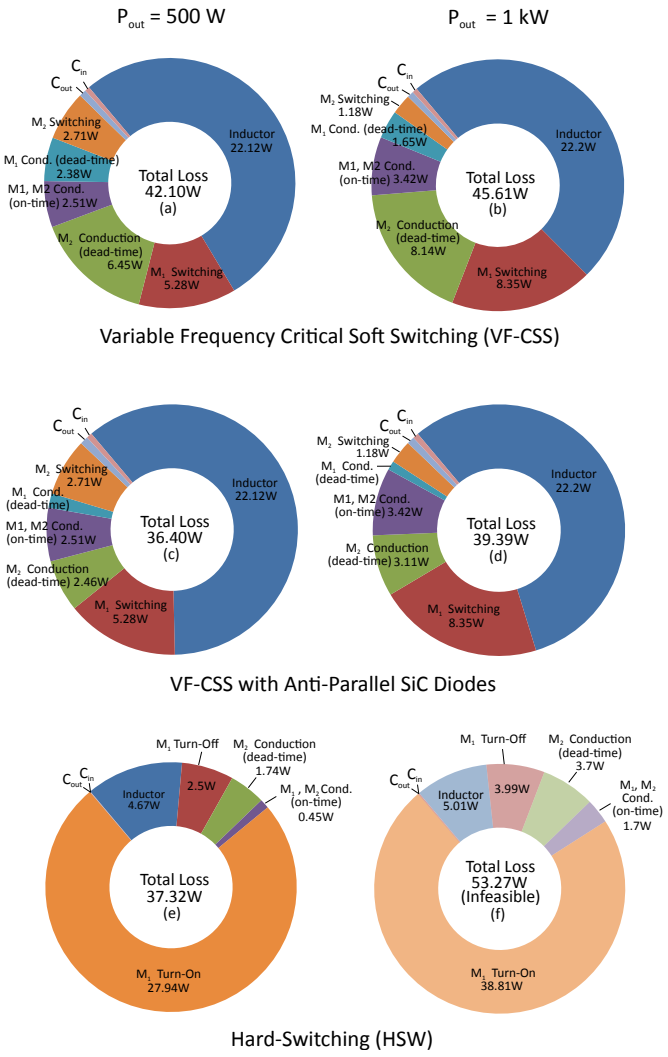

Fig. 22. Power loss estimation using analytical calculations and models at 1 MHz switching frequency.

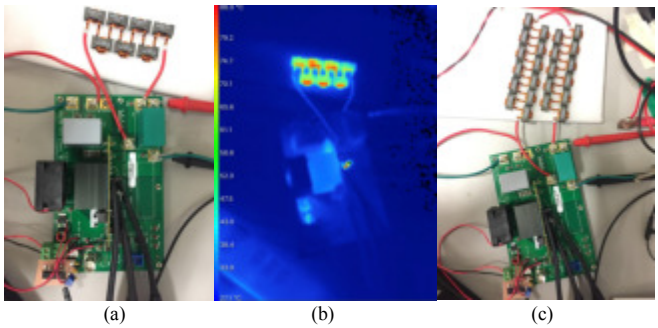

Fig. 23. (a) Top-view of the buck converter board using 2.1μH inductor and the VF-CSS method (b) Thermal image for operation of the top system at 1 kW with forced air cooling at 27^oC (c) Top-view of buck converter using 20.7μH inductor and hard-switching. Its steady-state thermal image is not captured to avoid system failure due to large switch losses and the resultant heating.

VI. Conclusion

This paper proposes a Variable Frequency Critical Soft-Switching control method to extend the switching frequencies of wide bandgap power converters to the MHz range. An analytical model of the device turn-off losses was proposed and validated for the GaN System GS66516T FET experimentally. The boundary conditions for critical soft switching are derived for the VF-CSS. The inductor has been largely reduced with the help of variable freqeuncy control under zero voltage soft switching operation. The reduced switching losses were leveraged to realize a buck converter with a 1 MHz switching frequency and 1 kW output power. This converter design achieves a 7.8 kW/L power density with forced air cooling that exceeds the DoE target of 4.6kW/L for 2025. A comparison with the traditional hard-switched buck converter indicates a potential to use a 5 times higher switching frequency while staying within the device power dissipation limits with the same cooling system design. Furthermore, we show that the addition of anti-parallel SiC diodes reduce the device losses, specifically the reverse conduction losses, further. Considering the significant margin between the operating current and the FET rating, losses in the switches and the relative insensitivity of the inductor losses to its average current, the present system can be extended for operation at output power greater than 1 kW and achieve an even higher power density. In future work, a custom inductor design will be implemented to decrease the inductor AC losses and improve the overall power converter efficiency. Furthermore, the switching concept can be applied to a range of power converters that consist of half-bridges and require filtering, e.g. grid connected inverters.

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