Analysis and Design of a High Efficiency, High Power Density Three-Phase Silicon Carbide Inverter

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***Abstract*—This paper discusses a design methodology for high power density converter design. The ideas are applicable to any topology and any switching technology. Particular attention is paid to the DC-link capacitors, as they are a regular point of failure and take up a sizeable portion of the volume in converters. In moving to wide-bandgap devices, smaller and more reliable film capacitors can be used by switching faster, thereby increasing the power density. A prototype inverter capable of switching 30kW is built using the discussed ideas and low power experiments show good correlation between the estimated and measured efficiency. A power density of 34kW/L is achieved under rated conditions when switching at 100kHz.**

I. Introduction

Wide-bandgap semiconductors, particularly Silicon Carbide, have been garnering increasing interest for power electronic applications as they continue to mature in the marketplace. Their inherently superior properties give them an advantage over Silicon semiconductor devices in terms of switching and conduction losses, as well as thermal conductivity, opening up the opportunity for more efficient and more compact systems that switch more power more efficiently.

In the automotive industry, regulatory mandates are becoming increasingly stringent, with fuel economy needing to be increased to be able to sell vehicles. Electrification, to any degree, is capable of increasing the overall efficiency of the powertrain and is seen as a key part of fuel economy gains as internal combustion engines reach their limits [1].

By employing wide-bandgap materials, these gains can be amplified. An example is [2], where the authors retrofitted simulation models of hybrid electric vehicles (HEVs) and plug-in hybrid electric vehicles (PHEVs), originally built with Silicon inverters, with Silicon Carbide JFET inverters. The results showed a substantial increase in powertrain efficiency, increasing the fuel economy and opening up the opportunity to optimize other aspects of the system.

Other authors have taken more general approaches to their work, where they have done device characterization to create scalable models and to quantify the benefits that can be seen by switching to wide-bandgap technologies [3]–[5]. Results are unanimously positive.

Others still have designed DC-DC [6]–[8] and DC-AC [9]–[12] converters to show that the benefits seen in characterization studies are mirrored in real applications. Once again, the results are positive, exhibiting that many applications stand to benefit from wide-bandgap semiconductor technologies.

Publications using Silicon Carbide devices are not new. The focus of the studies, however, differs. In [9], a forced-air cooled 10kW automotive-rated inverter was built. Others have sought to drive up power density, such as [10] and [11]. In [10], a 10kW forced-air cooled inverter achieved a power density of 20 kW/L; in [11], another 10kW inverter with a power density of 40kW/L was presented, though it did not integrate sensors, gate drivers or a controller. In [12], Silicon Carbide modules are used to design an inverter system for railway applications.

From this review of the available literature, it has been observed that publications tend to focus on the benefits to be reaped, in terms of efficiencies and possible size reductions, from employing wide-bandgap semiconductor materials. This work seeks to differentiate itself by focusing on maximizing the power density of a three-phase inverter by using Silicon Carbide devices. The methodology of a highly power dense design is discussed in general terms, allowing for it to be applied across a broad range of applications. Optimization techniques are not explicitly employed, though the notion of optimality is used for the selection of each component. The design procedure does not preclude the use of non-wide-bandgap devices, though certain focuses may need to be shifted to account for the change in device performance.

To that end, the layout of the paper is as follows: section II delves in to the theoretical analysis behind the inverter and its constituent components; section III applies these theories to the component selection and end design of the inverter; section IV presents low power experimental results when connected to an electric machine; and section V summarizes the findings.

II. Analysis

The effective design of a power electronic converter requires an individual treatment of each constituent component, followed by the synthesis into a whole system. These analyses can be as deep as desired: for example, modeling down to the semiconductor level or keeping with manufactured-provided datasheet values, in the case of a transistor.

In this paper, the analysis is kept simple so as to enable more rapid data processing and to provide a more general and scalable approach.

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A. Switches

The switching loss model employed is rather straightforward and has been used in papers before–such as [6] and [7]–with validity for a linear approach in loss estimation being given by [5] and, to a lesser extent, in [4].

A higher accuracy model could be used for switching energy loss calculations, with contributions from [13], for determining the rise and fall times; however, the non-flat plateau region in the $V_{GS} - Q_G$ curve of some–but not all–Silicon Carbide devices and modules complicates matters. The results in literature indicate a linear model based on datasheet parameters should be sufficient for a first-pass loss calculation. Once a series of component choices have been made, a more in-depth characterization may follow for design optimization.

The linear model assumption is that the switching energy losses are proportional to the current and voltage applied. That is to say,

$$E^* = E\left(\frac{V_{DC}}{V_{datasheet}}\right)\left(\frac{I_{Q,avg}}{I_{datasheet}}\right) \tag{1}$$

where E is the switching energy (on, off, reverse recovery or total); V_{DC} is the DC bus voltage; $I_{Q,avg}$ is the average current seen by the MOSFET; and $V_{datasheet}$ and $I_{datasheet}$ are the the voltage and current, respectively, at which the switching energy was measured by the device manufacturer, as stated in the datasheet. The reverse recovery energy, while not small enough to be negligible, is significantly smaller when compared to Silicon diodes and, for this paper, is assumed to be zero. The power loss from switching is the product of the energy and the switching frequency, $P_{switch} = E^* f_s$.

For MOSFET devices, the basic model of a resistance when on and an open circuit when off is used. Thus, $P_{MOSFET} = R_{DS(ON)} I^2_{FET,RMS}$, where $R_{DS(ON)}$ is the on-state resistance of the MOSFET and $I_{FET,RMS}$ is the RMS value of the current passing through the MOSFET.

The other loss-generating component within a standard MOSFET is the parasitic body diode, which is also normally used as the freewheeling diode. Again, using a simplified model, the power loss is the product of the average diode current, $I_{D,avg}$, and the forward voltage, V_F, expressed as $P_{diode} = I_{D,avg} V_F$.

B. Capacitors

The DC-link capacitor is an essential part of any power electronic converter. It acts as an energy storage element, thereby reducing the voltage fluctuation over an interval; it acts as a means of sinking ripple current generated by switching operations; and it provides a low impedance return for high frequency noise, which helps to reduce radiated electromagnetic emissions. Clearly, it is an important component.

Unfortunately, DC-link capacitor banks are often bulky and expensive, with volume, weight and cost being estimated at approximately 35%, 23% and 23%, respectively, of an automotive inverter [14]. Making an optimal–or even pseudo-optimal–selection for the DC-link capacitors populating the bank becomes an attractive proposition for minimizing these three impacts.

For most optimally building the DC-link capacitor bank, it is essential to understand what the requirements of the system are and how they may be met. In the case of an inverter, it services two key purposes: stabilizing the voltage and sinking ripple current. The third previously mentioned function–providing a low impedance path for meeting EMI requirements–is secondary in this analysis, though no less important in the overall integration of the system. The voltage ripple on the DC-side of an inverter can be estimated as [15],

$$C_{min} = \frac{I_{\phi,RMS}}{4\Delta V_{DC\%} V_{DC} f_s} \tag{2}$$

where V_{DC} is the DC-link voltage; $\Delta V_{DC\%}$ is the percent voltage ripple desired; $I_{\phi,RMS}$ is the phase output RMS current; and f_s is the switching frequency of the inverter.

Increasing the switching frequency becomes the most viable means of reducing the required capacitance for a given voltage ripple. Since the size of a capacitor approximately scales with the energy stored $\left(E = \frac{1}{2}CV^2\right)$, it can also be said that increasing the switching frequency will drive the volume down. Silicon Carbide devices are capable of operating at high power levels while still switching rapidly; thus, they are favourable for reducing the volume of the DC-link capacitor bank.

The ripple current through the capacitor which, coupled with the capacitor's internal resistance (ESR), cause power losses and drive a temperature rise, is more challenging to express. An approximation is given by (3) [16] and is valid for high power factor (i.e. permanent magnet) machines.

$$I_{C,RMS} \approx \frac{I_{\phi,RMS}}{\sqrt{2}} \tag{3}$$

C. PCB

Proper design of the printed circuit board (PCB) contributes significantly to reducing the parasitic inductance and ensuring transient voltage spikes remain below the maximum blocking voltage of the semiconductor devices. Detailed finite element analysis (FEA) can be performed to obtain a very accurate measurement of the inductance, thereby allowing for the design to be pushed closer to its operating limits; however, this can take a significant amount of time to not only run, but to model as well. Any minor change would result in a change in the impedance, resulting in a need to resimulate and reinterpret the results. An approach employing best practices is often sufficient for obtaining satisfactory performance.

A PCB can be thought of as a bus bar, albeit on a much smaller scale, as it is no more than layers of copper separated by an insulating material. By keeping forward and return current paths on opposing layers, flux cancellation can be maximized and the inductance reduced. Furthermore, by ensuring capacitors are placed close to components requiring transient power, loops can be minimized and the system's performance enhanced. Effective filtering can be used to shunt noise back to its source and reduce radiated emissions, as well as improving power quality.

D. Inverter

The objective of a voltage source inverter (VSI) is to generate a sinusoidal current by using a train of voltage square waves. In SPWM, the train emulates the behaviour of a sinusoid, with the fundamental having the shape of a sine wave. A sinusoidal reference, at the frequency of the desired fundamental frequency, is compared with a triangular carrier waveform with its period being the switching period.

Integral to assessing the efficiency of an inverter is a model that describes the current waveforms in the switch and the anti-parallel diode. To derive a simple, closed-form expression, two assumptions have to be made: the first is that the switching frequency is sufficiently high such that the output current waveform is a smooth sinusoid; and the second is that there is no delay nor deadtime during the switching operations.

Both of these assumptions will impact the waveforms and, consequently, the actual and estimated efficiency of the inverter. For the output phase voltage, the fundamental of the waveform will be reduced, as described in [17]. In an application where the load current is uncontrolled, this would mean a reduction in the RMS value of the current; however, in a traction application, currents and voltages are supplied to meet a demanded torque and speed. Hence, for a given load, the modulation index will need to be higher with added deadtime and rise/fall times than without.

From Kirchhoff's current law, the output current, $i(t)$, can be written as the sum of the currents entering and exiting the phase leg; i.e. $i(t) = i_p(t) - i_m(t)$, with $i_p(t)$ being the high-side current and $i_m(t)$ the low-side current, as exhibited in Figure 1.

The carrier waveform, directly related to the desired output sine wave, can be described as $m(t) = M\cos(\omega t)$, where M is the modulation index (the ratio of peak output to DC-link voltage). The output current waveform, then, would follow the reference waveform with a displacement angle, ϕ, resulting from the power factor of the load.

A duty cycle function, operating over the interval $[0, 1]$ can be defined as $d(t) = \frac{1}{2}\left(m(t) + 1\right)$, where over the interval $[0, \frac{1}{2}]$ the low-side switch and high-side diode are conducting and over $[\frac{1}{2}, 1]$ the high-side switch and low-side diode are conducting.

Instantaneous expressions for the high- and low-side currents can be calculated by multiplying the current waveform, $i(t) = I\cos(\omega t - \phi)$, with I being the peak current, by the duty function and applying the previous discussions. Employing the average and RMS value integrals, the currents through each switch and diode can be determined, per (4) and (5).

$$I_{S1} = \frac{1}{2\pi}\left(\int_{-\frac{\pi}{2}+\phi}^{\frac{\pi}{2}+\phi}\left(d(t)I\cos(\omega t - \phi)\right)^{j} d(\omega t)\right)^{\frac{1}{j}} \tag{4}$$

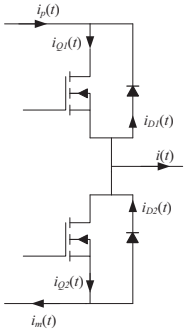


Fig. 1: Single phase leg analysis of a three-phase inverter.

$$I_{D1} = \frac{1}{2\pi}\left(\int_{\frac{\pi}{2}+\phi}^{\frac{3\pi}{2}+\phi}\left(-d(t)I\cos(\omega t - \phi)\right)^{j} d(\omega t)\right)^{\frac{1}{j}} \tag{5}$$

In both expressions, j dictates whether the integral calculates average current ($j = 1$) or RMS current ($j = 2$). Following from sine wave symmetry and the second assumption, the average and RMS values of both transistors and both diodes in the phase leg will be equal.

The final step in an efficiency analysis is to determine the output power. The apparent power of a three phase inverter driven by SPWM can be written as (6),

$$S_{3\phi} = \frac{\sqrt{3}}{\sqrt{2}} V_{DC} I_{\phi,RMS} M \tag{6}$$

The real component, the output power, P, is simply the apparent power, S, multiplied by $\cos(\phi)$, where ϕ is the displacement angle between the voltage and current waveforms.

III. System Design

For the system design, the goal was to drive the power density as high as possible by reducing the volume. One key means to achieve this is not to just focus on the volume of each individual component; rather, to effectively maximize the volumetric efficiency of a rectangular enclosure, the height of every component should be identical, or as close to identical as possible. This is a key point in the system's design. In emphasizing such considerations, a sort of harmony between components may be achieved, resulting in system-benefiting synergies.

Key system specifications are listed in Table I.

A. Switches

Component selection is a mandatory part of any design. Since there exist numerous Silicon Carbide devices, a decision must be made for which one to use. The quickest, and easiest, way to do so is to use datasheet parameters to perform a first-pass loss analysis of each device and compare the theoretical efficiencies. All datasheet values are taken at elevated junction temperature, as this is a more likely operating condition to be encountered in-system.

TABLE I: System specifications

Requirement	Value
DC-link voltage	$800V$
Load current	$30A_{RMS}$
Switching frequency	$100kHz$

TABLE II: Key device parameters.

Part	$E_{on}(mJ)$	$E_{off}(mJ)$	$R_{DS}(m\Omega)$	V_F
C2M0025120D	1.4	0.3	43	3.3
SCT2080KE	0.174	0.051	125	4.6
GA20SICP12-247	0.028	0.328	93	3
SCT30N120	0.5	0.4	90	3.5

Fundamental to the analysis of the MOSFETs is the application of equations (4) and (5). From these, the losses, both energy and conduction, can be obtained for each component using (1) and the basic device expressions. Then, the efficiency can be calculated as the ratio of output power to input power.

The results of voltage, current and modulation index sweeps are shown in Figure 2, with the displacement angle equal to zero (unity power factor). The GeneSiC MOSFET, GA20SICP12-247, performs best at the rated specifications, with a slight edge over Cree's C2M0025120D. This results from the superior switching characteristics exhibited by the GeneSiC device. However, a compromise has been made by the manufacturer, with lower switching energies coming at the expense of a higher on-state resistance; consequently, at high currents, the device succumbs to Cree's MOSFET. The MOSFET parameters used for the calculations are listed in Table II.

Because of the overall minor difference in efficiency between the two under rated conditions, the Cree device was chosen for the final design of the inverter. While a simplified loss model may compromise overall estimated accuracy, it does provide a uniform means of comparing switches and, therefore, the best performing switch of the group will always be the best, regardless of model complexity.

B. Capacitors

The design of the DC-link capacitor bank relies entirely on the system specifications and constraints. If the DC bus voltage, switching frequency, output phase current and desired voltage ripple are known, then equations (2) and (3) can be applied to aid in determining the number of capacitors required.

The minimum number of capacitors needed is the multiplication of the number of series capacitors required to sustain the continuous DC-link voltage, as well as the transient $L\frac{di}{dt}$ spikes, and the number of parallel capacitors needed to safely sink the current ripple without overheating. If the voltage or current ripple specification is not met, more still will need to be added in parallel.

A sort of pseudo-optimization can be devised, similar to [18], where a database of commercially available capacitors can be used to build DC-link capacitor banks, of a single device type, that satisfy all design requirements. It is at this point where a multitude of approaches can be taken: build a cost function (or a series of cost functions) that capture the important data points and find the minimum value; construct a surface that represents the dataset and find the global minimum; apply the Pareto front to the original data or the cost function representation; or, simply, use a series of constraints to reduce a problem with N many possible solutions to a problem with n, where n is the number of capacitor banks remaining after the constraining operation. In the last case, the final decision would be made by engineering intuition, component availability, etc. by the designer. The final procedure described is the one employed in this paper.

With the overarching goal of this work being to maximize the power density, the most significant constraint is placed on the volume of the DC-link capacitor banks being swept, while also paying close attention to the height of the capacitors for efficient volume utilization.

The constraining operation reduces the selection from 1750 capacitors to only 42. Further constraints and considerations with proposed board layouts led to the selection of the capacitor within the red circle in Figure 3 (b). The proposed DC-link capacitor bank is comprised of 10 of Vishay's MKP1848C series film capacitors.

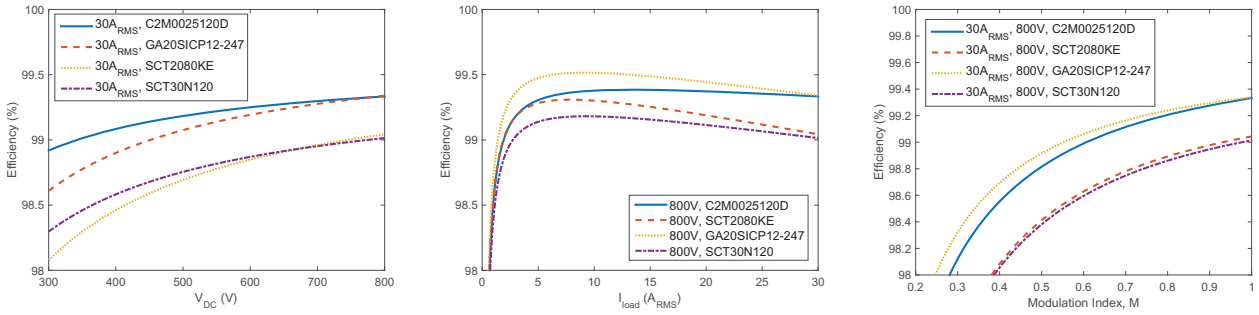
C. PCB

The design of the PCB is wholly dependent upon the design specifications. With a DC bus voltage of 800V and switches rated to 1200V, the board should be designed to withstand peak voltages of 1200V. The PCB has been designed to IPC-2221 standards with low inductance and a small profile. The length and width of the board were designed to fit the components and the intended cooling solution as tightly as possible. The thickness, however, relies upon the insulating materials and the voltage potential between layers. Conductor spacing is maintained at IPC-2221 recommendations, with 6mm on the external layers and more than 2mm on internal layers.

A typical PCB stackup for four layers is presented in Figure 4. The minimum required thickness of each layer is dependent upon the potential difference between layers and the dielectric strength of the materials used. Knowing these, the necessary thickness of the materials separating the conducting material can be calculated. Typical figures for the dielectric strength of the core material (normally FR-4) and the prepreg (epoxy resin) are 40kV/mm. Applying voltage stresses in excess of the breakdown field strength will result in board failure.

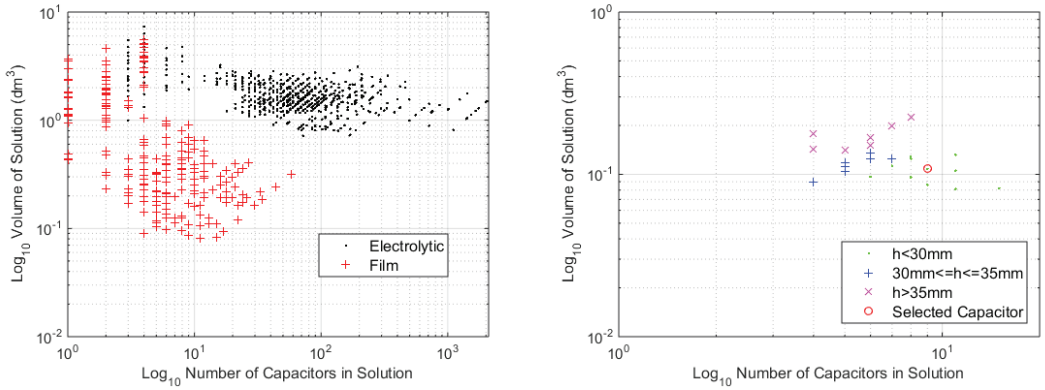
An interesting thing to note from Figure 4 is that copper traces cut in to the thickness of the prepreg layer, requiring extra attentiveness with respect to the minimum thickness to avoid breakdown. With the height of one ounce of copper being $35\mu m$, the impact of conducting layers can be taken in to account rather easily by checking if the difference between t_{pre} and t_{cu} is greater than the minimum thickness to prevent breakdown.

Auxiliary concerns that may arise from high voltage PCB design are whether the prescribed PCB thickness is manufac-



(a) DC-link voltage sweep, $M = 1$. (b) Load RMS phase current sweep, $M = 1$. (c) Modulation index sweep.

Fig. 2: MOSFET efficiency maps with a switching frequency of 100kHz and unity power factor.



(a) Total data set being operated on. (b) Result of constrain-and-filter operations.

Fig. 3: Log-Log plots of DC-link capacitors.

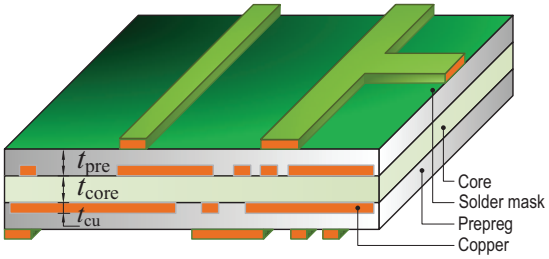


Fig. 4: Prototypical four-layer PCB stackup.

turable by a preferred vendor and whether the contacts of any through-hole components are long enough to be soldered on the opposite side of the board.

IV. Experiments

To test the inverter's functionality and to validate the efficiency obtained from the simplified analysis, it has been connected to electric machines acting as loads. The setup is shown in Figure 5, with a PMSM being the driving machine (right) that is directly connected to the inverter, an induction machine (left) as the load machine and a dSpace MicroAutoBox as the controller. Machine ratings meant that the currents involved with the testing were low.

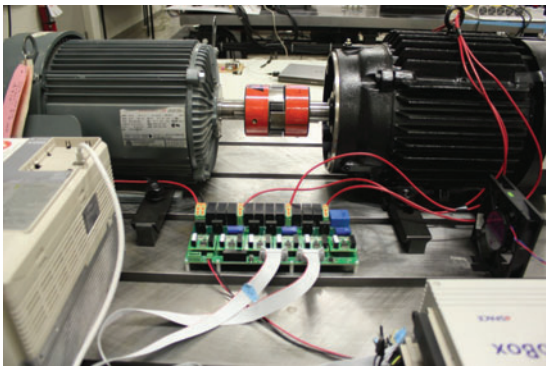


Fig. 5: The inverter testbench.

Measuring the efficiency of the inverter is a challenge, as the RMS voltage applied is not easily calculated from the PWM switching waveform. To bypass this, a power analyzer is used to calculate the power, which is obtained by measuring the three-phase currents and the line-line voltages.

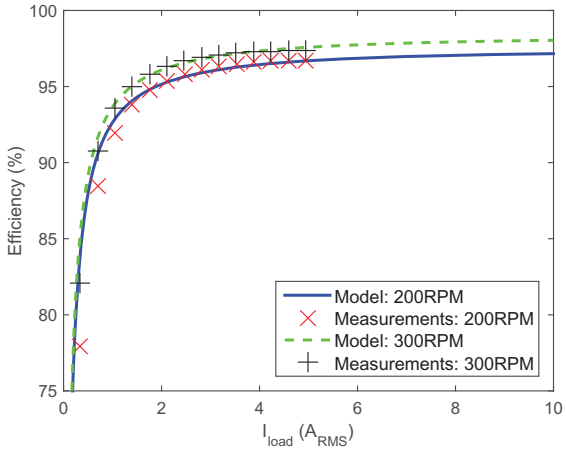


Fig. 6: Low power comparison between model and measurements at a DC-link voltage of 300V.

Complicating the comparison between the employed model and the measured results are several factors. The first is voltage regulation from the DC supply: As loading increases, the DC-link voltage decreases due to losses in the conversion chain, which requires the controller to compensate by increasing the modulation index to maintain constant speed. The second issue is the non-constant power factor, with a higher value being observed at lower currents and vice-versa at higher currents. Both of these obstacles are overcome with the use of an electric machine model to estimate an average power factor and modulation index over the loading spectrum.

The measured efficiency at light load is compared with the simplified model in Figure 6. The two show good correlation under test cases at different speeds.

V. Conclusion

This paper presented the design of a three-phase inverter using some of the most advanced discrete Silicon Carbide devices on the market. A strong emphasis was placed on the design of the system as a whole, where optimality was sought in each major component of the converter. The result was an inverter with an output power density of 34kW/L at a switching frequency of 100kHz with the implementation of a cooling system in the designated channel. Experimental results showed that, even under low load conditions and far from rated operation, the inverter achieved high efficiency and that the basic model provided a good approximation of the losses.

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