Three-Phase Inverter Design Using Wide-Bandgap Semiconductors to Achieve High Power Density

THREE-PHASE INVERTER DESIGN USING WIDE-BANDGAP SEMICONDUCTORS TO ACHIEVE HIGH POWER DENSITY

BY

WILLIAM MICHAEL EULL, B.Eng. & Mgmt.

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AUTHOR:	William Michael Eull B.Eng. & Mgmt. (Electrical Engineering) McMaster University, Hamilton, Canada
SUPERVISOR:	Dr. Ali Emadi
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To my family.

Abstract

Electric and more-electric vehicle proliferation continues unabated as government mandates worldwide demand fuel economies in excess of what conventional internal combustion engines are capable of. Vehicle electrification, to any degree, is perceived to be the means by which automotive companies may meet these targets. Electrification introduces a myriad of problems including cost, weight and reliability, all of which must be addressed in their own right. The rapid commercialisation of wide-bandgap semiconductor materials which, as a whole, exhibit properties superior to ubiquitous Silicon, provides the opportunity for power electronic converter minimisation and efficiency maximisation, easing the challenge of meeting current and incoming standards.

This thesis concerns itself with the design methodology of a highly power dense converter, as applied to a three-phase inverter. By using figures of merit, simple modelling techniques and novel discrete component selection tools, a well-designed converter is achieved that is capable of switching 30kW of electric power at 100kHz in a small package. Testing results show that the converter, with a simple forced air heatsinking solution, can effectively switch 15kW of power. Given the temperature rise of one phase leg of the inverter relative to the others, a superior heatsink design would allow the inverter to reach its rated power levels.

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Chapter 1

Introduction

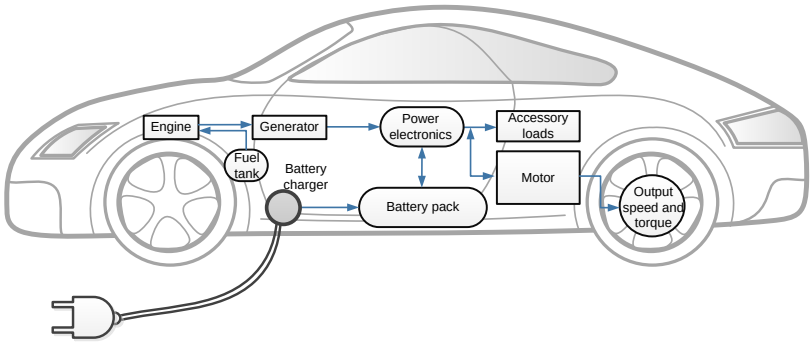
With transportation alone contributing to a third of green house gas emissions in the United States, a paradigm shift is required to slow the onset and minimise the impact of climate change. Governments worldwide are beginning to recognise the economic and societal impacts of air pollution and climate change and have been introducing stricter fuel economy mandates for new vehicles. These, in tandem with the general public's demand for more environmentally friendly transportation options, have been driving an increase in interest in electrified vehicles by automotive manufacturers (Bilgin *et al.*, 2015).

One of the most notable programs for mandated vehicle electrification is California's Zero Emission Vehicle (ZEV) program. Devised in 1990 and launched in 1998, the ZEV program mandates that a certain percentage of new car sales in the state must output no pollution when driving, encompassing fuel cell (FC) and battery-electric vehicles (BEVs). Other states have opted for similar programs following the successful launch in California (Alliance of Automobile Manufacturers, 2016).

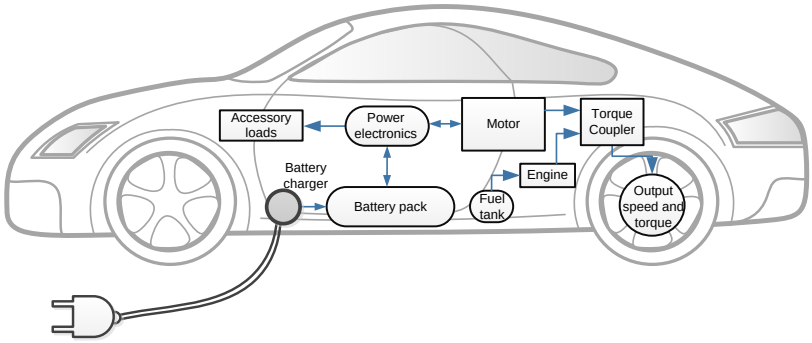
Another program launched by the United States Department of Energy is the

EV Everywhere Challenge, which is a collaborative project between manufacturers, national laboratories and the government to innovate in transportation electrification to obtain size and cost reductions. Targets are laid out for cost, power density and other key parameters in powertrain development in the coming years (Rogers, 2012). New developments and technologies are key to achieving these mandates and targets.

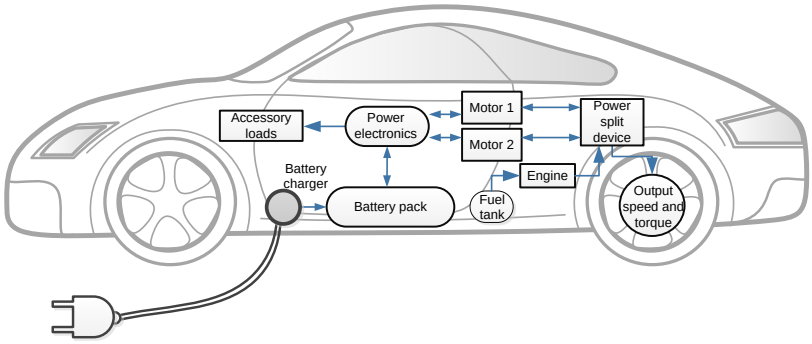
Three major electric vehicle architectures exist and are shown in Figures 1.1. Automotive manufacturers develop a powertrain based off of what architecture meshes best with their planned vehicle and load profiles. Vehicle types can be broken in to three major categories: hybrid electric (HEV), battery electric and fuel cell. Hybrids can be further subdivided depending on the level of hybridisation, with the lowest level being a start-stop configuration and the highest a plug-in hybrid vehicle, where the battery is the primary propulsion source and gasoline the secondary. More comprehensive illustrations of electrified vehicle architectures with many of the auxiliary loads shown can be found in (Emadi *et al.*, 2006).



(a) Series configuration.



(b) Parallel configuration.



(c) Compound configuration.

Figure 1.1: Electrified vehicle architectures, with battery charging circuit (Emadi, 2015).

A simplified power conversion chain in an electrified vehicle is presented in Figure 1.2. The battery does not connect to the motor directly for two reasons: the first is that a battery's output is DC and AC motors are better suited for vehicle applications; and the second is that a high voltage battery pack is expensive to build and manage charge balancing due to the need to create large series stacks to increase the voltage level. For these reasons, two converters interface between the battery and the electric motor: a DC/DC converter where current can flow to the motor and back to the battery, and an inverter to convert from DC to AC. The battery also connects to an auxiliary power module (APM) to bring the voltage level down to that which auxiliary loads demand. If the vehicle is a PHEV or BEV, then a battery charging circuit is required; if not, it is omitted.

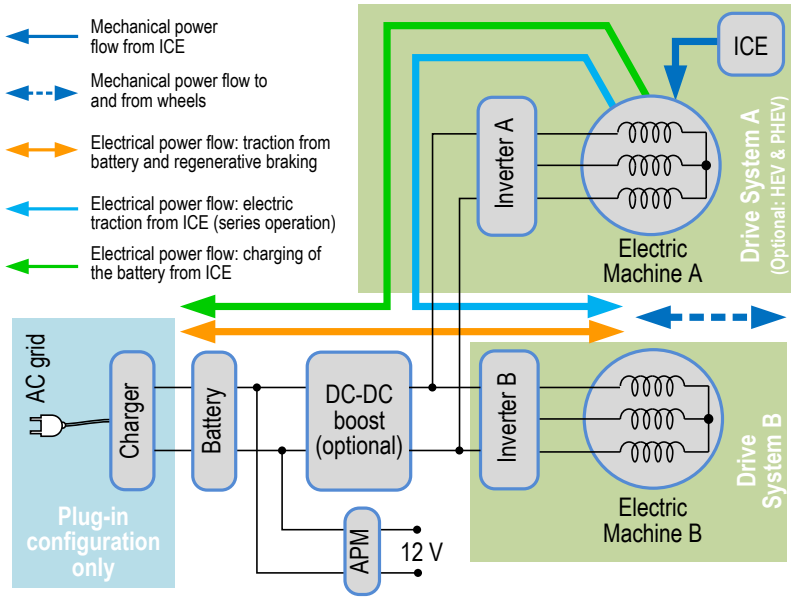


Figure 1.2: Electric power flow and conversion chain in an electrified vehicle (Bilgin *et al.*, 2015).

For illustration's sake, inverter A is assumed to not be active. The efficiency in the primary power conversion chain, from battery to motor, is the product of the efficiencies of the components in series and is calculated as (1.1). For a high chain efficiency, each individual item needs to have a high efficiency.

$$\eta_{drive} = \eta_{battery}\eta_{DC/DC}\eta_{invB}\eta_{motor} \tag{1.1}$$

It is here where the benefits of novel technologies for power switches can be best observed. Silicon, the material underpinning the modern technological revolution and the majority of power converters presently, is approaching its limits and it takes innovations, such as Superjunction technology, to obtain ever higher performance. Wide-bandgap (WBG) materials, however, have intrinsic properties that are favourable to reducing power losses, making them capable of higher efficiency operation.

As outlined, there are three, four or more–depending on the vehicle's architecture (Emadi *et al.*, 2008)–major power converters in an electric vehicle. They all stand to benefit, in some form, from a shift to wide-bandgap materials. Due to differences in voltage and current levels, some materials are more likely to see use than others for a given converter.

The auxiliary power module (APM) steps down the battery voltage, high or low, to 12V, replacing the alternator for powering auxiliary loads. There exist many possible circuit topologies and control schemes for an APM (Hou *et al.*, 2015). Inductors or transformers, depending on whether isolation is desired, are required and can be made smaller by increasing the switching frequency. On the low voltage bus, the currents can be in the hundreds of Amperes, demanding switches with low conduction losses. Wide-bandgap devices can meet both of these needs..

The bidirectional boost converter steps up the voltage from the battery to levels that would generate a desired speed for the electric motor, as well stepping-down voltage during a regenerative braking operation to recharge the battery a small amount. There are several topologies, primarily related to the number of switches and inductors in the system. A phase can be defined as a conduction leg with two switches, for forward and reverse conduction. Topology variations can have one inductor per phase, a shared inductor between phases, or some variant thereof (Ye *et al.*, 2014a). Higher phase numbers are beneficial for reducing the volume of the required inductor, as well as the power losses in the switches. In one study, the benefits to be seen in terms of inductor and switch volume and losses were quantified, justifying a decision to move to a higher phase order (Magne *et al.*, 2015). Increasing the switching frequency can further reduce inductor volume, thereby driving upwards the power density of the converter. WBG semiconductor devices are capable of switching at a higher frequency than their Silicon counterparts with lower losses, providing a viable avenue to reduce the inductor volume and even the heatsink via reduced losses.

The inverter converts the stepped-up DC voltage to an AC voltage, which is used to drive the electric motor. Many inverter topologies exist, such as the Z-source (ZSI), current source (CSI), voltage source (VSI) and various multi-level inverters. These topologies can exist as a single three-phase inverter or several in parallel for supplying several loads. The ease by which a voltage source inverter may be implemented, as well as the reduction in the total number of components relative to other topologies, make it preferred for automotive applications (Ye *et al.*, 2012b). Cost considerations come in to play for these more component-heavy topologies, which spurred an investigation in to alternative, reduced-part dual inverters. The general findings were that for

a dual inverter, reliability and voltage utilisation issues make it difficult to justify a reduction in transistors (Ye *et al.*, 2012a). Outside of component count reduction, the other means by which the size of an inverter can be reduced is the DC capacitor bank, which is estimated to consume 35% and 23% of the volume and weight, respectively (Balachandran *et al.*, 2014), of a traction inverter. Fast switching devices reduce the capacitance required for a given voltage ripple level (Preindl and Bolognani, 2011), making them an attractive proposition.

The battery charger, the optional converter that depends on the degree of electrification of the vehicle, interfaces between the electrical grid and the battery in the vehicle. Most of the time, the battery charger steps-down and rectifies the AC voltage to a DC voltage; however, interest is growing in bidirectional topologies, also known as Vehicle-to-Grid (V2G), that allow an unused electric vehicle to supply energy to a load that accepts AC voltage as an input: a house, the power grid, etc. If the charger is on-board as opposed to off-board, then it becomes imperative to reduce its total in-system footprint. If the system is non-integrated, i.e. a separate charging circuit is added, then additional active and passive components are required, which add bulk to the vehicle (Yilmaz and Krein, 2012). WBG materials are favourable to reducing losses and the size of magnetic components. An additional benefit of the employment of WBG semiconductors is that, with a higher efficiency charging system, a battery can be charged faster and, therefore, has the potential to assist in electrified vehicle adoption. Furthermore, if the car is being used in V2G mode, where a bidirectional converter is absolutely necessary, a higher efficiency from the charging circuit would translate in to more energy supplied to the grid, which could assist in grid stability when demand is high.

From this overview of the typical major power converters within an electrified vehicle, two conclusions can be drawn: they need to be small and efficient; and that wide-bandgap materials have the potential to greatly aid in this endeavour. Over the years, many researchers have considered both the efficiency of the individual component and the efficiency of a system when using wide-bandgap transistors. They range in their goals, with some seeking to characterise a device and draw a conclusion and others showing the benefits to be reaped in a particular application.

Two studies that consider the first point are (Merkert *et al.*, 2014) and (Jahdi *et al.*, 2014). In both, the authors characterise conventional and Silicon Carbide transistors and make a comparison between the two. In the former, continuous functions for specific devices are built by fitting a curve to the experimentally obtained data and are used for a simulation of an inverter's efficiency. The results showed that an inverter built with Silicon Carbide JFETs performed better than one built with Silicon IGBTs. In the latter study, a Silicon Carbide MOSFET and diode were compared against a Silicon IGBT and diode under several different operating conditions: slew rate, temperature, voltage, current and gate resistance. These results were used for a three-phase inverter conversion efficiency simulation under different modulation schemes. The Silicon Carbide system obtained significantly higher efficiency under different modulation strategies. A third study mapped out the switching and conduction losses of even more switches to come to the same conclusion, although it was published several years earlier (Glaser *et al.*, 2011).

One study published, predating the first two, showed very clearly the gains to be obtained for an electrified vehicle by using Silicon Carbide devices (Zhang *et al.*, 2011) in the inverter stage. The authors experimentally obtained performance curves

for a Silicon Carbide JFET and Silicon IGBT for use in simulations of a HEV and PHEV model over a typical driving cycle. The end result was that, in both vehicle architectures, the overall system efficiencies were higher with Silicon Carbide. The resulting junction temperature estimation was low enough that the heatsink could be redesigned and made smaller for the JFET, yielding further synergies.

One drawback to the previous investigation is that it does not take advantage of the higher frequency operation that wide-bandgap semiconductors afford by switching only at 20kHz, nor their ability to operate at higher temperatures than Silicon. These are rectified in (Wrzecionko *et al.*, 2014), where a 10kW inverter operating in an environment with an ambient temperature of 120°C is designed and implemented. Silicon Carbide's maximum permissible junction temperature is higher than that of Silicon, making it favourable for such an application. Replacing a Silicon inverter with the designed one would allow for a reduction in the size and complexity of the heatsink and, consequently, increase the power density of the system.

Another study focused on three converters for automotive applications: one three-phase inverter and two DC-DC converters, one bidirectional and the other unidirectional. Using a sample of devices on the market and their ratings, a trend was created to scale devices from one power level to another via die size modifications, with this information being used to develop loss models of the three converters. Under these conditions, all-Silicon Carbide devices offered superior performance to Silicon MOSFETs, IGBTs and even hybrid Silicon IGBTs, which fuse an IGBT with a Silicon Carbide diode to reduce the reverse recovery losses of the diode when switching. Silicon Carbide MOSFETs were also shown to meet rather handily the demands of the autmotive industry (Biela *et al.*, 2011).

Shifting focus entirely to DC-DC converters, a paper published considered an on-board battery charger for an electric vehicle using Silicon Carbide MOSFETs. The topology consists of a boosting rectifier and an isolated step-down converter with a high level of integration and custom-made MOSFET modules. The end result was an on-board charging system outputting just under double the United States Department of Energy's 2022 target, as well as having a power density and specific power five and four times, respectively, larger than the target. No direct comparison is made between Silicon and Silicon Carbide devices, though it can be assumed that the 2010 Prius PHEV that is used as a benchmark did not use WBG materials. In this case, the designed charger achieves much better performance (Whitaker *et al.*, 2014).

The application of wide-bandgap semiconductors is not exclusive to automotive applications. In (Alkayal and Saada, 2013), the researchers designed a three-phase inverter using Silicon Carbide MOSFET modules for an electric train. The main result of the study was that the same techniques for designing a Silicon-based inverter applied to a Silicon Carbide inverter. They also showed that the optimal switching frequency for a Silicon Carbide inverter was higher than that of Silicon, when taking in to account mass, volume and cost of the system. This includes the heatsink and an AC-side filter, which requires inductors and capacitors.

Nor are wide-bandgap materials exclusive to transportation. For photovoltaic applications, the conversion efficiency from panel to grid is of great importance, in no small part due to the fact that solar cells convert a fraction of the energy they receive from the sun. The importance of wide-bandgap materials for these applications was espoused in (Rodriguez *et al.*, 2013) and (Garcia-Rodriguez *et al.*, 2014), with the former considering Silicon Carbide and the latter Gallium Nitride. In both studies,

the efficiency of the wide-bandgap devices are compared with comparable Silicon ones. The results showed clear gains by transitioning to WBG transistors.

An interesting study is undertaken in (Gurpinar and Castellazzi, 2016), where a single-phase T-type inverter is designed using three different switches: a Silicon IGBT, a Silicon Carbide MOSFET and a Gallium Nitride MOSFET. Analysis shows that the GaN FET achieves higher efficiency over temperature, power and switching frequency. This translated in to an estimated reduction in the heat sink size, relative to Silicon Carbide, of almost four times, as well as a lower loss for a given output filter volume, in no small part due to the higher switching frequencies that can be obtained at a lower power loss. The key takeaway is that Silicon Carbide is not the only solution when designing-in wide-bandgap semiconductors and, indeed, niches may exist.

Take, for example, a presentation given by Yole Développement at the Applied Power Electronics Conference (APEC) in 2015 pertaining to market trends in the semiconductor industry. Their statement, concurred with by semiconductor manufacturers, is that different materials will dominate different voltage levels and price points. At the moment, Silicon Carbide and Gallium Nitride are cutting in to high-end, performance applications; however, as their cost comes down, they are expected to further erode Silicon's position. Gallium Nitride is expected to be used in ultra-high frequency applications below 100V and in general converters up to about 600V before Silicon Carbide dominates in higher voltage levels (Gueguen, 2015).

Two papers published using Gallium Nitride hit home its versatility in voltage levels, which is yet to be seen in Silicon Carbide publications where they have so far been used at higher voltage levels. In the first study, Gallium Nitride High Electron

Mobility Transistors (HEMTs) are used for a 48 to 12 Volt resonant step-down converter operating at 1.2MHz, delivering several hundred Watts of power. Analytical and experimental results, as well as a low voltage figure of merit (FOM) designed specifically for hard switched GaN devices, show that superior efficiency and performance can be achieved (Reusch and Strydom, 2015).

Similar work on a resonant converter, albeit at a DC bus voltage of 400V, is shown in (Huang *et al.*, 2014). A GaN HEMT is compared with a Silicon MOSFET switching at 1MHz to deliver several hundred watts on a 12V bus. The two share similar conduction losses; however, the switching losses are where the GaN device shines, with a significant reduction exhibited. The end efficiency is several percentage points higher, making it an attractive option for future designs.

In total, the consensus is that wide-bandgap semiconductors are beneficial to loss and system footprint reduction and are worthy of applied research. From this survey of literature, two gaps are observed, both of which are related to the power dense design of a converter: the first is in a simple, accurate and generalised process that does not rely on heavy levels of modelling and testing to preliminarily determine converter losses; and the second is in discrete component selection, where many studies simply state a component was chosen with no process outlined.

This thesis aims to alleviate these identified issues. In chapter 2, the basics of power semiconductor devices and materials are outlined. Intrinsic material properties show that wide-bandgap semiconductors have inherently great potential to benefit power electronic designs. Figures of merit, for both materials and switches, are presented. For the materials, the benefits to be reaped from moving to designs employing wide-bandgap semiconductors are definitively shown.

In chapter 3, a review of modelling techniques is undertaken and a decision is made on which to employ when evaluating the losses of a converter. A three-phase inverter is chosen as the targeted application and the means of evaluating the efficiency are presented. Optimality in component selection, a rarely discussed subject, is introduced, along with several possible approaches. The fundamentals of parasitic parameter analysis of a power transmission system are discussed and exemplified via finite element simulations on a realised bus bar.

Chapter 4 is focussed on the design of the converter, with an emphasis on component selection. The figures of merit for specific devices, introduced in chapter 2, are used to draw an initial conclusion regarding which transistor to use. Simplified analysis under equal operating conditions is used to determine exactly which transistor to design-in as the FOMs are not capable of delivering an exact answer. Novel techniques are used to select the DC-link capacitor, which are equally applicable to any other discrete component selection problem, given appropriate tuning is applied to the data pre-processing and algorithm. The basics of PCB design for a high voltage circuit are discussed and applied to design two versions of the prototype inverter.

Testing of the prototype inverter is presented in chapter 5. The Impedance measurements of a bare board and a populated board show that it is well-designed, exhibiting low parasitic inductance. The inverter is then tested in two configurations, with the first showing good correlation with the basic model at low power and the second showing the temperature of the cases when switching approximately 10.5kW of mechanical power, which translates to roughly 40% of the rated electrical power.

A summary of the work undertaken is given in chapter 6 and potential avenues of future research are outlined.

Chapter 2

Switching Devices & Comparative Analysis

2.1 Types of Devices

For electronics applications, there exist many different devices for controlling voltages and the flow of currents. In this section, only the major power switching devices and the basic diode will be discussed to provide the basic framework for moving forward with a comparison of different semiconducting materials and devices for an application.

2.1.1 Bipolar Junction Transistor

The Bipolar Junction Transistor (BJT), invented in the late 1940s, was the first power transistor to have been created and used for power electronic applications.

The most simplified, albeit not fully representative, model of a BJT is that of a

current-controlled switch: a current in the base determines how much current can exit the third terminal of the device. For an NPN BJT, current flows in to the base of the transistor, amplifying the current in the collector; in the case of a PNP BJT, current flows out of the base and determines the amplification in the emitter. The level of amplification is tied to the amplification factor, β, which is dependent upon the doping levels of a specific device. The basic schematic representation is given in Figure 2.1.

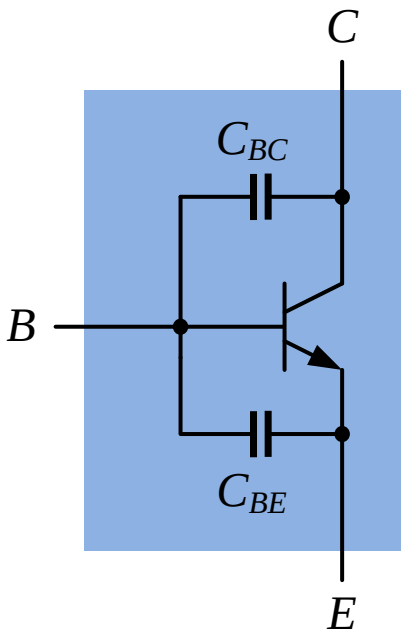


Figure 2.1: BJT schematic with parasitic capacitances.

A BJT has three operating modes: cutoff, saturation and active. These can be seen in Figure 2.2. The two modes of interest for a power switch are cutoff and active. Cutoff is achieved when no current is flowing in to or out of the base; active has several

conditions that have to be met, which will also determine the flow of current through the device. Coarsely speaking, if a current, i, is defined as positive when flowing from collector to emitter in an NPN BJT,

$$i = \begin{cases} > 0, & \text{if } v_C > v_B > v_E \\ < 0, & \text{if } v_C < v_B < v_E \end{cases} \tag{2.1}$$

where v_C, v_B and v_E are the voltages at the collector, base and emitter. For a PNP BJT, v_C and v_E would change positions in the inequalities.

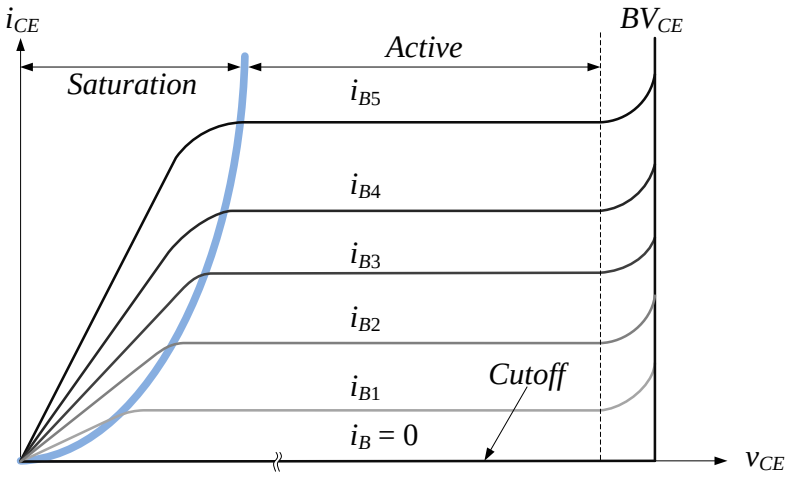


Figure 2.2: BJT current-voltage characteristic.

BJTs are minority carrier devices and, as a result, have significant tail currents when turning off due to the need to remove the charge carriers from the base. Moreover, power BJTs often have low current gains and require large base currents to turn on (Mohan *et al.*, 2003). These issues make them unfavourable for high frequency power switching applications due to the significant power losses that can be incurred.

BJT relevance is low in modern applications because of MOSFET advances and the introduction of IGBTs, which combine the attributes of a MOSFET and BJT for superior operating characteristics–including an elimination of the base current–and ease of use.

2.1.2 Metal-Oxide-Semiconductor Field-Effect Transistor

The Metal-Oxide-Semiconductor Field-Effect Transistor (MOSFET) is a voltage-controlled device where an applied voltage builds an electric field which, when sufficiently high, creates a region where electrons may move through, creating electric current flow. MOSFETs come in two varieties: n-channel (NMOS) and p-channel (PMOS). NMOS devices are preferred due to the higher mobility of the charge carriers, driving a reduction in the on-state resistance for a given die size.

A MOSFET, like a BJT, has three different operational regions: cutoff, triode (or Ohmic) and saturation. The most desirable region to operate in is saturation, particularly for power applications, as it permits a higher current flow with a lower resistance. The three regions are exhibited in Figure 2.3. With the saturation region being of primary interest, it will be the only one to receive discussion. The effects of channel length modulation are omitted.

For a laterally built MOSFET, the current carrying capability of the device in the saturation region can be described as,

$$i_D = \mu_n C_{ox} \left(\frac{W}{L}\right) (v_{GS} - V_{th})^2 \tag{2.2}$$

where μ_n is the electron mobility ($\frac{cm^2}{V \cdot s}$); C_{ox} is the capacitance of the Silicon dioxide insulation between gate and source and gate and drain; $\frac{W}{L}$ is the aspect ratio of the

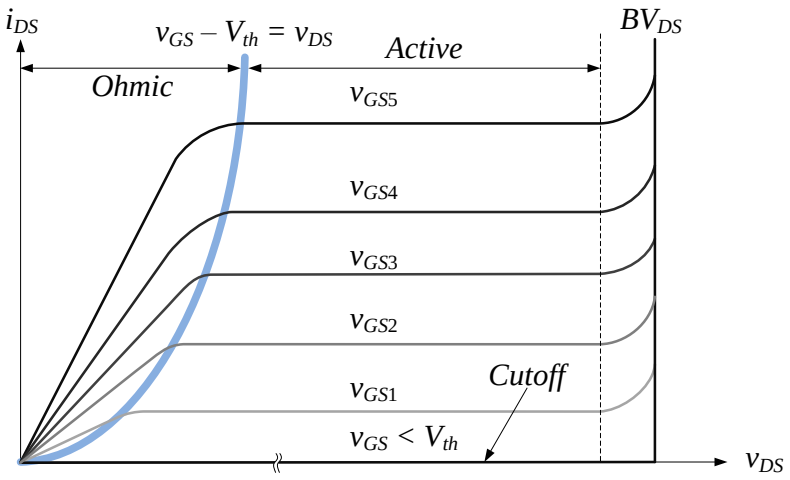


Figure 2.3: MOSFET current-voltage characteristic.

conduction channel, the ratio of the width, W, to the length, L; v_{GS} is the gate-source voltage applied to the MOSFET; and V_{th} is the threshold voltage of the device. The product of $(\mu_n C_{ox})\left(\frac{W}{L}\right)$ is the channel conductance, g_{DS}.

This expression is most commonly associated with low voltage MOSFETs for signal amplification purposes as, for power devices, to achieve a sufficient blocking voltage, the length, L, must be increased; however, increasing L drives the channel resistance upwards. There comes a point where the device becomes excessively large and lossy when building laterally. For this reason, power MOSFETs are typically built vertically and are referred to as Diffusion MOS (DMOS) transistors (Sedra and Smith, 2010). Superjunction MOSFETs, described in section 2.3.1, are built using a variation on DMOS techniques.

Despite not being universally applicable to MOSFETs, (2.2) helps with the basic

understanding of a MOSFET's performance. It is also helpful in explaining why Gallium Arsenide devices came to prominence in some applications, despite the bandgap and breakdown electric field strength not being substantially larger than what Silicon offers. A popular means of building Gallium Nitride MOSFETs, which has a much larger bandgap than both Gallium Arsenide and Silicon, is to do so laterally, permitting (2.2) to be employable.

The most basic interpretation of an NMOS is that, under a positive gate-source voltage exceeding the threshold voltage, it is on and under zero (or negative) gate-source voltage it is off. While it is a gross oversimplification, it covers the most important operating characteristics of a MOSFET for power applications. To operate in the saturation region, two conditions must be met:

$$v_{GS} \geq V_{th} \tag{2.3a}$$

$$v_{GS} - V_{th} \geq v_{DS} \tag{2.3b}$$

wherein v_{DS} is the drain-source voltage, which is the drain-source current, i_{DS}, multiplied with the on-state resistance, r_{DS}.

A schematic representation of a typical MOSFET with its parasitic capacitances is given in Figure 2.4. When switching a MOSFET, the parasitic capacitances contribute greatly to its performance. The two that contribute most significantly are C_{iss} and C_{rss}, which affect the current and voltage transition times, respectively. They are defined as,

$$C_{iss} = C_{GS} + C_{GD} \tag{2.4}$$

$$C_{rss} = C_{GD} \tag{2.5}$$

where C_{GD}, C_{GS} and C_{DS} are the gate-drain, gate-source and drain-source capacitances, respectively.

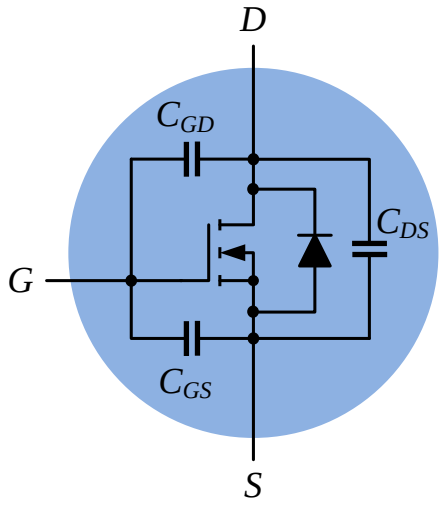


Figure 2.4: MOSFET schematic with parasitic capacitances.

Contributing to the overall energy losses of the MOSFET is the equivalent output capacitance, C_{oss}. It can be calculated as (2.6).

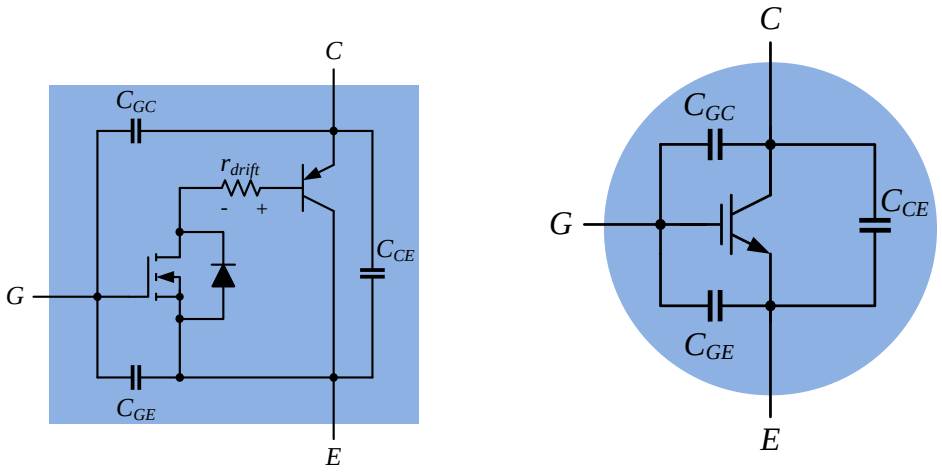
$$C_{oss} = C_{DS} + C_{GD} \tag{2.6}$$

Together, the capacitances and resistance fully describe a given MOSFET. Under specific operating conditions, the switching transition times can be approximated and, thusly, the losses.

MOSFETs find the most use in lower voltage, lower current, high frequency applications.

2.1.3 Insulated-Gate Bipolar Transistor

The Insulated-Gate Bipolar Transistor (IGBT) is the combination of both a MOSFET and BJT in a single semiconductor structure. An IGBT is built vertically in the same fashion as a DMOS with an additional p layer added, which gives rise to a pn junction that forms the BJT. Schematics of the device can be seen in Figure 2.5, where (a) is the more comprehensive–yet approximated–internal model of an IGBT and (b) is the most basic representation, where it is considered simply as a voltage-controlled device.



(a) The more complete IGBT model. (b) Simplified IGBT model.

Figure 2.5: Complex and basic IGBT schematics.

The IGBT is composed of two stages: a PNP BJT that conducts current and the

n-channel MOSFET that controls its base and, hence, the flow of current. When the gate of the NMOS is driven high and it turns on, the base of the PNP is permitted to conduct current from Base to Emitter, giving rise to a voltage, v_{BE}, that influences how much current flows from Collector to Emitter.

In reality, the top terminal of a PNP BJT is the Emitter and the bottom the Collector, which does not match the schematic representation of Figure 2.5; however, since it acts like an NPN BJT where it conducts with a positive applied voltage, the notation of Collector on top and Emitter on the bottom avoids confusion in practice. This discussion is relevant for an n-type IGBT. Its current-voltage characteristic is more or less equivalent to that of a MOSFET.

The IGBT, like the BJT, suffers from long tail currents when switching off due to its minority carrier structure. This makes it unfavourable for high frequency applications as the off-switching energy is high; however, the base current required to drive the device is eliminated, making it much better for use than a BJT. IGBTs find widespread use in high voltage, high current, low frequency converters.

2.1.4 Hybrid Silicon

Hybrid Silicon devices combine Silicon and Silicon Carbide components within the same package. This normally entails the use of a Silicon device as the switch, either a MOSFET or an IGBT, with the freewheeling diode being Silicon Carbide. However, since a MOSFET has a parasitic diode embedded in its structure, the benefits to be seen by paralleling a separate diode are more evident with respect to conduction and not switching. The total gains are more pronounced with IGBTs and, as a result,

the majority of commercially available hybrid Silicon devices are Silicon IGBTs co-packaged with Silicon Carbide diodes. This allows these hybrid transistors to mesh the superior current carrying characteristics of an IGBT with the reduced reverse recovery losses of a Silicon Carbide diode. This provides a strong benefit when considering high voltage, high current devices, as the reverse recovery energy is linked intrinsically to the junction capacitance of the diode which, itself, grows with the demanded blocking voltage.

A typical schematic for a hybrid IGBT is shown in Figure 2.6. The sole point of differentiation between a hybrid IGBT and a standard IGBT is the inclusion of a Silicon Carbide freewheeling diode.

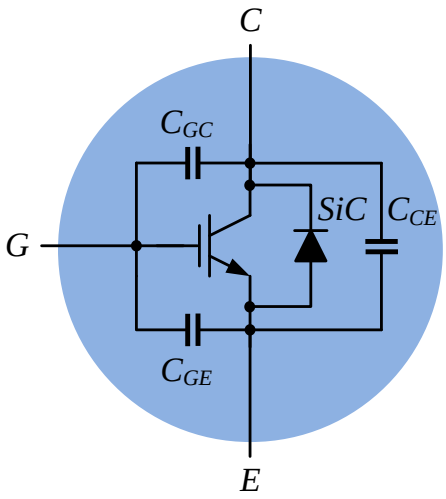


Figure 2.6: Hybrid IGBT schematic with parasitic capacitances.

Hybrid IGBTs find use in the same circuits that regular IGBTs do. The lower losses associated with the Silicon Carbide freewheeling diode can enable a reduction in heatsink size or an increase in the switching frequency of the converter.

2.1.5 Diodes

Diodes, in contrast to the other devices discussed so far, are two terminal semiconductors that only permit unidirectional current flow. BJTs, MOSFETs and IGBTs permit bidirectional flow by controlling whether the device is on or off via a third terminal, making them inherently more versatile.

The most basic model of a diode is a unipolar switch that turns on when the voltage applied to the anode is higher than the minimum voltage drop on the junction, V_F. When this condition is met, current flows from anode to cathode; if not, then no current may pass.

The current-voltage characteristic of a typical diode is shown in Figure 2.7. The forward voltage is non-linear and is a function of the current being passed by the device. Once a minimum voltage, V_j, is surpassed on the anode, current begins to flow from anode to cathode.

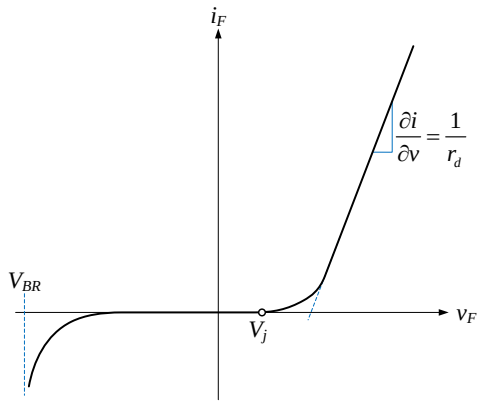


Figure 2.7: Current-voltage characteristic of a generic diode.

Diodes find widespread use in power converters, as they provide a path for energy stored in parasitic parameters and inductances to be dissipated. Without an

anti-parallel (or freewheeling) diode, the voltage would rise until the semiconductor device is forcibly short-circuited. Depending on the circuit topology and efficiency requirements, diodes can be replaced by tightly-controlled transistors acting in an identical manner.

2.2 Why Consider Wide-Bandgap Materials?

Wide-bandgap materials have many properties that are beneficial to power electronic applications. The larger bandgap itself gives rise to many of them: high temperature operation, radiation hardening, high blocking voltage and lower total power losses.

The simplest model of a semiconductor is that there exist three regions: the valence band, which is where the electrons rest until excited; the conduction band, which is where electric current begins to flow as the movement of electrons; and the bandgap, the region separating the two. As one would expect, as the bandgap grows larger, so, too, does the amount of energy required to excite electrons to jump from the valence to conduction band. This is the reason why wide-bandgap materials have some of their beneficial properties. In terms of radiation hardening, significantly more energy is required to force turn-on from an external source. For high temperature operation, more thermal energy is required to excite the electrons in the valence band sufficiently to make the transition. For the blocking voltage, a higher electric field is required to cause dielectric breakdown and force conduction. Together, these allow wide-bandgap materials to perform in harsher environments.

Related to the bandgap are the power losses of a device. As will be discussed in section 2.3.5, the internal capacitances and resistances of a MOSFET can be determined from the semiconducting material's properties. Wide-bandgap materials

allow for lower resistances and capacitances to be achieved for a given blocking voltage capability, thereby reducing the losses under all operating conditions. Reduced capacitances, in turn, allow for the switching frequency to be increased, driving a reduction in the size of certain passive components: capacitors, inductors and transformers. Several capacitors for power electronic applications are shown in Figure 2.8. Capacitor (b), were it rated for 800V, would likely be larger than (a); conversely, if capacitor (c) were to have a capacitance of 1000μF, it, too, would be large. In reducing the capacitance requirements for a given voltage ripple, the size of a converter can be decreased dramatically.

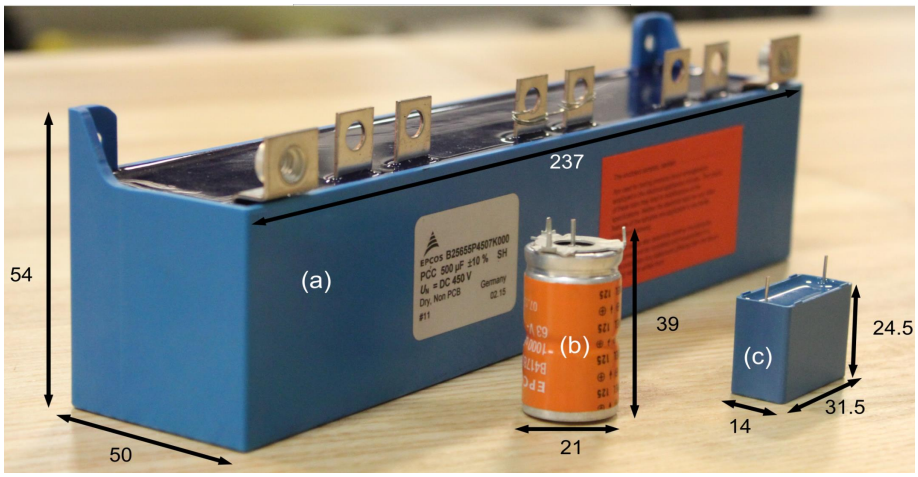


Figure 2.8: DC capacitors of different types, voltages and capacitances: (a) 400V, 500μF, film; (b) 63V, 1000μF, electrolytic; and (c) 800V, 5μF, film.

These, among other reasons (Gueguen, 2015), are why wide-bandgap materials are finding increasing usage in industry and academia.

2.3 Types of Semiconductor Materials

There are many possible semiconducting materials for electronics applications; however, only a few of them show good promise, as well as being commercially viable now or in the future, near or far. Properties key to electronics applications for these elements are provided in Table 2.1. An individual treatment of each material follows in the proceeding sections.

Table 2.1: Semiconductor material properties (Tolbert *et al.*, 2003).

Material	E_g	ϵ_r	E_c	μ_n	μ_p	λ	ν_{sat}
Si	1.12	11.9	300	1500	600	1.5	1
GaAs	1.43	13.1	400	8500	400	0.46	1
6H-SiC	3.03	9.66	2500	400	101	4.9	2
4H-SiC	2.36	10.16	2200	1000	115	4.9	2
GaN	3.45	9	2000	1250	850	1.3	2.2
Diamond	5.45	5.5	10,000	2200	850	22	2.7

The parameters in Table 2.1 are: the bandgap, E_g (eV); the relative dielectric constant, ϵ_r; the critical electric field, E_c (kV/cm); the electron mobility, μ_n ($\frac{cm^2}{V \cdot s}$); the hole mobility, μ_p ($\frac{cm^2}{V \cdot s}$); the thermal conductivity, λ ($\frac{W}{cm \cdot K}$); and the saturated electron drift velocity, ν_{sat} ($\times 10^7 cm/s$).

2.3.1 Silicon

Silicon is ubiquitous and is synonymous with the modern world. It has been the workhorse of electronics since transistors began to supersede vacuum tubes in the 1950s, beginning first with BJTs and now progressing steadily with MOSFETs and IGBTs. However, it is beginning to approach its theoretical limits in terms of $R_{DS(ON)}$ and internal capacitances, making gains increasingly incremental. Innovations in

manufacturing and structure are being used to try to alleviate this (Brown, 2006). One such example is the Superjunction MOSFET.

Silicon Superjunction

Silicon Superjunction (SJ) MOSFETs are amongst the latest advancements in Silicon MOSFET technology. Superjunction MOSFETs change the physical build of a device: instead of a strict vertical structure where thicker layers are required to block higher voltages, the idea of charge balancing is employed to cancel electric fields under reverse bias conditions, thereby reducing the necessary layer thickness to block a given voltage (Havanur and Zuk, 2015). The largest benefits are a lower gate capacitance–and, consequently, gate charge to fully turn on–and a lower $R_{DS(ON)}$ per unit area than standard Silicon. These features enable higher frequency, higher power operation of a MOSFET in the same package, thereby providing the opportunity to increase the efficiency and power density of a converter.

2.3.2 Silicon Carbide

Silicon Carbide (SiC) is one of the current most promising novel semiconductor materials for high power switching applications. A Ph.D thesis was written on the system-level benefits it could provide (Ozpineci, 2002) and the results were overwhelmingly positive, even with few MOSFETs and primarily low voltage, low current SiC diodes available. Further research has been conducted as the technology has matured and the offerings widened that continued to show strong gains.

Silicon Carbide has many polytypes; however, the two most widely available for power devices are 4H and 6H, with 4H being the polytype of choice (Tolbert *et al.*,

2003). SiC, resulting from its material properties (see Table 2.1), outperforms basic Silicon in a die of the same size both electrically and thermally. It exhibits a lower on-state resistance, blocks a higher voltage per unit area and has significantly reduced switching energies due to the smaller die structure while also evacuating heat more efficiently than Silicon; however, current packaging and bonding materials limit the recommended maximum junction temperature. Solutions are currently being devised (Horio *et al.*, 2012) so as to take advantage of its ability to operate at very high junction temperatures and eclipse Silicon in another regard.

2.3.3 Gallium Nitride

Gallium Nitride is the other semiconductor technology that has been gaining increasing attention. Its properties are favourable–more so than Silicon Carbide–to reducing switching losses. Lateral device structures, where current flows horizontally as opposed to vertically, have also helped in driving down the on-state resistance and the capacitances that contribute to switching losses. Research has shown solid leaps over Silicon performance (Reusch and Strydom, 2015,?; Huang *et al.*, 2014) and, even, over Silicon Carbide MOSFETs (Gurpinar and Castellazzi, 2016). GaN shows promise for high and low power switching applications.

Gallium Nitride devices are often referred to as High Electron Mobility Transistors (HEMTs) as a result of their high electron mobility parameter. To date, significant work has been done to design normally-off devices as opposed to normally-on. Two of the major approaches to developing an enhancement mode (normally-off) device are the cascode structure, where an enhancement mode Silicon MOSFET is placed in series with the GaN FET and gate doping, to achieve a positive threshold voltage

(Jones *et al.*, 2014).

2.3.4 Gallium Arsenide

Gallium Arsenide (GaAs) has seen use for some time in radio frequency applications. The small increase in bandgap relative to Silicon makes it less susceptible to accidental turn on due to radiation and, thus, it has been favoured for aerospace and satellite designs. The high electron mobility reduces the dynamic channel resistance of a GaAs MOSFET and, even though the relative dielectric constant is higher than Silicon, the increase in switching losses associated with a higher capacitance can be mitigated by taking advantage of the higher critical electric field, enabling a smaller die to be used and an overall lower capacitance achieved. An additional benefit of the reduction in the on-state resistance is that there is an increase in the cutoff frequency of the device, allowing GaAs MOSFETs to operate over a wide frequency band without suffering significant attenuation (Ajram and Salmer, 2001).

With respect to power electronic applications, GaAs is not widely used. Indeed, its low thermal conductivity makes evacuating heat a challenge. With junction temperature being the limiting factor of power switches, Gallium Arsenide devices are unable to sustain large power losses without significant and complex cooling solutions added. These issues do not preclude GaAs transistors from being used for power switching applications. Some research has been done–one example being (Ajram and Salmer, 2001)–that shows them as low voltage power switches; however, they are unlikely to gain much traction with the advent of Gallium Nitride devices that are superior in many regards. It is more probable that Gallium Nitride will cut in to applications that Gallium Arsenide currently holds.

2.3.5 Examples

To illustrate the benefits of wide-bandgap semiconductor materials, several important parameters related to devices used in switching applications will be introduced and elaborated upon.

The specific on-resistance is defined by (2.7). It is also referred to as the drift region resistance and, for high voltage MOSFETs, it dominates the total on-state resistance of the device (Mohan *et al.*, 2003; Havanur and Zuk, 2015). Thus, minimising $R_{on,sp}$ is an important part of driving efficiency higher. It can be clearly observed that a high permittivity, mobility and critical electric field are beneficial to this task. Referring back to Table 2.1, it becomes obvious that wide-bandgap materials are key to this endeavour.

$$R_{on,sp} = \frac{4V_B^2}{\epsilon \mu E_c^3} \tag{2.7}$$

An alternative means of quantifying the resistance is given by (2.8), which is the calculation of the resistivity of a sheet of semiconducting material in its most fundamental sense. In this case, a low resistivity is desired. This is achieved by driving the doping concentrations and mobilities of electrons and holes higher. Silicon, as a whole, tends to have higher mobilities, which favour it for a given doping density; however, wide-bandgap materials allow for higher doping to be achieved because of their higher critical electric fields and relative permittivities. Hence, when considering all factors, wide-bandgap materials can still achieve lower resistances than Silicon, per the definition of the resistivity of a semiconductor,

$$\rho = \frac{1}{q\left(N_n \mu_n + N_p \mu_p\right)} \tag{2.8}$$

where q is the value of an elementary charge and N_n and N_p are the doping densities of electrons and holes, respectively.

To help make this point, consider a simple pn diode. Its blocking voltage can be approximated as (2.9) (Mohan *et al.*, 2003),

$$V_B \approx \frac{\epsilon_r E_c^2}{2qN_d} \tag{2.9}$$

where N_d is the total doping density. For wide-bandgap materials, their numerators are significantly larger than the numerator for Silicon. The consequence of this, under equal doping levels, is a heightened blocking voltage. However, as previously discussed, the doping level is inversely proportional to the resistivity. Thus, in achieving the same blocking voltage, wide-bandgap diodes have lower resistances.

Observing the dependency of the blocking voltage on the doping of the material, a relationship can be envisioned with (2.7) in mind: as doping increases, V_B drops and, consequently, the specific on-state resistance of a MOSFET. Great benefit can be observed by pushing the doping concentration up to a certain level to achieve a desired blocking voltage.

Continuing in this vein, the specific input and output capacitances per unit area can be calculated using material parameters. They are given by (2.10) and (2.11), respectively,

$$C_{iss,sp} = \frac{\epsilon E_c}{2\sqrt{V_G V_B}} \tag{2.10}$$

$$C_{oss,sp} = \frac{\epsilon E_c}{2\sqrt{V_D V_B}} \tag{2.11}$$

where V_G and V_D are the voltages applied to the gate and drain, respectively, of the

MOSFET.

The results in table 2.2 indicate that wide-bandgap materials will have a higher specific input and output capacitance. However, it should be noted that the specific capacitances are measured in Farads per unit area. Wide-bandgap devices, relative to their Silicon counterparts, require a smaller area to block the same voltage and, hence, their capacitances will be lower. Indeed, in calculating the depletion width, this can be shown.

$$W_d = \frac{2V_B}{E_c} \tag{2.12}$$

The depletion width can alternatively be represented as,

$$W_d = \sqrt{\frac{2\epsilon V_G}{qN_d}} \tag{2.13}$$

which is (2.12) with the approximated expression for the blocking voltage–V_B, (2.9)–substituted in. This new form complicates matters by exposing an underlying relationship between the specific capacitances and the doping concentration. Previously, it was shown that the blocking voltage–and, consequently, the specific on-resistance–has a relationship with the doping levels. In turn, this implies that the doping affects both, with resistance going down with doping and capacitance rising. By substituting (2.9) in to (2.7), (2.10) and (2.11), modified forms can be obtained that are represented in equations 2.14 through 2.16.

$$R_{on,sp} = \frac{\epsilon E_c}{q^2 N_d^2 \mu} \tag{2.14}$$

$$C_{iss,sp} = \sqrt{\frac{qN_d}{2V_G\epsilon}} \tag{2.15}$$

$$C_{oss,sp} = \sqrt{\frac{qN_d}{2V_D\epsilon}} \tag{2.16}$$

As the doping level increases, the resistance decreases at a rate much faster than the capacitance rises. This result states that the conduction losses of a device can be reduced significantly with a relatively smaller increase in capacitance and, consequently, switching losses. At high load currents, this reduction can become more significant than the lowering of switching losses associated with lower device capacitances.

These forms take on greater importance when considering the Baliga and New High Frequency Figures of Merit in section 2.4. Nevertheless, the preceding discussion outlines the importance of considering each distinct parameter when determining what material is best suited for an application.

Table 2.2 summarises the intrinsic device parameter calculations and normalises them to Silicon to show the benefits to be reaped by moving to wide-bandgap materials. Calculations are made with a blocking voltage, V_B, of 1200V; a drain voltage, V_D of 800V; and a gate voltage, V_G, of 10V. For example, under this operating regimen, the required depletion region width of 6H-Silicon Carbide is 12% that of Silicon; hence, the total width of the device can be reduced to take advantage of the smaller necessary dimensions. Along with this potential reduction in device size comes the added benefit of a reduction in specific on-resistance.

Of note is the increased levels of specific capacitance, both input and output.

Table 2.2: Intrinsic device parameters, normalized to Silicon.

Material	$R_{on,sp}$	$C_{iss,sp}$	$C_{oss,sp}$	W_d	$V_{B,pn}$
Si	1	1	1	1	1
GaAs	6.76E-2	1.47	1.47	0.75	1.96
6H-SiC	7.98E-3	6.76	6.76	0.12	56.37
4H-SiC	4.48E-3	6.22	6.22	0.136	45.64
GaN	5.36E-3	5.04	5.04	0.15	33.61
Diamond	3.98E-5	15.41	15.41	0.03	513.54

For dies of the same size, the capacitances will be higher for wide-bandgap materials; however, their main benefit is in device size reduction via higher critical electric fields. Taking advantage of these properties, the capacitances can be reduced well below that of a MOSFET built using Silicon. This is shown in great detail in (Ozpineci, 2002).

2.3.6 Conclusions

The preceding discussion is not exhaustive; indeed, there exist many other materials, but they don't currently have the potential or relevance that those in Table 2.1 do. Gallium Nitride and Silicon Carbide show promise to be game changers for power electronic applications with many new devices coming to market and research showing strong gains that aren't slowing down. Compared to the ubiquitous Silicon, they block higher voltages in smaller packages (E_c); have lower on-state resistances because of the thinner layers of semiconductor material; have lower relative dielectric coefficients (ϵ_r), resulting in lower internal capacitances; and they have wider bandgaps, which give rise to many of their attractive properties.

A problem that exists is comparing the information presented in Table 2.1 and the results from section 2.3.5 to make a decision as to the performance of a material. Indeed, the synthesis of data like this, often conflicting, is a challenge. Researchers

have attempted to alleviate this problem by designing Figures of Merit, described in the following section.

2.4 Material Figures of Merit

A good method to compare different objects on equal footing is to use special metrics, referred to as Figures of Merit (FOM). These can be based off of material parameters, such as Johnson's FOM (JFOM), Baliga's FOM (BFOM), Baliga's High Frequency FOM (BHFFOM) (Baliga, 1989), the New High Frequency FOM (NHFFOM) (Kim *et al.*, 1995) and Huang's Chip Area FOM (HCAFOM) (Huang, 2004), to name a few; or, they can be specifically for physical devices, as in section 4.2.1. Figures of merit combine different parameters together, allowing for a simpler representation of a complex system. In this case, they make a comparison between the different semiconductor materials discussed in section 2.3 easier.

2.4.1 Johnson's Figure of Merit

Johnson's Figure of Merit (Johnson, 1966) is a measure that provides an upper limit on a transistor's power switching ability that is solely dependent upon the semiconductor material employed. It has units of Volts per second. Johnson's analysis shows that there is a tradeoff between the switching frequency and the amount of power being transmitted: either significant power is switched at low frequency, or little power at high frequency.

$$JFOM = \frac{E_c \nu_{sat}}{2\pi} \tag{2.17}$$

2.4.2 Baliga's Figure of Merit

Baliga's Figure of Merit (BFOM) (Baliga, 1989), defined in (2.18), is a measure of the resistive losses of a MOSFET. It is the denominator of (2.7); hence, as BFOM grows large, the specific on-resistance falls.

$$BFOM = \epsilon \mu E_c^3 \tag{2.18}$$

2.4.3 Baliga's High Frequency Figure of Merit

Baliga's High Frequency Figure of Merit (BHFFOM) (Baliga, 1989) is a measure of the switching losses. Based off of experimental data from previous research, it assumes that the input capacitance of a MOSFET, (2.4), is the dominant switching loss generating mechanism as the charging of the gate-source and gate-drain capacitances is directly related to the turn on of a MOSFET. The BHFFOM's unit is Hertz; hence, the denominator can be thought of as an RC time constant. The higher the value–i.e. the shorter the time span; or, the faster the charging time of the capacitances–the better.

$$BHFFOM = \frac{1}{R_{on,sp} C_{iss,sp}} \tag{2.19}$$

Recall the discussions surrounding equations 2.14 through 2.16. The BHFFOM and NHFFOM are calculated by taking the product of the specific on-resistance and respective capacitance. Substituting (2.14) and (2.15) in to (2.19), a different representation of the BHFFOM can be obtained.

$$BHFFOM = \frac{\mu \left(qN_d\right)^{1.5} \sqrt{2V_G \epsilon}}{E_c} \tag{2.20}$$

This expression validates the thinking previously discussed in section 2.3.5. As the doping concentration, N_d, is increased, the resistance falls more rapidly than the capacitance rises and it becomes more beneficial from a figure of merit standpoint to continue doping to reduce the power losses. Furthermore, the doping level goes hand in hand with the blocking voltage, as noted by (2.9). High blocking voltage MOSFETs are not favourable for maximising the BHFFOM as they require either a high doping level for a given critical electric field to reduce the on resistance, causing an increase in capacitance; or, an increase in the width of the device to reduce the resistance, again increasing the capacitance. There is a strong tradeoff between resistance capacitance, between conduction and switching losses.

2.4.4 New High Frequency Figure of Merit

The New High Frequency Figure of Merit (NHFFOM) (Kim *et al.*, 1995) is similar in nature to the BHFFOM, except instead of considering the input capacitance, it considers the output capacitance, $C_{oss} = C_{DS} + G_{GD}$.

$$NHFFOM = \frac{1}{R_{on,sp} C_{oss,sp}} \tag{2.21}$$

Just like the BHFFOM, the NHFFOM can be rewritten by making the appropriate substitutions of (2.14) and (2.16) in to (2.21).

$$NHFFOM = \frac{\mu \left(qN_d\right)^{1.5} \sqrt{2V_D\epsilon}}{E_c} \tag{2.22}$$

Depending on the circuit topology and the means by which losses are calculated for a MOSFET, the NHFFOM may not have much meaning. If soft switching is

employed, then the energy stored in the output capacitance, $E_{oss} = \frac{1}{2}C_{oss}V_{DS}^2$, tends to zero. If the typical linearised inductive switching model is used, research indicates that this term more or less cancels itself out when going through a full switching cycle (Xiong *et al.*, 2009).

Nevertheless, despite its inapplicability in certain cases, the NHFFOM remains a useful tool for understanding material performance.

2.4.5 Huang's Chip Area Figure of Merit

Huang's Chip Area Figure of Merit (HCAFOM) (Huang, 2004) is one of a series of figures of merit proposed to further exemplify the benefits of wide-bandgap materials. The chip area FOM is a measure of the relative size (area) of a chip for a given operating condition. A smaller chip area implies lower losses.

$$HCAFOM = \epsilon\sqrt{\mu}E_c^2 \tag{2.23}$$

The three parameters that comprise the chip area FOM–the dielectric constant, mobility and critical electric field–follow logically: a higher mobility implies lower resistance and, thus, losses; a higher critical electric field would mean the device does not need to be as thick to block a voltage, reducing the resistance and capacitance; and a high dielectric constant would reduce the size requirements of the gate for building an electric field to create the depletion region and also the internal capacitances formed by the electrodes.

2.4.6 Summary

Table 2.3 summarises the figures of merit discussed, when normalized to Silicon. The BHFFOM and NHFFOM are equal when looking at the same material when normalised to Silicon because the only terms changing are the critical electric field and the relative permittivity. The general consenus of the analyses is that wide-bandgap materials result in higher FOMs and, thus, are indicative of superior performance when used to fabricate a switching device.

Table 2.3: Material dependent FOMs, normalized to Silicon.

Material	JFOM	BFOM	BHFFOM	NHFFOM	HCAFOM
Si	1	1	1	1	1
GaAs	1.33	14.79	10.07	10.07	4.66
6H-SiC	16.67	125.27	18.52	18.52	29.11
4H-SiC	14.67	223.15	35.85	35.85	37.27
GaN	14.67	186.74	37.04	37.04	30.68
Diamond	90	25,106.34	1629.23	1629.63	621.93

2.5 Device-Specific Figures of Merit

Following from the material-specific figures of merit are ones designed specifically for switching devices. These FOMs are very useful for making a like-for-like comparison of transistors with varying parameters.

2.5.1 Baliga's High Frequency Figure of Merit

Baliga's High Frequency Figure of Merit, (2.19), is applicable to both materials and switches. When using the BHFFOM to draw conclusions about the quality

of switches, it should be noted that it is valid only for MOSFETs. The on-state resistance and output capacitance can be taken from the datasheet under expected operating conditions, with the resistance being valid at higher voltages where the drift region resistance dominates the total resistance. A high BHFFOM is indicative of a good switch at high frequencies.

2.5.2 New High Frequency Figure of Merit

The New High Frequency Figure of Merit, 2.21, for a device, just like in the material case, is very similar to the BHFFOM. It is only valid for MOSFETs. A high NHHFOM is favourable for reducing the losses of an application.

2.5.3 Power Density Figures of Merit

The power density figures of merit were proposed in (Wang, 2007) as a means of determining which transistor, from a set of devices, would be favourable for a high power density design. This is achieved by maximising each of equations 2.24 through 2.26. What is essentially being calculated is the product of loss-generating mechanisms over a given area and how efficiently the heat can be extracted. They are given by,

$$PDFOM_{MOSFET} = \frac{1}{\sqrt{R_{DS(ON)}Q_{gd}}A_{pack}R_{th}} \tag{2.24}$$

$$PDFOM_{IGBT} = \frac{1}{V_{CE(sat)}(i)\left(E_{on}(i) + E_{off}(i)\right)A_{pack}R_{th}} \tag{2.25}$$

$$PDFOM_{diode} = \frac{1}{V_F(i)E_{rr}(i)A_{pack}R_{th}} \tag{2.26}$$

where A_{pack} is the area of the package; Q_{gd} is the gate-drain charge, which is closely associated with the gate-drain capacitance and the drain-source voltage; and R_{th} is the thermal resistance, in $\frac{K}{W}$, stating the temperature rise for a given power loss.

The PDFOM experiences several drawbacks. One example is that it is calculated only for a specific device type. For example, co-packaged freewheeling diodes, either an additional component for IGBTs or the parasitic body diode for MOSFETs, are not taken in to account when calculating the FOM. Many modern IGBTs have these built-in for ease of design; furthermore, for MOSFETs, quite often the body diode is used for freewheeling purposes. A second issue is that the units of the MOSFET and IGBT PDFOMs are not identical, making it difficult to compare the two directly.

Nevertheless, the PDFOMs are useful tools for preliminarily determining the most size efficient devices for a design.

2.5.4 MOSFET Figure of Merit

The MOSFET FOM can be written as (2.27) (Brown and Moxey, 1995).

$$FOM_{MOSFET} = Q_G \cdot R_{DS(ON)} \tag{2.27}$$

The MOSFET FOM is the product of two parameters that give an indication of losses: the on-state resistance and the gate charge. Generally speaking, if the required gate charge to have the MOSFET fully on is high, so, too, will be the switching losses. This can be realised simply by thinking of the case where a device is being turned on by a constant current source. Since current is the amount of charge moving per unit time, $I = \frac{dQ}{dt}$, a fixed current means Q Coulombs will be on the gate in t seconds. Hence, a large Q is unfavourable to achieving fast turn on and,

consequently, low switching losses. The on-state resistance dictates the conduction losses and is simpler to envision: a large $R_{DS(ON)}$ generates proportionally higher losses across the conduction channel.

The goal is to reduce this FOM; however, there is a tradeoff between the two. More material is required to reduce the resistance; yet, an increase in material drives an increase in the required gate charge, arising from the higher capacitance. Process advancements, such as the Superjunction MOSFET, have helped to lower the product.

2.5.5 IGBT Figure of Merit

The IGBT figure of merit, similar to the MOSFET FOM, is the product of two of the major loss generating mechanisms. It can be simplified from its form in (Suzuki and Masuoka, 2015) and written as (2.28). The IGBT FOM should be driven as high as possible, thereby implying that low losses would be exhibited in an application.

$$FOM_{IGBT} = \frac{1}{V_{CE(sat)} \cdot E_{off}} \tag{2.28}$$

2.6 Summary

This chapter outlined the three most prevalent technologies for switching devices and provided their basic operating characteristics. Benefits and drawbacks were discussed that resulted in compartmentalizing them for specific applications: BJTs for current amplification at the expense of high base driving power requirements; MOSFETs for high frequency, low current converters; and IGBTs for low frequency, high current and high voltage applications. Recent innovations in Silicon manufacturing, such as hybrid devices and Superjunction technology, were reviewed.

A comprehensive analysis of semiconductor materials was undertaken, showing clearly the benefits that can be seen by fabricating devices with wide-bandgap materials. Specific resistance and capacitances were shown to be lower when full advantage was taken of the enhanced electrical properties these materials exhibit. These reductions lead to a decrease in power losses, both conduction and switching, enabling an increase in efficiency and the potential for system footprint reduction.

Further analysis with figures of merit, metrics devised by researchers to compare different subjects, showed that wide-bandgap materials outperformed Silicon by a significant margin. These include low frequency and high frequency operation and the required die size for a given power loss. Other FOMs not explicitly discussed, albeit covered in literature, point to benefits from moving to wide-bandgap materials.

Additional figures of merit designed specifically for switching devices were introduced and discussed. They find use in chapter 4 as a part of the component selection process during converter design.

Chapter 3

Inverter Modelling and Analysis

3.1 Switch Modelling Techniques

Comprehensive modelling of transistors is key to not only understanding and predicting the underlying phenomena during operation, but also for accurately estimating converter performance and cooling requirements. A significant amount of research effort has been invested in this field, with many papers being widely disseminated that show improvements in accuracy by tweaking models, adding layers of complexity and integrating insights obtained from experimentation.

Modelling can be broken in to three major groups–simulation, analytical and testing–and then further sub-divided based off of how the techniques are executed. A discussion of the findings presented in studies follows, with conclusions drawn at the end to justify the modelling approach taken for the design of a converter.

3.1.1 Simulation

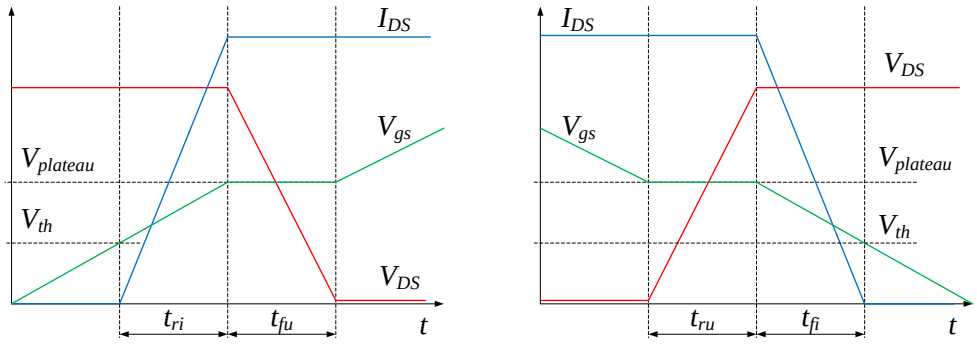
Simulation covers device models (e.g. SPICE) and physics-based, where a virtual transistor can be designed and analysed. The former leaves the designer at the whim of what the manufacturer provides in the model or what can be physically deduced and programmed, whereas the latter can be difficult to apply to commercially available devices. Therefore, neither approach is particularly good for generalised applicability, though they do give an excellent understanding of what is physically occurring and allow for strong insight in to the problem.

An excellent example of insight being obtained from a physics-based simulation that is applicable to other techniques was reported by (Xiong *et al.*, 2009). The authors found that the linearised inductive switching model overcompensates losses enough such that the energy stored in the output capacitance can be disregarded. While not explicitly stated in the publication, this, in turn, implies that the most significant driver of non-linear energy losses is due to the parasitic inductances.

3.1.2 Analytical

Analytical techniques, on the other hand, aim to develop equations, either for a specific application or for mapping switching performance under general conditions. Most analytical methods utilise datasheet parameters in some form and, for increased accuracy, begin to account for parasitic components; however, the degree of complexity of analysis goes hand-in-hand with the accuracy, which often has diminishing returns in terms of utility to the designer.

The simplest and most popular technique to use is the linearised switching model. It takes two forms: resistive and inductive. The differences between the two are



(a) Turn-on waveforms. (b) Turn-off waveforms.

Figure 3.1: Linearised inductive switching model waveforms.

when the voltage and current begin to rise and fall relative to one another when the transistor is turned on and off. Most real loads have some inductance, with some having a substantial amount (e.g. electric motors, transformers). Therefore, the model which will be examined more deeply is the inductive switching model. Figure 3.1 shows the primary waveforms when considering linearised inductive switching.

The estimation of the switching losses under the linearised model depends heavily upon the rates at which the current and voltage transition. A longer transition time would incur higher losses whereas a smaller time would lead to a reduction. This requires a calculation of the rise and fall times of both the current and voltage. The transition times of the currents are given by,

$$t_{fi} = R_g C_{iss} \ln\left(\frac{V_{plateau}}{V_{th}}\right) \tag{3.1}$$

$$t_{ri} = R_g C_{iss} \ln\left(\frac{V_{drive,high} - V_{th}}{V_{drive,high} - V_{plateau}}\right) \tag{3.2}$$

where R_g is the total gate resistance, which includes internal and external resistances; and $V_{drive,high}$ is the higher of the two applied gate voltages, which is meant to turn the switch on. These expressions are obtained from (Brown, 2004).

The second half of the energy loss expression requires the computation of the rise and fall times of the voltage. These can be obtained by using the following two expressions,

$$t_{fu} = \left(V_{DS} - V_{DS(on)}\right)\left(\frac{R_g C_{rss}}{V_{drive,high} - V_{plateau}}\right) \tag{3.3}$$

$$t_{ru} = \left(V_{DS} - V_{DS(on)}\right)\left(\frac{R_g C_{rss}}{V_{plateau} - V_{drive,low}}\right) \tag{3.4}$$

where $V_{drive,low}$ is the lower of the two gate voltages, which is used to turn the gate off quickly. These are taken from (Graovac *et al.*, 2006).

The parasitic capacitances of the MOSFET are non-linear functions of the drain voltage. At high voltages, the capacitances fall, whereas at low voltages they rise. A typical set of curves from a device datasheet (ROHM Semiconductor, 2015) are presented in Figure 3.2. This raises a point on how the reverse transfer capacitance and input capacitance, C_{rss} and C_{iss}, in equations (3.1) through (3.4) should be determined. Their value has a direct impact on the rise and fall times of the waveforms. Often, this is a designer decision, where some choose the maximum, others the minimum, and others still something in-between.

In choosing an appropriate value for the capacitances, the total switching losses can then be estimated as,

$$E_{sw} = \frac{1}{2} V_{DS} I_{DS} \left(t_{on} + t_{off}\right) + \frac{1}{2} C_{oss} V_{DS}^2 \tag{3.5}$$

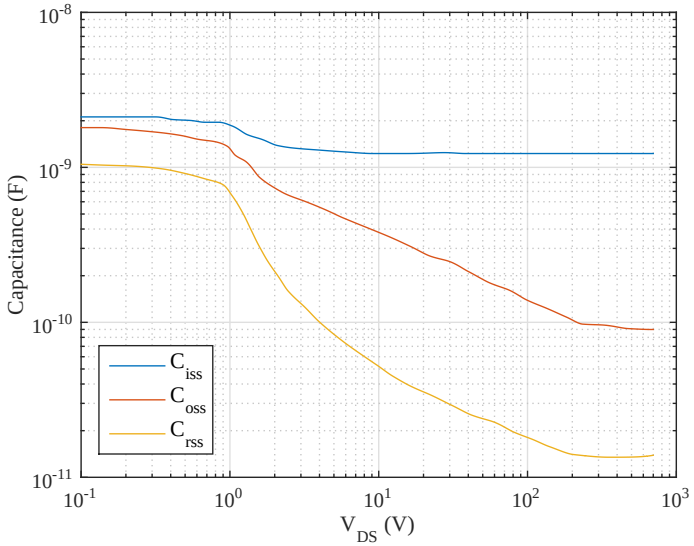


Figure 3.2: Parasitic capacitances of SCT2120AF Silicon Carbide MOSFET.

where $t_{on} = t_{fu}+t_{ri}$ and $t_{off} = t_{ru}+t_{fi}$. The inclusion of an energy term for the output capacitance is logical: the physical construction of a MOSFET leads to parasitic capacitances between its terminals, and a capacitor stores energy in the form of an electric field. When the switch is turned on, a potential difference is seen between the drain and the source, providing the parasitic capacitor the opportunity to discharge to the point where $V_{DS} = V_{DS(on)}$. This energy is dissipated in the conduction channel of the device. When the device is turned off, the output capacitance is again charged to the DC bus voltage, beginning the cycle anew.

A modification to the basic switching model is presented in (Guo *et al.*, 2015), where the authors discretise the capacitance curve and evaluate it over different values of V_{DS}. The result is a series of smaller time intervals, per (3.6), which can be summed to more accurately determine the rise and fall times. The difference between taking the mid-point of the C_{rss} curve and the proposed modification is over a factor of 10, allowing for a much more accurate estimation of the losses. The calculation of the

modified fall time is computed by,

$$t_{fu}^{*} = \sum_{i=1}^{N} \Delta V_{DS} \left(\frac{R_g C_{rss}(V_{DS} - (i-1)\Delta V_{DS})}{V_{drive} - V_{plateau}} \right) \tag{3.6}$$

where N is the number of intervals to be employed in the calculation; and V_{DS} is the voltage difference between intervals, calculated as (3.7).

$$\Delta V_{DS} = \frac{V_{DS} - V_{DS(on)}}{N} \tag{3.7}$$

The same treatment can be applied to the input capacitance, C_{iss}, to enhance the accuracy of its estimation and, consequently, the switching energy loss.

Despite the enhancements to the model, it still does not capture the dynamic nature of the actual switching transitions. Indeed, ringing from the parasitic capacitances and inductances is ignored, as are the effects on the gate charging and discharging waveforms. It is very difficult to take in to account the ringing, as it is very much device, packaging and interconnection layout specific; hence, the latter case is most reasonable to examine next. The effects of gate charging and discharging are discussed in (Brown, 2006), where a series of generic equations are developed and used to estimate the switching losses of a MOSFET in a buck converter. It is an extension of the work presented in (Brown, 2004).

In this study, the author further redevelops the fundamental equations from (Brown, 2004). The dependence of the MOSFET's parasitic capacitances as the drain-source voltage changes is emphasised and used for the calculations of rise and fall time. The findings of the study are summarised with a series of tables that compare measured and calculated transition times with different values plugged in to

the equations. Generally poor correlation is obtained throughout, which is likely attributable to poor selection in the value of the input capacitance. The selection of the values for the capacitances is of the utmost importance and, hence, the methodology presented in (Guo *et al.*, 2015) is important.

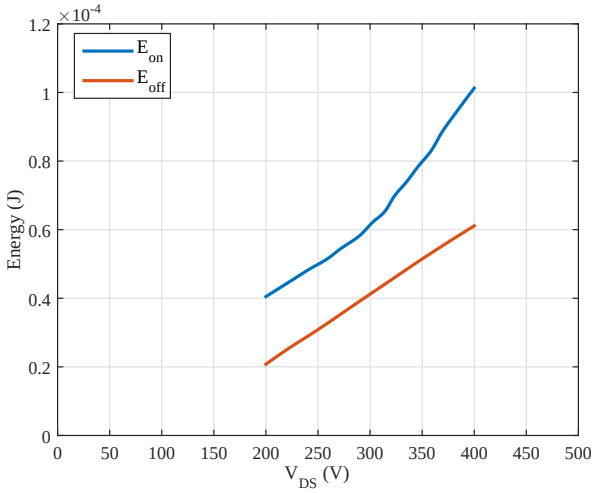
Both of these models assume that the rise of the gate-source curve flattens out and is constant at what is called the *Miller plateau*, which is when the voltage begins to rise and fall during turn-off and turn-on. Little literature is available on this subject, with only a few application notes, such as (McArthur, 2001), which indicates that the rise and fall times of the voltage and current would be non-linear. One could expect that the curves would fall much more rapidly than in the case where the plateau is flat, meaning that a linearised analysis would overestimate the losses.

Delving deeper in to the modelling of MOSFETs, the investigation by (Xiong *et al.*, 2009), as previously mentioned, determined that the output capacitance term can be neglected in (3.5), thereby simplifying the expression to (3.8).

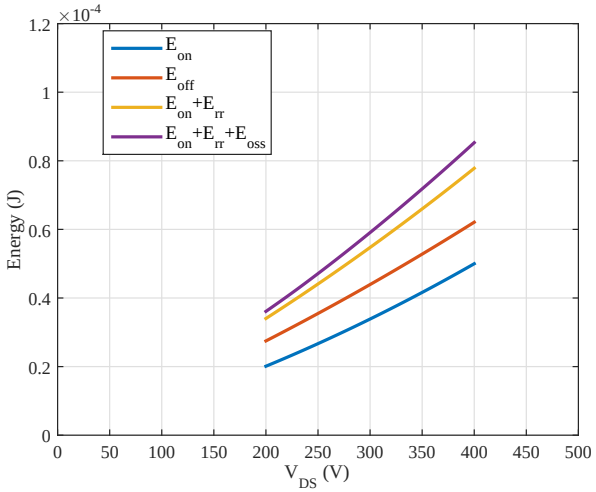
$$E_{sw} = \frac{1}{2} V_{DS} I_{DS} \left(t_{on} + t_{off} \right) \tag{3.8}$$

Some preliminary investigation for the development of a comprehensive loss model of a MOSFET was undertaken and it showed that this omission may not be appropriate in all cases. Consider the Silicon Carbide MOSFET *SCT2120AF*, manufactured by ROHM Semiconductor (ROHM Semiconductor, 2015). The energy loss curves over voltage and current show that, at lower levels, the result is approximately linear; however, at higher values, a non-linear, seemingly quadratic term arises. This implies that the output capacitance and the parasitics added to the losses measured in a significant fashion, particularly over the *on*-switching interval. Testing this hypothesis

yields Figure 3.3, where the on and off switching energies are calculated per (Guo *et al.*, 2015) while varying the DC-link voltage. Artefacts in plot (*a*) are a result of the curve tracing operation employed to extract the curves from the datasheet.



(a) SCT2120AF datasheet switching losses.



(b) Estimated SCT2120AF switching losses.

Figure 3.3: Datasheet and estimated switching losses of SCT2120AF MOSFET.

In the device's datasheet, the on-switching energy has the reverse recovery losses added to it; hence, these had to be calculated. An approximation utilised was to

observe the typical reverse recovery waveform in textbooks and in the datasheet itself to, under the conditions described in the document, create a quadratic function to approximate the curve, since no value was explicitly given. While not perfect, it provides an idea of the reverse recovery energy loss.

When neglecting both the reverse recovery and stored output energy, the on-switching interval is grossly underestimated at all voltages, though the effect is amplified at higher values. The addition of both loss terms gives good correlation, though not exact, which can likely be attributed to a non-linear rise in reverse recovery losses as the voltage level increases due to parasitic effects in the test setup. Off losses remain linear over the assessed range, which matches well with the datasheet.

These results indicate that the conclusion drawn in (Xiong *et al.*, 2009), where the energy stored in the output capacitance can be neglected, does not hold; indeed, they concur with the notion that parasitics need to be taken in to account, as they change the turn-on and -off waveforms, as well as causing ringing, which further adds to the losses. Studies published have considered the impacts of parasitics in great detail. For example, in (Reusch and Strydom, 2014), the impacts of the parasitic inductance of the commutation loop and a Gallium Nitride MOSFET are studied. The general conclusion is that the lower the loop inductance, the higher the efficiency and the rate at which it can switch.

Other studies have built comprehensive analytical models to include the parasitic components, complete with equations describing each aspect of the turn on and turn off of a MOSFET. It began with (Ren *et al.*, 2006), where the output stage of a buck converter is investigated, thanks to the simplicity with which it can be equivalently represented. An enhancement to the aforementioned model is presented by

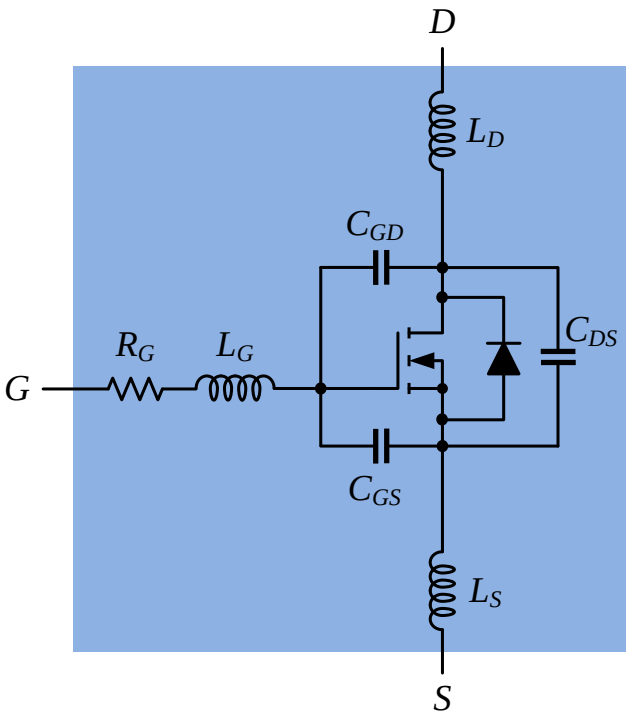


Figure 3.4: Model of a MOSFET with all major parasitics included.

(Rodríguez *et al.*, 2010). The model of a single MOSFET that is used is shown in Figure 3.4.

As an exercise to assess the tradeoff in modelling complexity and accuracy presented by each study, a comparison between the losses of the basic model and the presented model can be executed upon. In (Ren *et al.*, 2006), the authors state the switching losses of a physics-based simulation, which is also the benchmark; the linear inductive switching model; and their proposed analytical model, with the parasitics included. The percent deviations from the benchmark for the basic and complex models are, respectively, -19% and +7.7%. Overassessing is preferable to underassessing,

as a heatsink is normally designed to maintain a certain junction temperature under a given loss profile; hence, though the system would be marginally overdesigned, it would be operate well over the entirety of its specified lifetime. Experimental results closely matched the complex model, giving it good validation.

Muddying the waters are the results presented in (Rodríguez *et al.*, 2010). In this study, the authors sought to expand upon the model developed by (Ren *et al.*, 2006). At the end, several comparisons between the proposed model and the basic linear inductive switching model are shown with diverging conclusions. In one figure, the on and off energies for both are plotted under several operating conditions: voltage, current and frequency. These cases exhibit that the off losses are underestimated, whereas the on losses are grossly overestimated. However, when the two are summed together, the basic model's predicted power losses are very close to the enhanced model's. Since the total switching interval losses have more meaning than the individual on and off cycles, the conclusion can be drawn that moving forward with a complex model may not be necessary. Two further experiments show a divergence in the models by an appreciable margin, whereas a fourth and final experiment then gives more weight to the original conclusion drawn that a complex model needn't be used to accurately capture performance. Such inconsistencies make it difficult to trust the results from the study while also raising doubts about the work presented by (Ren *et al.*, 2006).

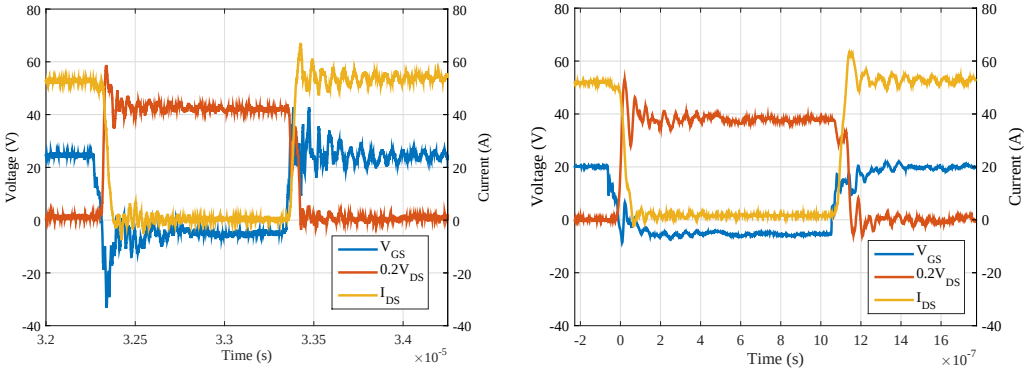
The methods outlined by (Ren *et al.*, 2006) and (Rodríguez *et al.*, 2010) can be prohibitively difficult to develop and evaluate. The authors of (Wang *et al.*, 2013) acknowledge the modelling difficulties and present a paper that develops equations and theory that are capable of neatly describing the effects of parasitic components on the

switching characteristics for the same buck converter topology previously employed. The most interesting results are the figures which show the individual impact of each parasitic component on all key waveforms over time: voltage, current and power. Broadly speaking, as a single parasitic component increases, so, too, do the switching losses. This is not always the case, though it holds in many cases; furthermore, the interaction of one parasitic with another and the relative change as they increase and decrease in tandem are not explored in depth due to the sheer scale of said problem.

3.1.3 Testing

Testing is a straightforward approach: a test circuit is built which, depending on what kind of study is being undertaken, will assess the performance of an individual switch or an entire circuit. The results can be used to build a comprehensive model, such as those presented by (Merkert *et al.*, 2014) and (Blaabjerg *et al.*, 1995); alternatively, they can be used to show general trends underlying the type of device and the material with which it was fabricated, as in (Jahdi *et al.*, 2014). For the former, the data is normally processed, fitted to a curve and used to more accurately estimate losses in-system. Linearity is exhibited in switching losses for IGBTs and Silicon Carbide MOSFETs in (Blaabjerg *et al.*, 1995) and (Jahdi *et al.*, 2014), respectively, whereas in (Merkert *et al.*, 2014) the switching energy curves are strongly quadratic at higher load currents.

The most severe drawback to testing is that no real insight about generalised performance can be gleaned. The losses and waveforms are valid for that test alone: a given switching frequency, cabling arrangement, voltage and current levels, device under test, etc. Without a controlled study where pieces are added and subtracted,



(a) Double pulse test on a test board.

(b) Double pulse test on first iteration of inverter board.

Figure 3.5: Double pulse test waveforms with $V_{DC} = 200\text{V}$ and $I_{DS} = 50\text{A}$ on two different test platforms.

such as (Wang *et al.*, 2013), the effects of parasitic components and circuit topology cannot be examined. Nor can a scaleable model be built.

An advantage of testing relative to other methods, however, is that it can provide more realistic waveforms, which include the ringing resulting from parasitic inductances and capacitances of the packaging and the interconnection mechanism. However, depending on the design of the interconnection, the result can be substantially different. Take, for example, Figure 3.5, where a double pulse test (DPT) for obtaining the switching losses is performed on two different test setups under the same conditions of $V_{DC} = 200\text{V}$ and $I_{DS} = 50\text{A}$. The left figure is the test run on a board designed specifically for a DPT, whereas the figure on the right is on the first iteration of the inverter designed for this thesis. The results are markedly different, with more substantial peaks and troughs encountered, as well as more pronounced ringing and measurement noise.

While it is the most reliable method for realistic results and is the means by

which models are validated, a testing-only regimen is time consuming and lacking in scalability and, therefore, not ideal for generalised design. Furthermore, for best results, the transistor should be characterised on the intended platform; however, this would require a full design commitment to a transistor, rendering analysis and substantiated decision making obsolete.

When a design is unwaveringly committed to, though, testing is the best means by which the converter can be characterised and a loss model developed under real-world conditions. Some such examples are shown in (Jahdi *et al.*, 2014; Zhang *et al.*, 2011; Glaser *et al.*, 2011; Merkert *et al.*, 2014; Blaabjerg *et al.*, 1995).

3.1.4 Conclusions

From the preceding discussions, no clear conclusion can be drawn as to what model for the switching circuit provides the best results aside from testing, as the greatest uncertainty comes from the circuit where the switch operates; however, it can be said that the basic linearised model provides a "good enough" solution that can be used as a starting point for a design before committing to a more comprehensive analysis. A sufficient number of publications have shown that linearity holds well when performing switching loss experiments (Jahdi *et al.*, 2014; Blaabjerg *et al.*, 1995; Blaabjerg and Pedersen, 1997). Linearity has seen use in other studies for converter analysis (Biela *et al.*, 2011; Shang *et al.*, 2014). From these publications, it can be deduced that linearity is a rational approach to determining the losses of a converter.

3.2 Three-Phase Inverter Modelling

An inverter converts DC quantities to AC quantities. Many topologies exist, as outlined in (Ye *et al.*, 2012b); however, only a voltage source inverter will be discussed in detail in this work. A typical schematic of a three-phase inverter for a motor drive application is presented in Figure 3.6.

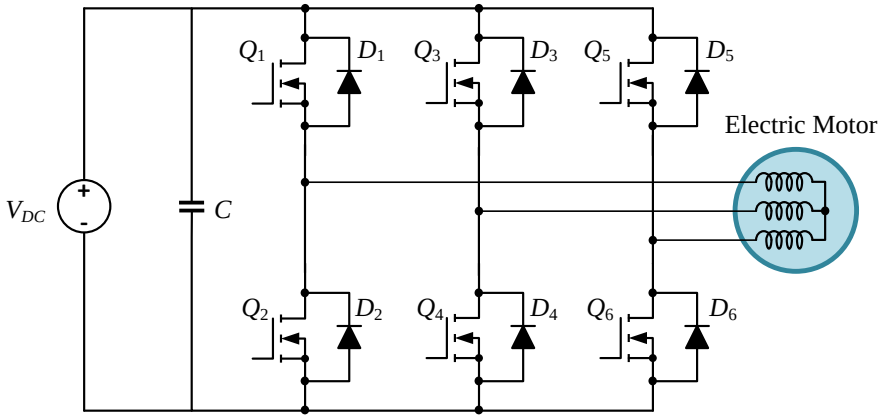


Figure 3.6: Three-phase inverter schematic.

3.2.1 Sinusoidal Pulse Width Modulation

Pulse Width Modulation (PWM) is a technique by which a series of two-level–high or low–pulses are generated and transmitted. As the name implies, the width of the pulse is controlled, allowing for the on- and off- time to vary at a fixed frequency. PWM is the most popular modulation technique for representing an analog signal digitally, particularly when controlling a power transistor.

Sinusoidal PWM is a subset of PWM that is used for generating a train of square

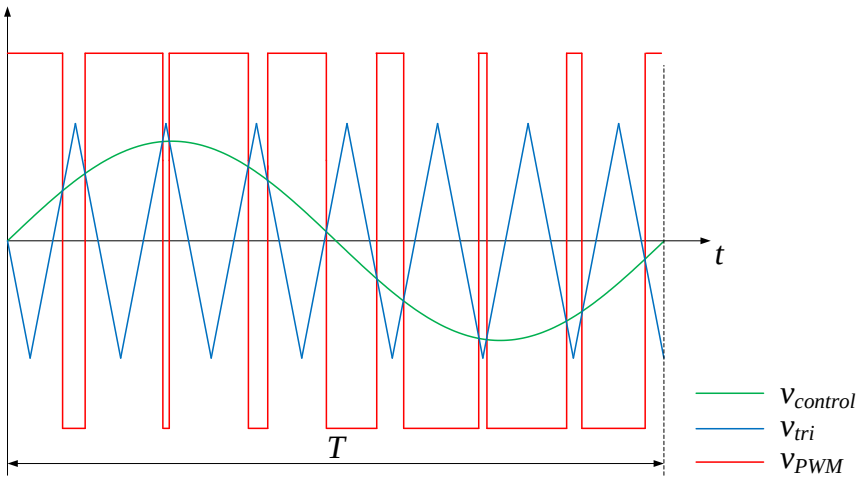


Figure 3.7: Sinusoidal Pulse Width Modulation.

waves that, on average, represent a sine wave. In SPWM, a triangular carrier waveform is compared with a reference sinusoid. If the carrier is greater than the sine wave, then the output goes low and the transistor is commanded to turn off; if the sinusoid is greater than the carrier, then the output is high and the transistor turns on. This operation is exhibited in Figure 3.7.

The carrier, v_{tri}, is the rate at which v_{PWM} switches and, consequently, the transistors. The higher its frequency, the closer the output waveform resembles a sinusoid. The frequency of the reference sine wave, $v_{control}$, controls the frequency of the sinusoid being output by the modulation strategy.

The determination of the characteristic voltages and currents associated with any modulation technique is of key importance to understanding the performance of a system. The voltages are simple: they are a series of square waves, with an average value representing a sinusoid, that switch between several fixed levels. The currents, however, are of greater interest, particularly when considering the loss estimation in

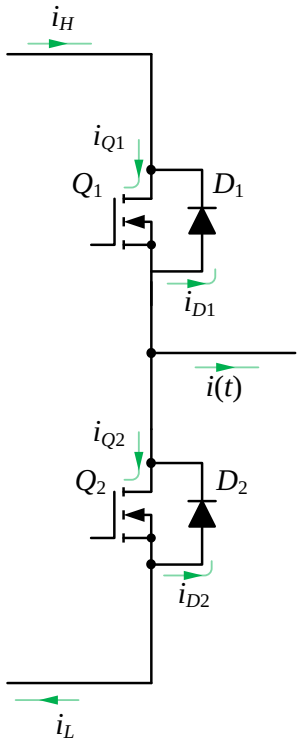


Figure 3.8: Single phase leg analysis of a three-phase inverter under SPWM.

the proceeding section. They can be calculated by considering a single phase leg of a three-phase inverter, shown in Figure 3.8.

To derive a simple, closed-form expression, several assumptions have to be made: the first is that the switching frequency is sufficiently high such that the output current waveform is a smooth sinusoid; the second is that there is no delay nor deadtime during the switching operations; and the third is that there are no resistive voltage drops in the conduction path. These assumptions impact the waveforms and, consequently, the estimated efficiency of the inverter. The inclusion of deadtime in the calculation would cause a drop in the voltage of the fundamental and require

compensation by increasing the modulation index, as would the inclusion of voltage drops. Together, these two would cause the value of the current waveform to fall, assuming no closed-loop control is present. Furthermore, deadtime would add distortion to the output current waveform. The resistive losses themselves depend on the currents, creating a complex coupled problem; therefore, it is simpler to ignore them for initial estimation. A method by which the impact of deadtime can be assessed and compensated for is presented in (Jeong and Park, 1991).

From Kirchhoff's current law, the output current–the smooth sinusoid $i(t)$–can be written as the sum of the currents entering and exiting the phase leg, $i(t) = i_H(t) - i_L(t)$, with $i_H(t)$ being the high-side current and $i_L(t)$ the low-side current, as exhibited in Figure 3.8.

The reference sinusoid, $v_{control}$, which determines the output frequency of the sinusoid, can be described as,

$$m(t) = M\cos(\omega t) \tag{3.9}$$

where M is the modulation index, which is the ratio of peak output voltage to the DC-link voltage. The output current waveform, $i(t)$, follows the reference waveform, albeit with a displacement angle, ϕ, resulting from the power factor of the load.

A duty cycle function, operating over the interval $[0, 1]$ is defined by (3.10).

$$d(t) = \frac{1}{2}\left(m(t) + 1\right)) \tag{3.10}$$

Over the interval $[0, \frac{1}{2}]$ the low-side switch and high-side diode are conducting and over the other half, $[\frac{1}{2}, 1]$, the high-side switch and low-side diode are conducting.

Instantaneous expressions for the high- and low-side currents can be calculated by multiplying the current waveform,

$$i(t) = I\cos(\omega t - \phi) \tag{3.11}$$

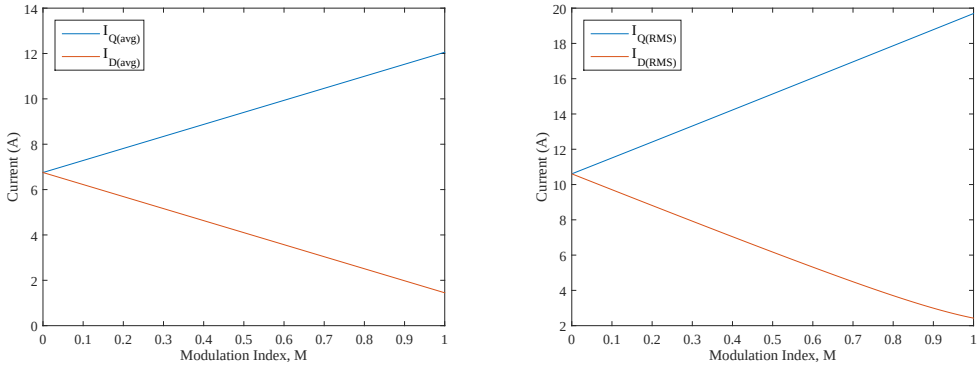
where I is the peak current, by the duty function. By using the average and RMS value integrals, the currents for the diodes and transistors in the phase leg can be determined.

$$I_{Q1} = \frac{1}{2\pi}\left(\int_{-\frac{\pi}{2}+\phi}^{\frac{\pi}{2}+\phi}\Big(d(t)I\cos(\omega t - \phi)\Big)^{j} d(\omega t)\right)^{\frac{1}{j}} \tag{3.12}$$

$$I_{D1} = \frac{1}{2\pi}\left(\int_{\frac{\pi}{2}+\phi}^{\frac{3\pi}{2}+\phi}\Big(-d(t)I\cos(\omega t - \phi)\Big)^{j} d(\omega t)\right)^{\frac{1}{j}} \tag{3.13}$$

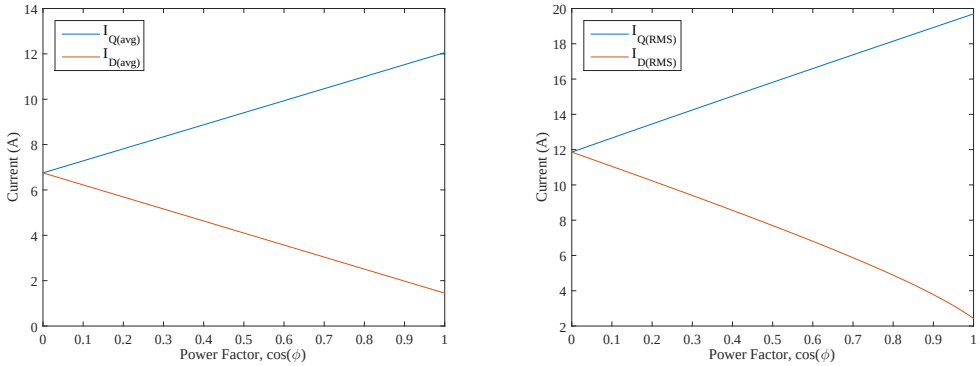
In these expressions, j is a number, either 1 or 2, which determines whether the integral evaluates the average ($j = 1$) or RMS ($j = 2$) value. As a result of symmetries in the system and the assumptions made, the currents in the high-side and low-side devices will be equal.

Solving the integrals will yield closed-form expressions with which the currents are quantified. The solved expressions can be used to observe what effects different values of modulation index and power factor have on the currents. Plots are shown in Figures 3.9 and 3.10 with a load current of 30A RMS.



(a) Diode and transistor average currents. (b) Diode and transistor RMS currents.

Figure 3.9: Sweep of the modulation index under SPWM with $\cos\phi = 1$ and $I_{o,RMS} = 30A$.



(a) Diode and transistor average currents. (b) Diode and transistor RMS currents.

Figure 3.10: Sweep of the power factor under SPWM with $M = 1$ and $I_{o,RMS} = 30A$.

3.3 Converter Loss Estimation

Converter loss estimation is essential when undertaking a design. The power losses generate heat, which must be evacuated from the package to ensure the junction temperature does not exceed a prescribed level. With Silicon devices, this is normally 150°C; with Silicon Carbide, this can go higher, though packaging and bonding materials are limiting factors and require further research (Horio *et al.*, 2012). The size

and complexity of the power devices, circuit topology and heatsink depend directly on the losses. A well-designed power converter will have minimal size and complexity in all aspects.

Power losses can be broken in to two major categories: switching and conduction. Switching losses are the result of the non-instantaneous nature of voltage and current transitions (Figure 3.1), whereas conduction losses are the power losses generated from currents passing through a non-ideal conducting medium. Switching losses are normally listed in energies, with units of Joules, which allows for a straightforward application to circuits with variable switching frequencies. The on and off energies can be exactly modelled as,

$$E_{on} = \frac{1}{T}\int_0^{t_{on}} v_{DS}(t) i_{DS} dt \tag{3.14}$$

$$E_{off} = \frac{1}{T}\int_{DT}^{DT+t_{off}} v_{DS}(t) i_{DS} dt \tag{3.15}$$

where T is the fundamental period, which is the inverse of the switching frequency, f_s; and D is the duty cycle, the ratio of on-time to off-time over the switching period. In preliminary analyses, the time-dependent waveforms for voltage and current are not necessarily known, nor will their exact characteristics be known due to parasitic components in the transistor and the circuit. This requires a general adjustment of the energies over all operating points.

The discussion from section 3.1 outlined methods and difficulties associated with the estimation of switching energies and concluded that a linearised model, where the energies are exactly proportional to the voltage and current applied, is sufficiently

good for commencing a design. This can be considered as a sort of optimisation of the design over the entirety of its range, where the best transistor can be selected from a set for a design. Once determined, detailed simulations can be performed to check the validity of the selection at critical operating points.

The switching energies are listed in the datasheet of the component under different test conditions and can be scaled per the linear assumption as,

$$E^* = E\left(\frac{V_{DC}}{V_{datasheet}}\right)\left(\frac{I_{Q,avg}}{I_{datasheet}}\right) \tag{3.16}$$

where E is the energy, which can be E_{on}, E_{off} or E_{sw}, the sum of the two; and $V_{datasheet}$ and $I_{datasheet}$ are the voltage and current levels in the device's datasheet at which the energies were assessed. In this fashion, an estimation of the switching energy losses under arbitrary operating conditions can be determined.

The switching power loss is the product of the total switching energies and the switching frequency and can be written as,

$$P_{sw} = f_s E_{tot} = f_s\left(E_{sw} + E_{rr}\right) \tag{3.17}$$

where E_{rr} is the reverse recovery loss associated with the discharging of the energy stored in the freewheeling diode's capacitance during turn-off. The most formal expression of the reverse recovery loss is,

$$E_{rr} = \int_0^{t_{rr}} V_{DS}(t) I_{rr}(t) dt \tag{3.18}$$

wherein t_{rr} is the reverse recovery time; and I_{rr} is the reverse recovery current. This

expression is difficult to handle, however, as it requires knowing exactly the waveforms, which are heavily dependent upon the intrinsic behaviour of each device. An approximation can be made that assumes the losses to be represented by two triangles, with the losses dominated by the second half of the interval. This is written as,

$$E_{rr} \approx Q_{rr} V_{rr} \approx \frac{I_{rr} t_{rr}}{4} \tag{3.19}$$

where Q_{rr} is the reverse recovery charge; V_{rr} is the peak transient voltage during turn-on; and I_{rr} is the peak reverse recovery current. Many alternative methodologies exist for calculating the reverse recovery energy and, indeed, there is no truly exact method other than (3.18). However, since it requires measurements to determine and depends heavily on the design of the circuit, estimates are necessary.

The conduction losses are the summation of the losses in both the switch and the diode, should one be present. Most power electronic applications have need of one to enable reverse currents to flow. The losses within a power switch's package depend on what type it is and the specific application. For a MOSFET, it inherently has a body diode and that must be calculated by default. For IGBTs and BJTs, freewheeling diodes are not inherently present and must be added, either within or outside the confines of the package. The most general definition of the conduction losses for a transistor without a diode can be expressed as (3.20).

$$P_{cond,Q} = \frac{1}{T} \int_{t_{on}}^{t_{on}+DT} v_{DS}(t) i_{DS}(t) dt \tag{3.20}$$

For a MOSFET, however, the primary conduction loss generating mechanism is the on-state resistance; hence, the RMS value of the current needs to be calculated.

For a BJT or IGBT, the DS subscripts would be replaced by CE and the average current would need to be computed. Under SPWM operation, the solution RMS current in the switch is calculated by (3.12). The conduction losses of a MOSFET can then be computed as (3.21).

$$P_{MOSFET} = R_{DS(ON)} I_{Q,RMS}^2 \tag{3.21}$$

The on-state resistance, $R_{DS(ON)}$, is dependent upon the junction temperature, which itself is determined by the power losses incurred. In this work, the resistance is assumed to be fixed and is always taken at the value in the datasheet listed at high temperature, thereby removing an additional degree of complexity.

The general expression for the conduction losses of a diode are calculated by (3.22).

$$P_{diode} = \frac{1}{T} \int_0^{t_{on}} v_F(t) i_F(t) dt \tag{3.22}$$

Again, due to the necessity of having a waveform to calculate the value of the integral from, an approximate closed-form expression can be used. The forward voltage can be determined as,

$$V_F = V_j + r_d I_{D,RMS} \tag{3.23}$$

where V_j is the voltage across the pn junction; and r_d is the diode's dynamic on-state resistance, defined as the rate of change of voltage over current, $\frac{dV}{dI}$. The exact value of V_j is difficult to determine and requires an understanding of the exact structure of the device.

The power losses of a diode under such a model can be calculated as,

$$P_{diode} = V_j I_{D,avg} + r_d I_{D,RMS}^2 \tag{3.24}$$

where $I_{D,avg}$ and $I_{D,RMS}$ are calculated in (3.13).

This power loss is highly dependent upon the specific traits of the diode and whether the diode is actually seeing use. Depending on the application, the diode–added or the parasitic body diode of a MOSFET–may not see use (e.g. a bidirectional boost converter). An approximation that is useful for devising a generalised loss estimation where the dynamic resistance of the diode is neglected is given by (3.25).

$$P_{diode} \approx V_F I_{D,avg} \tag{3.25}$$

In this case, V_F can be considered to be a constant value from the device's datasheet or taken to rise linearly with current, per the provided current-voltage characteristic.

Altogether, this allows for the calculation of the total losses for a single MOSFET to be calculated as (3.26).

$$P_{cond} = P_{MOSFET} + P_{diode} \tag{3.26}$$

The total losses over a full switching period when supplying an arbitrary load with a transistor, independent of type, can be written as (3.27).

$$P_{loss} = P_{sw} + P_{cond} \tag{3.27}$$

Lastly, the losses of a three-phase inverter can be calculated as (3.28). It is a multiplication by three as opposed to six because only three switches at a time will be switching and conducting.

$$P_{loss,3\phi} = 3P_{loss} \tag{3.28}$$

Under SPWM operation, the output apparent power of a three-phase inverter, with no voltage drops subtracted, can be expressed as (3.29).

$$S_{3\phi} = \sqrt{\frac{3}{2}} V_{DC} I_{\phi,RMS} M \tag{3.29}$$

The power delivered to the load is the real component of the apparent power; hence, (3.29) can be rewritten as (3.30).

$$P_{3\phi} = \sqrt{\frac{3}{2}} V_{DC} I_{\phi,RMS} M \cos\phi \tag{3.30}$$

The efficiency of the inverter is the ratio of output power to input power. The input power is the summation of the output power and the power lost in the conversion process, as given by (3.31).

$$\eta = \frac{P_{out}}{P_{in}} = \frac{P_{3\phi}}{P_{3\phi} + P_{loss,3\phi}} \tag{3.31}$$

In total, this analysis allows for the losses of a converter to be estimated and the efficiency determined. The losses determine if a given transistor is feasible for an application and influences strongly the type and size of the cooling method.

3.4 Power Electronic Converter Optimisation

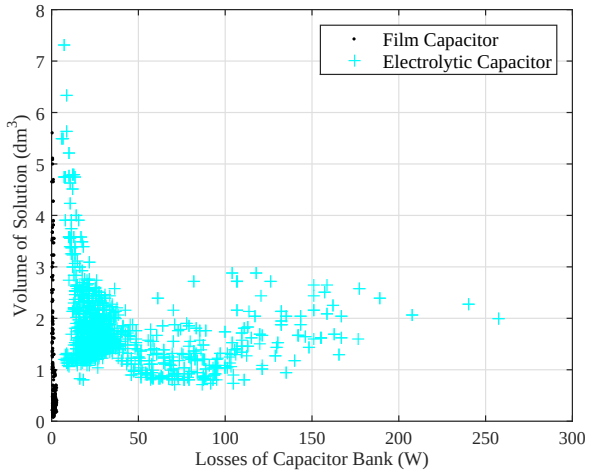
The notion of optimality in a design is integral to achieving a high power density and ensuring that the converter is neither oversized nor undersized; that is to say, it is appropriately designed for the given application. Three approaches to a discrete optimisation problem are outlined which provide several avenues by which it may be solved.

3.4.1 Convex Optimisation

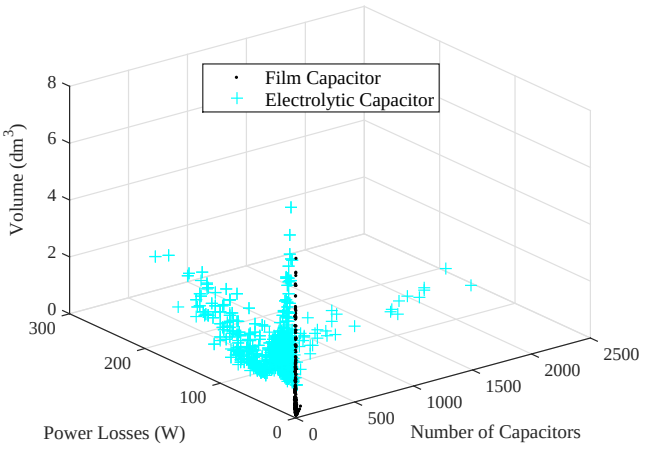
As a note, the figures presented in this subsection are for a self-built database of commercially available capacitors. The capacitor bank construction ideas presented in section 4.3.2 are used, along with the specifications of the designed inverter in chapter 4, to generate the plotted data. The goal of this subsection is to introduce the idea of convex optimisation and to attempt to reformulate a non-convex problem in a convex fashion, allowing for efficient algorithms to be used to find the global minimum. While the ideas are applied to capacitor data, nothing stops it from being used on other, similar problems.

Convexity is the holy grail when tackling an optimisation problem. A convex function, or set, has a unique global minimum that can be found efficiently via many well-established algorithms. For power electronics, however, convexity is seldom found in the problem itself and, even with significant simplification and the employment of many assumptions, it is not guaranteed to be found, nor is the integrity of the original problem guaranteed to remain. In the case of component selection, the data is discrete and, therefore, highly non-convex and, quite often, without a discernible pattern. Such an example can be found in Figure 3.11, which shows an arbitrary plot of

the characteristics of commercially available capacitors. For other components, such as transistors and inductors, similar results can be expected. Film and electrolytic capacitors are explicitly plotted to allow for quantitative decision making on which type to use.



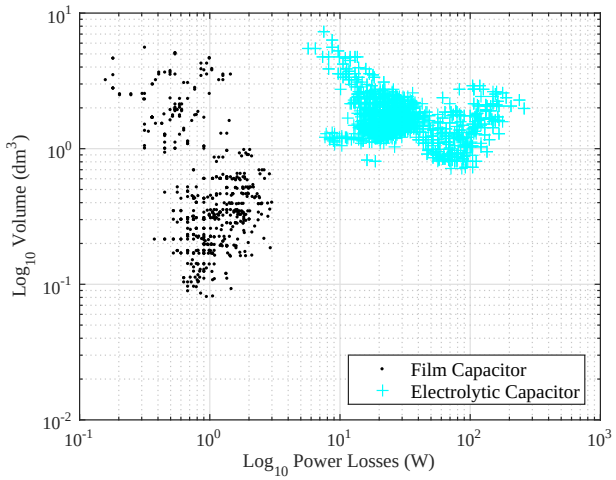
(a) 2D plot of capacitor bank losses and volume.



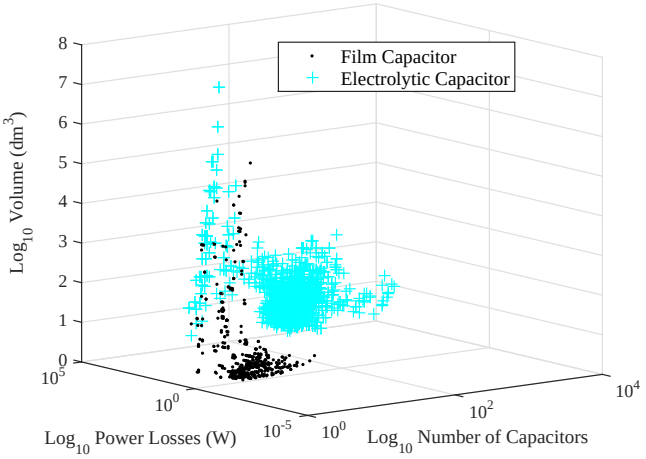
(b) 3D plot of losses, volume and number of capacitors.

Figure 3.11: 2D and 3D plots illustrating non-convex, random nature of data.

It is clear that to optimise this function in a convex fashion is an exceedingly



(a) 2D plot of capacitor bank losses and volume.



(b) 3D plot of losses, volume and number of capacitors.

Figure 3.12: Log-log plots of the data presented in Figure 3.11.

challenging problem. Following from the properties of convex functions, it is known that the data is not logarithmically convex; however, it is a useful exercise to plot it logarithmically to see if any immediate conclusions can be drawn to simplify the problem. Log-log plots of the same data are presented in Figure 3.12.

The immediate result of the logarithm operations is that the difference between

film and electrolytic capacitors, in this particular case, are striking: there exists a strong boundary between the two, where the film capacitors have a smaller volume and power loss. With the goal being to minimise the objectives presented on the axes, it becomes obvious that electrolytic capacitors do not lend themselves to this task. A simplification of the problem can be made, then, that involves disregarding electrolytic capacitors, thereby reducing the size of the problem drastically.

Though the problem is smaller, the issue of non-convexity of the dataset itself is not resolved. A series of relaxations can be applied to make the set continuous and convex, allowing for the interior to be scanned in a robust fashion to find the global minimum.

The first relaxation to be made is to remove the restriction on the values that the data may take on. For example, the total number of capacitors must be an integer, as the series and parallel requirements are forced to be integers by the ceiling operator. Physically, this makes perfect sense: two-thirds of a capacitor cannot be purchased and integrated; it is either a whole object or none at all. Therefore, the initial relaxation is to allow the number of capacitors, N, which is the product of the series and parallel quantities n_s and n_p, to be continuous over all positive, non-zero numbers; hence,

$$\{N|N \in \mathbb{Z},\ N > 0\} \rightarrow \{N^*|N^* \in \mathbb{R},\ N^* > 0\} \tag{3.32}$$

where N^* is the relaxed variable. This is a reasonable relaxation to make as, should an unacceptable result arise, it can be disregarded and the next best realisable one can be taken. Alternatively, if the best result lies in an inadmissible region, then a distance metric can be used to decide upon which to take in a localised region. These

can involve the 1-, 2- or ∞-norm. Whichever capacitor minimises the value of the selected norm would then be the optimal device. The definition of an arbitrary norm is,

$$\|x\|_p = \left(\sum_{i=1}^{n} |x_i|^p \right)^{1/p} \tag{3.33}$$

where x is a vector of values; and p is the value of norm desired, where the most regularly employed ones are the 1-norm (summation of absolute values), the 2-norm (Euclidean norm) and the infinity-norm (maximum value).

The next, and most significant, relaxation to be made is to allow every design variable in the set, D, to be able to take on any real value. That is to say,

$$\{D \mid D \in \mathbb{R}\} \tag{3.34}$$

where negative quantities can be easily disregarded as inadmissible, as they would make no physical sense.

With these relaxations in hand, the discrete problem has been transformed in to a continuous one. While the data itself remains highly non-convex, an operation can be applied to try to bind the set in a convex fashion. This approach takes advantage of the idea convex hull, Co, defined in (3.35).

$$Co(D) = \cap\{D^* \mid D \subseteq D^*,\ D^* \text{ convex}\} \tag{3.35}$$

The convex hull finds the most exterior points and connects them so that the bounded set is convex. The simplest means of binding would be linearly. Like this, the problem can then be written as the minimisation of some function subject to

linear constraints; i.e.,

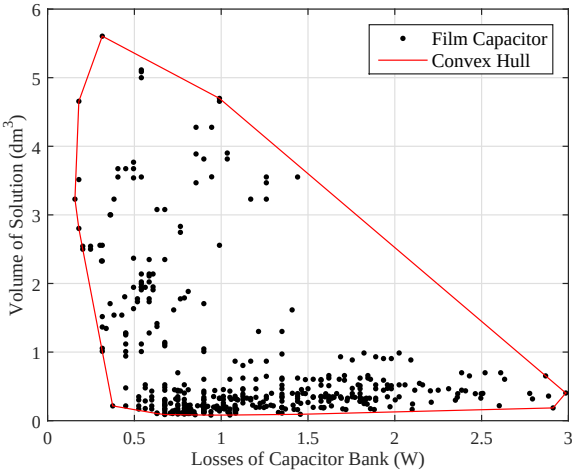
$$\begin{aligned} \underset{x}{\text{minimize}} \quad & c^T x \\ \text{subject to} \quad & Ax \leq b \end{aligned} \tag{3.36}$$

This formulation lends itself to optimisation via linear programming, some form of interior point method, or even a basic algorithm which moves around the periphery of the set and chooses the smallest encountered value. The convex hull applied to the previously presented data is shown in Figure 3.13.

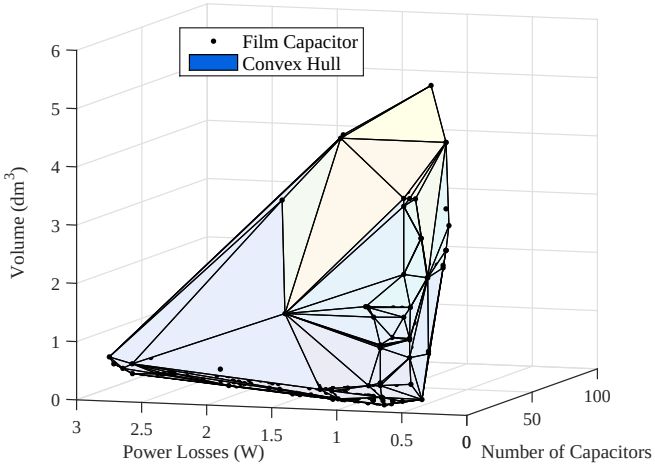
A serious problem in seeking a convex solution is that, as a result of the nature of the dataset, the problem to be minimised is highly non-convex. The previous simplifications have alleviated this to an extent, allowing for a convex representation to be possible; however, no clear function, let alone a convex one, can be deduced from the presented data. It is at this point where a function must be introduced to proceed in a convex fashion. This function can be of a simple nature, such as a cost function to tie as many variables together as possible, where the greatest weight is placed on a parameter that should be minimised; alternatively, it could be obtained via curve fitting techniques. Depending on the nature of the data, a representative function can be built and operated upon.

3.4.2 Heuristic Optimisation

Heuristic optimisation tends to find use when a problem is too computationally expensive or even impossible to solve using classical techniques. Heuristic algorithms search for a minimum (maximum) by starting with an initial guess and eventually improving upon it until a solution is found. This solution is not guaranteed to be the global minimum, though it tends to find a result that is satisfactory. The found



(a) 2D convex hull with data points.



(b) 3D convex hull with data points.

Figure 3.13: 2D and 3D plots illustrating the convex hull on a reduced dataset shown in Figure 3.11.

solution can be a starting point for a classical method or used as the next initial guess for the heuristic algorithm, running again until a better solution is found.

Many heuristic algorithms exist that work well under certain circumstances. Evolutionary algorithms–of which the Genetic Algorithm (GA) is a member–are very

popular, though seemingly not well suited for a discrete problem such as component selection. A review publication outlined many techniques for discrete optimisation (Arora *et al.*, 1994), including the GA, and simulated annealing was found to fit best within the confines of the problem at hand. Other evolutionary algorithms, when reviewed, did not have the same fit and, thus, were not considered in great detail (Elbeltagi *et al.*, 2005).

Depending on the goal, however, some evolutionary algorithms do fit within the confines of a discrete optimisation problem. For example, Particle Swarm Optimisation (PSO) has been shown to perform well for calculating the coefficients of a B-spline for surface reconstruction (Gálvez and Iglesias, 2012). A continuous surface could be evaluated over using classical and numerical techniques to find local or global minima, blending heuristic and classical techniques.

Simulated Annealing

Simulated annealing is a heuristic optimisation technique that uses stochastic methods to converge to a "good enough" solution. A thorough treatment of the subject can be found in (Ingber, 1993), (Dekkers and Aarts, 1991) and (Bertsimas and Tsitsiklis, 1993). A simplified explanation follows, highlighting key aspects and results that are beneficial for optimising datasets.

The simulated annealing algorithm is designed to mimic nature's tendency to favour lower energy states. The process of annealing involves heating up a piece of metal and allowing it to slowly cool. During the cooling process, some defects can be eliminated, allowing the metal to reach an overall lower energy state. Simulated

annealing is a computerized version that "heats up" a function and, eventually, converges to a maximum (minimum). The most popular formulation, for maximisation, is presented in (3.37). Minimisation would require a reversal of the decision making process. The condition to check and the decision to be made are,

$$p(T) = \begin{cases} \exp\left(-\left(\frac{E_{i+1}-E_i}{T}\right)\right), & \text{if } E_{i+1} - E_i \leq 0 \\ 1, & \text{if } E_{i+1} - E_i > 0 \end{cases} \tag{3.37}$$

where E_{i+1} and E_i are the next energy state and current energy state, respectively; T is the temperature; and $p(T)$ is a value, over the range [0,1], which is used in tandem with a probability function for escaping local maxima. The result from (3.37) is compared to a number drawn from a probability distribution–normally the uniform distribution–and a decision is made, per (3.38),

$$E = \begin{cases} E_{i+1}, & \text{if } p(T) \geq \rho \\ E_i, & \text{if } p(T) < \rho \end{cases} \tag{3.38}$$

with ρ being the number drawn from the preferred probability distribution. The comparison of p with ρ allows for local maxima to be escaped from by allowing the algorithm to move to a higher energy state, in the hopes that it will eventually find a greater maximum.

One of the biggest questions with this algorithm is how the "neighbour," E_{i+1}, is to be selected. Ideally, the next point should be near the current point, E_i, for a guided movement in a function with a coherent structure. In the case of a seemingly random set of data, this logic does not necessarily need to be maintained, though it makes

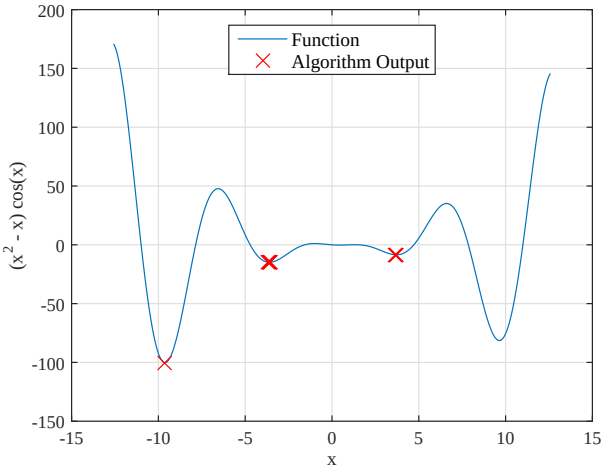
sense to for generality's sake. Neighbour selection can take on a number of forms: completely random, a fixed step from the current point, or temperature dependent. Temperature dependency is likely the most robust, allowing for the likelihood of movement to be tied to the level of progress yet to be made. That is to say, if the algorithm is near the beginning (i.e. T is large), then the neighbour has the possibility of being relatively far away from the current point. Conversely, if T is small, it implies the algorithm is near its end and it would not make sense to look too far away, under the assumption that it has already converged to–or is close to converging to–a minimum. The neighbour is selected as,

$$n_{i+1} = n_i + X \cdot T \tag{3.39}$$

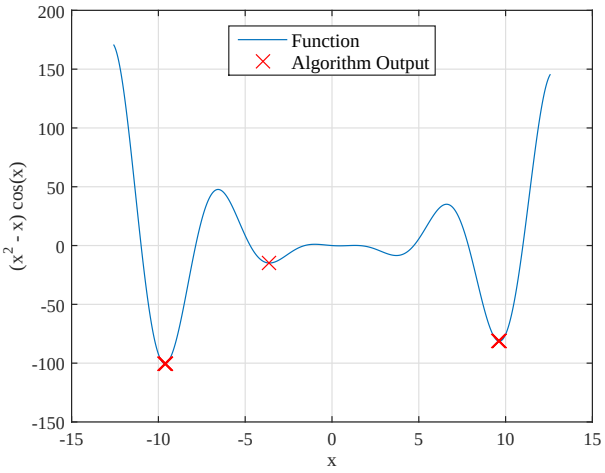
where n is the current position in the data set; X is a random variable, drawn from a probability distribution of choice, with adjustments made, depending on the probability distribution, to allow for negative values, thereby enabling backwards movement in the dataset; and n_{i+1} is the neighbour to be explored. A Gaussian distribution, for example, would be biased towards its mean, whereas a uniform distribution would have less predictable movement. In theory, as the temperature is lowered, an optimal solution should be approached; hence, at low T, movement when $E_{i+1} < E_i$ is not favoured and the algorithm breaks down in to the greedy algorithm, whereby the program moves to maximize (minimize) the value in question.

An example of simulated annealing for minimisation run on a continuous test function is shown in Figure 3.14. In a), the initial temperature, T_0 is 20K, and in b) it is 50K. When the initial temperature is lower, the minima found are more evenly balanced throughout the function. This is a result of the temperature dependency

built in to the neighbour selection, as well as the algorithm having more time to move around before collapsing in to the greedy algorithm. Such a dependency is a highly beneficial property to employ as, in *b*), the global minimum is found quite regularly, along with a local minimum that is not significantly different from the global one.



(a) Simulated annealing with $T_0 = 20$K.



(b) Simulated annealing with $T_0 = 50$K.

Figure 3.14: Ten runs of the simulated annealing algorithm on the test function with different initial temperatures.

3.4.3 Pseudo-Optimality

Pseudo-optimality is the process of finding the best solution within a dataset without using any explicit optimisation technique. This differs significantly from heuristic optimisation, where a "good enough" solution is found by some well-defined algorithm requiring minimal human interference. Pseudo-optimality uses many approximations and metrics and attempts to make a side-by-side comparison with a high level of designer influence being present.

Pseudo-optimality can be used to describe the component selection process when designing an electronic circuit. In this problem, the best component is sought by manually sifting through a large amount of data. Metrics, such as the figures of merit described in section 2.5 or the linearised loss analysis in section 3.3, can be used to filter down the results and enable assessment of a dataset of reduced-order. It is intuitive as it requires no particular algorithm or exceptional handling to be devised: The designer simply looks for parts and, once satisfied, stops the search with what is deemed to be best in his or her opinion.

3.5 Parasitics Analysis

The parasitic parameters of each component and interconnection mechanism are significant drivers in the performance of a power electronic converter. To achieve the best results, both in terms of efficiency and electromagnetic compatibility, the stray inductance and capacitance of the commutation loop need to be well understood and integrated in to models.

The estimation of parasitic parameters varies wildly in terms of difficulty. In the

case of basic geometries, such as round or rectangular conductors of constant cross section, the results are well disseminated, even in the case of parallel conductors, where mutual coupling has an effect (Rosa, 1908). Outside of these basic cases, however, analytical techniques break down and become either prohibitively difficult or unacceptably inaccurate. Hence, finite element simulations become the preferred method for obtaining accurate results.

This does not preclude a preliminary analysis from being useful in guiding the construction of the interconnection scheme or understanding best practices; indeed, at the core of every complicated design are fundamental principles that impact performance. In this section, these principles are discussed for a pair of parallel conductors in a simple, two-conductor fashion, that most closely resembles a bus bar. A printed circuit board (PCB) is a subset of a bus bar; hence, the analysis remains valid, when operating with the same restrictions.

For clarity's sake, a generic drawing of parallel rectangular conductors is provided in Figure 3.15.

3.5.1 Current Density

The distribution of current in a conductor is the driving force behind the parasitic resistance and inductance; therefore, a brief treatment of the subject is necessary before delving in to an analysis of the parasitic parameters.

In a long conductor with a constant cross section transmitting current, the DC current density can be expressed as (3.40).

$$J_{DC} = \frac{I_{DC}}{wt} \tag{3.40}$$

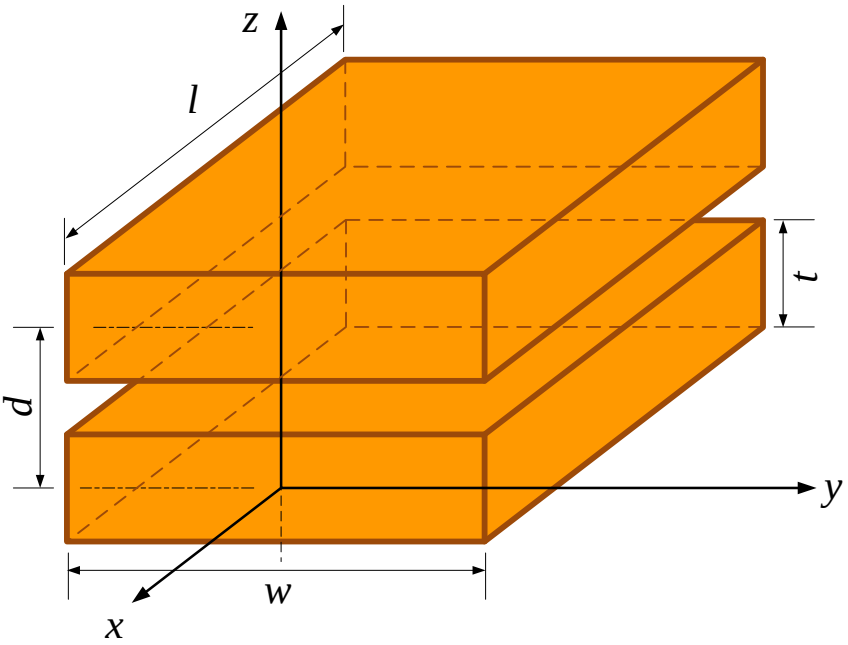


Figure 3.15: Reference drawing of parallel conductors with dimension notations.

Once the cross section changes and a sink for the current is defined, the DC current density strays from what (3.40) suggests. An example of this can be seen in Figure 3.16, where sets of IGBT module terminals are shorted together to form a closed loop for current flow. The IGBT terminals closest to the DC inputs see the most current, whereas the ones farthest away see significantly less. The current density is not the same over any arbitrary cross section.

The current density over a long conductor of constant cross section transmitting AC current can be described as,

$$J(z) = J_s e^{-\frac{z}{\delta}} \tag{3.41}$$

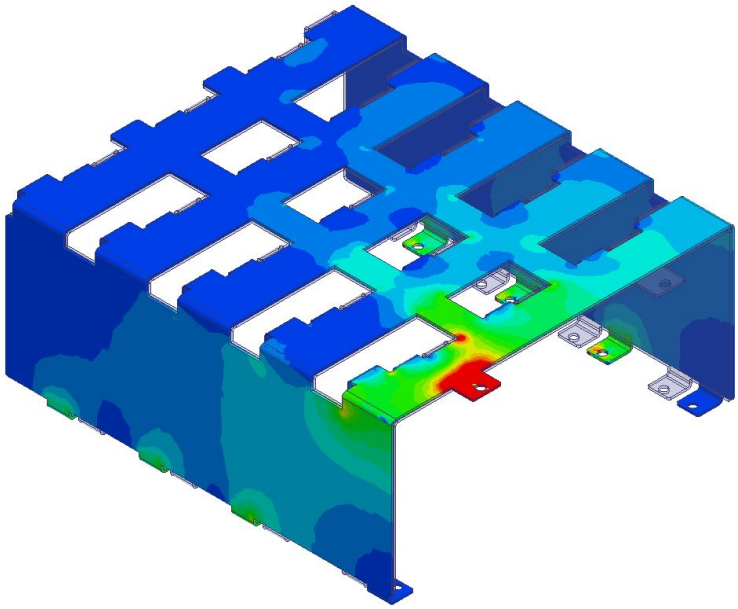


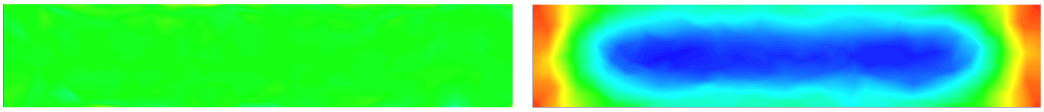
Figure 3.16: DC current density of a copper bus bar.

where J_s is the current density at the surface of the conductor, d is the penetration depth from the surface and δ is the skin depth, as described in (3.42). The skin depth is defined as the level of penetration electromagnetic waves may achieve without attenuating by a factor of e^{-1} and is calculated as,

$$\delta = \frac{1}{\sqrt{\pi f \mu \sigma}} \tag{3.42}$$

wherein f is the frequency of the wave; μ is the total permeability of the material, the product of the relative permeability of the material and the permeability of free space ($\mu = \mu_r \mu_0$); and σ is the conductivity of the conducting material.

A comparison of DC and AC current densities over a rectangular transmission line can be seen in Figure 3.17. In the DC case, the current is uniformly distributed throughout the conductor; however, in the AC case, the current peaks at the surface



(a) DC current density.

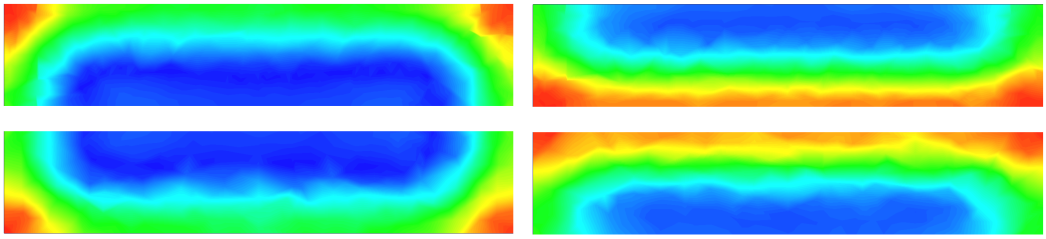
(b) AC current density, f=10kHz, illustrating the skin effect.

Figure 3.17: DC and AC current densities on a copper transmission line with a width and thickness of 10 and 2mm, respectively.

and, particularly, along the z-axis edges. This result diverges from (3.41) though, at the centre of the conductor, it matches reasonably well.

The proximity effect is less intuitive. Physically, the proximity effect is a result of fundamental electromagnetic laws that cause eddy currents to be generated in nearby conductors when exposed to time-varying magnetic fields. Conceptually, it can be likened to a sort of electromagnetic equilibrium within the conductor where the impedance is equal at every distance d: the current rising to the surface of one conductor reduces the impedance on the surface of the other conductor which, in turn, causes an increase in the surface current of the first. This exchange continues until an equilibrium is achieved. Visually, the proximity effect exacerbates the current crowding phenomenon at the surface of the conductor that began with the skin effect. Depending on whether the currents in the parallel conductors are in the same or opposing directions, the current would either be pushed away (same direction) or pulled together (opposing directions). Prototypical examples are presented in Figure 3.18.

Representing the proximity effect numerically is a challenging task. One approach is to use an expression for the current density in two parallel plates that meshes the skin and proximity effects, such as (3.43) (Kazimierczuk, 2009); however, this relies on several assumptions and, for complex geometries, it becomes time consuming and



(a) AC current densities with currents in the same direction.

(b) AC current densities with currents in opposing directions.

Figure 3.18: AC current densities illustrating the proximity effect on a copper transmission line with a width, thickness and separation of 10, 2 and 0.5mm, respectively.

prone to error. Nevertheless, it is useful for understanding the coupled effects of the skin and proximity effects on parallel conducting planes.

$$J(z) = -\left(\frac{\gamma I}{w}\right)\frac{\cosh\left(\gamma\left(z+\frac{t}{2}(-1)^p\right)\right)}{\sinh(\gamma t)} \tag{3.43}$$

In this expression, $\gamma = \frac{1+\mathrm{j}}{\delta}$, which relates the real and imaginary components of the alternating current to the skin depth; I is the current being passed through the conductor; t is the thickness; w is the width; and p is a number, either 1 or 2, which is used to determine if the currents are in the same direction ($p = 1$) or opposing directions ($p = 2$).

The AC current density in a real design, similar to the DC current density, does not match the governing equations exactly. An example of AC current flow from a single IGBT phase leg to the DC-link capacitors is shown in Figure 3.19. Again, over an arbitrary cross section, the current density does not follow the expected distribution from the equation; furthermore, it diverges from what is shown in Figure 3.18, as the current is not flowing through a uniform conductor to a single sink.

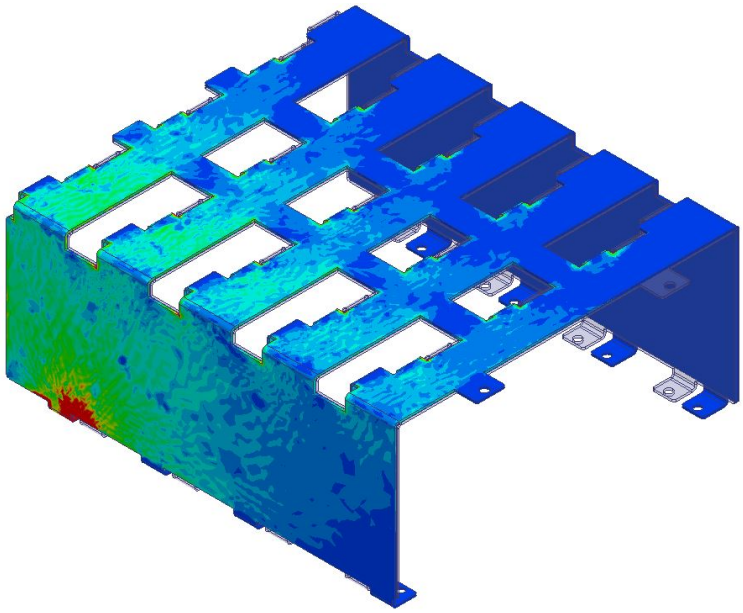


Figure 3.19: AC current density of a copper bus bar with f_s=10kHz.

All these effects combined make it clear that finite element simulations are required to truly understand the current density distribution–and, hence, the parasitic parameters–through the conducting medium.

3.5.2 Resistance

The resistance is a fundamental property of a conductor. It dictates the voltage drops and power losses of the system, causing voltage regulation on the line and heat generation. The DC resistance over a long, uniform conductor can be calculated as,

$$R_{DC} = \rho_e \frac{l}{wt} \tag{3.44}$$

where ρ_e is the electrical resistivity of the conducting material.

When AC currents enter the discussion, the resistance changes, following from

the current density. With the majority of current flowing through a region nearer the surface of the conductor, the skin depth becomes an important parameter. The computation of the AC resistance for an isolated conductor can then be determined as (3.45).

$$R_{AC,\delta} = \frac{\rho l}{2w\delta}\left(\frac{\sinh\left(\frac{t}{\delta}\right)+\sin\left(\frac{t}{\delta}\right)}{\cosh\left(\frac{t}{\delta}\right)-\cos\left(\frac{t}{\delta}\right)}\right) \tag{3.45}$$

This expression is rather complicated and involves a number of terms; however, a simplification can be made: If the ratio of thickness to skin depth is much greater than unity–$\frac{t}{\delta} \gg 1$–then (3.45) can be simplified to (3.46). As this ratio increases, the bracketed term tends to unity and has no impact.

$$R_{AC,\delta} \approx \frac{\rho l}{2w \cdot \delta} \tag{3.46}$$

When a parallel plate is present, the proximity effect arises and further changes the resistance by increasing the current crowding near the surface of the conductor. This phenomenon can be expressed as (3.47).

$$R_{AC} = \frac{\rho l}{w\delta}\left(\frac{\sinh\left(\frac{2t}{\delta}\right)+\sin\left(\frac{2t}{\delta}\right)}{\cosh\left(\frac{2t}{\delta}\right)-\cos\left(\frac{2t}{\delta}\right)}\right) \tag{3.47}$$

The same simplification when going from (3.45) to (3.46) can be applied when the thickness is much larger than the skin depth.

Table 3.1 presents the simulated and calculated resistances for the bus bar shown in Figure 3.19. The calculated resistance is approximately half that which is obtained via simulation, which is likely a result of the current crowding at certain junctions and the simplifying assumption that each surface is a continuous plane. The accuracy could be enhanced by attempting to take in to account these choke points; however,

this would still rely heavily on assumptions regarding the current density distribution and, hence, is still lacking in overall accuracy.

3.5.3 Inductance

The inductance of the interconnection scheme has several adverse effects. It slows the transition times of signals, incurring higher switching losses; it gives rise to transient voltage spikes, which can damage components in the circuit; and it causes noise to radiate from the system, possibly coupling in to other circuits and affecting them. Its approximation is important for enhancing the performance of a converter.

The self-inductance of an isolated rectangular plate under DC operation can be calculated using expressions from (Rosa, 1908).

$$L_{self} \approx 2l \left(\ln \left(\frac{2l}{w+t} \right) + 0.5 + 0.2235 \left(\frac{w+t}{l} \right) \right) \times 10^{-6} \tag{3.48}$$

In the case of parallel plates, the interaction between the magnetic flux emitted by the currents passing through the system cause a coupling between conductors, called the mutual inductance, and is calculated as,

$$M \approx 2l \left(\ln \left(\frac{2l}{d} \right) - 1 + \frac{d}{l} \right) \times 10^{-6} \tag{3.49}$$

with d being the centre-to-centre distance of the conductors, in millimetres.

Depending on the direction of flow of the currents, the mutual inductance can either increase (same direction) or decrease (opposite directions) the total inductance

of the conducting arrangement. This is expressed as (3.50).

$$L_{total} = 2\left(L_{self} + (-1)^{p-1}M\right) \tag{3.50}$$

The preceding equations are valid only in the DC case. As the frequency of the currents increases, they rise to the surface, enhancing the mutual coupling between the conductors, thereby reducing the total inductance of the arrangement. However, this reduction in inductance comes at the cost of increased resistance.

Neglecting the case where only the skin effect is present, the inductance of two parallel plates with opposing currents can be calculated as (3.51).

$$L_{AC} = \frac{\rho l}{2\pi f w \delta}\left(\frac{\sinh\left(\frac{2t}{\delta}\right) - \sin\left(\frac{2t}{\delta}\right)}{\cosh\left(\frac{2t}{\delta}\right) - \cos\left(\frac{2t}{\delta}\right)}\right) \tag{3.51}$$

As the frequency increases, as the analytical expression indicates, the inductance decreases. Table 3.1 provides the results of calculations and simulations for the inductance of the bus bar shown in Figure 3.19 The analytical expression, when assuming current flows uniformly from IGBT terminals to the capacitors and back without employing the third surface, grossly underestimate the inductance of this particular structure. Analytical techniques fail to capture the true behaviour.

3.5.4 Capacitance

The capacitance of a pair of parallel conductors can be calculated in the same fashion as a parallel plate capacitor,

$$C = \varepsilon_0 \cdot \varepsilon_r(f)\left(\frac{l \cdot w}{d}\right) \tag{3.52}$$

Table 3.1: Simulated and calculated AC parasitic parameters of the bus bar shown in Figure 3.19.

Frequency (kHz)	Inductance (nH)		Resistance ($\mu\Omega$)	
	L_s	L_c	R_s	R_c
10	13.90	1.04	193.88	62.69
20	13.14	0.72	263.90	90.74
30	12.80	0.59	318.10	110.81
40	12.59	0.51	363.95	127.87
50	12.45	0.46	404.42	142.98
60	12.35	0.42	441.04	156.63
70	12.26	0.38	474.75	169.19
80	12.20	0.36	506.15	180.87
90	12.14	0.34	535.64	191.84
100	12.10	0.32	565.55	202.22

where ε_0 and $\varepsilon_r(f)$ are the permittivity of free space and the relative permittivity of the dielectric material being used, respectively. The frequency dependence of the dielectric can be found in the material's corresponding datasheet.

3.5.5 Parasitic Interactions

From the preceding discussions, the means of calculating the parasitic parameters in a conducting medium have been identified. Their interaction with one another impacts the quality of signals transmitted through the medium. Two final points to consider are the characteristic impedance and the resonant frequency of the conductor.

The characteristic impedance can be calculated as,

$$Z_0 = \sqrt{\frac{R + j\omega L}{G + j\omega C}} \tag{3.53}$$

where G is the transconductance of the dielectric material. If R and G are small

enough so as to be ignored–which is a fair first estimate–then the characteristic impedance becomes the square root of the ratio of inductance to capacitance.

As the inductance decreases, so, too does the characteristic impedance; however, by reducing the inductance via smaller spacing, the capacitance increases, which further decreases it. A low characteristic impedance is beneficial to radiated emissions as it minimises the magnitude of reflections which is believed to help in reducing radiated EMI (Atmel, 2014). To achieve a low Z_0, the conducting plates should be tightly coupled, resulting in low inductance and a high capacitance.

However, this perspective changes when considering resonance. The resonant frequency of a system, assuming it is connected only to itself, occurs when the capacitive and inductive reactances are equal. It can be calculated by (3.54).

$$\omega_0 = \sqrt{\frac{1}{LC}} \tag{3.54}$$

The resonant frequency should be sufficiently high such that it should not be activated with a signal or harmonic of high magnitude. In reducing the inductance via tight coupling of the conductors, the capacitance increases in turn, causing a reduction in the resonant frequency and increasing, depending on the system, the probability of it being triggered and adding significant noise. For power electronic applications, this frequency is normally in the high megaHertz and is not normally of concern. The resonant frequency of a bare PCB and the assembled inverter are shown in section 5.1 and is observed in the tens of megaHertz.

3.6 Summary

In this chapter, the necessary analysis for power electronic converter design is outlined. A thorough review of previous studies came to the conclusion that a high fidelity model of the switching losses is not required for turning out a well-designed converter, leading to the decision to analyse the losses via the popular linearised inductive switching model. In selecting a modulation strategy, the currents that influence the switching and conduction losses can be obtained, allowing for an estimation of the converter's losses.

The idea of optimality in a design for maximising power density is discussed and the necessity for such complexity is rationalised. An attempt at reformulating the highly non-convex problem of discrete component selection is attempted and a reasonable approach is found by using the convex hull. Other methods less likely to return the global minimum via heuristic techniques and the notion of pseudo-optimality are set out as a means of bypassing the convexity issues inherent to the problem.

The analysis of the parasitic parameters of a bus bar is introduced. The inductance, resistance and capacitance, in both the DC and AC cases, are discussed and expressions provided. The analysis also applies to a PCB, which is a subset of a bus bar. However, what is discussed only applies to uniform conductor cross sections with specific assumptions made, enabling current and potential distributions to be known. For complex geometrical structures, multi-layer designs–which a PCB is most likely to be–and with asymmetric conduction paths present and non-uniform distributions, finite element solvers become the most reliable means by which the parasitics can be analysed and the last iota of performance squeezed from a design.

Chapter 4

High Power Density Inverter Design

This section seeks to outline good practices to the design of a high power density converter, with a targeted application of a three-phase inverter. Specifications for the inverter are provided in Table 4.1.

Table 4.1: Three-phase inverter specifications.

Requirement	**Value**
Output power	$30kW$
DC-link voltage	$800V$
Load current	$30A_{RMS}$
Switching frequency	$100kHz$
Voltage ripple	$\leq 1\%$

4.1 Power Density

Power density is defined as the ratio of power transmitted to volume ($\frac{W}{dm^3}$).

$$\rho_p = \frac{P_{out}}{Vol} \tag{4.1}$$

A high power density can be achieved by driving the otuput power upwards or the volume downwards. Generally speaking, as the output power goes up, so, too, does the volume. This follows naturally when considering the loss-generating mechanisms: Conduction loss increases with current and the switching loss increases with both current and voltage; hence, as more power is transmitted (i.e. higher voltage and/or current levels), the power losses go up. As power losses increase, the size of the heat sink must increase so as to evacuate sufficient heat to maintain operation.

A tradeoff can clearly be observed when trying to maximise the power density: a converter can have a high output power, a low volume, or something in-between. An interesting study undertaken examined the effects of a power density-centric design, showing that increasing the switching frequency alone cannot lead to a sustained increase in power density via passive reduction (Biela *et al.*, 2009). Beyond a certain frequency, high frequency effects will begin to demand an increase in the size of the magnetic components, as well as an increase in losses that requires a larger heat sink, offsetting the overall reduction in passive component sizing to the point where the power density begins to drop.

Wide-bandgap materials are favourable to the endeavour of power density maximisation: for a given power loss, novel materials can switch faster, reducing the size of the passive components; alternatively, power losses can be reduced at the same

switching frequency, allowing for the often-bulky heat sink to be downsized. Wide-bandgap materials provide an extra degree of freedom to the design process and open up the possibilities to move to high frequency operation. Indeed, Gallium Nitride devices are seeing applications in excess of 1MHz (Reusch and Strydom, 2014, 2015) with high efficiency being maintained.

4.2 Switches

Switch selection is one of the major gates to pass through in a design. Its importance demands an appropriate selection, particularly if the converter is to be optimally sized for the application. This section will seek the best power transistor for the specification given in Table 4.1 from a set of components by applying ideas and modelling techniques outlined in chapters 2 and 3.

4.2.1 Device Figures of Merit

With a daunting selection of transistors available on the market, some tools must be used to assist in filtering out ones that are not desirable for a given design. This is where the figures of merit discussed in section 2.4 become useful: they allow for a comparison of the fundamental characteristics of a specific device and permit a balanced assessment of performance. The transistors in question are broken in to two groups: 600/650V, rated for 15kW operation, in Table 4.2; and 1200V, for 30kW operation, in Table 4.3. The current loading levels remain the same, which means that the DC bus voltage is cut in half for the half-power inverter. The calculated figures of merit for each respective case are presented in Tables 4.4 and 4.5.

Table 4.2: 600 and 650 Volt rated power transistors selected for analysis. Parameters are taken from their respective datasheets at elevated temperature.

Device	Type	Test Conditions	$R_{DS}(m\Omega)$	$V_{CE(sat)}$ (V)	E_{on} (mJ)	E_{off} (mJ)	E_{rr} (mJ)	V_F (V)	R_{th} (K/W)
SCT2120AF[1]	SiC MOSFET	400V/40A	15	-	1	0.4	≈ 0	3.1	0.2
IRGP4069D[2]	Si IGBT	400V/35A	-	1.9	0.709	0.929	0.304	1.4	0.32
HGTG30N60A4D[2]	Si IGBT	390V/30A	-	1.6	0.28	0.45	0.72	2.2	0.39
IXGH48N60C3C1[2]	Hybrid IGBT	400V/35A	-	1.8	0.37	0.57	≈ 0	1.8	0.56
STY112N65M5[1]	SJ MOSFET	400V/64A	43	-	2	2.5	2.6	1.5	0.34
STY139N65M5[1]	SJ MOSFET	400V/80A	84	-	2	2.5	2.6	1.5	0.34
STY145N65M5[1]	SJ MOSFET	400V/85A	22	-	2	2.5	2.6	1.5	0.34
PGA26C09DV[2,*]	GaN FET	400V/8A	150	-	-	-	≈ 0	2.5	1.5

[1] 650V device.
[2] 600V device.
* Preliminary datasheet. Not all information provided.

Table 4.3: 1200 Volt rated power transistors selected for analysis. Parameters are taken from their respective datasheets at elevated temperature.

Device	Type	Test Conditions	$R_{DS}(m\Omega)$	$V_{CE(sat)}$ (V)	E_{on} (mJ)	E_{off} (mJ)	E_{rr} (mJ)	V_F (V)	R_{th} (K/W)
C2M0025120D	SiC MOSFET	800V/50A	43	-	1.4	0.3	≈ 0	3.1	0.2
C2M0040120D	SiC MOSFET	800V/40A	84	-	1	0.4	≈ 0	3.1	0.2
IRG7PH42UD	Si IGBT	600V/30A	-	2.1	1.503	1.968	1.475	2.2	0.27
STGW40H120DF2	Si IGBT	600V/30A	-	2.4	1.81	2.46	0.94	3.05	0.38
GA35XCP12-247	Hybrid IGBT	800V/35A	-	3.9	2.66	4.35	≈ 0	3.5	0.27

As was touched upon in section 2.4, while figures of merit provide a good basis for comparison amongst devices of the same type, there exist challenges in applying them to a decision making process involving different types. Furthermore, they don't necessarily capture the operating characteristics of the converter topology. This requires a more in-depth form of analysis to determine which technology and switch is best for the application.

4.2.2 Linear Analysis of Devices

As previously laid out, the figures of merit do not necessarily paint a full picture. It becomes necessary, then, to move on to another form of analysis to make a definitive decision. In this case, the converter loss estimation method described in section 3.3 is employed to generate Figures 4.1 and 4.2, in an attempt to resolve which switch

Table 4.4: Device-specific FOMs for 600 and 650 Volt rated devices.

Device	Type	BHFFOM	NHFFOM	PDFOM	MOSFET FOM	IGBT FOM
SCT2120AF[1]	SiC MOSFET	5.59E+9	7.46E+10	1.28E+2	1.10E+8	-
IRGP4069D[2]	Si IGBT	-	-	2.36E+3	-	5.67E+2
HGTG30N60A4D[2]	Si IGBT	-	-	9.07E+3	-	1.39E+3
IXGH48N60C3C1[2]	Hybrid IGBT	-	-	3.97E+3	-	9.75E+2
STY112N65M5[1]	SJ MOSFET	1.25E+8	2.69E+9	3.15E+2	1.30E+8	-
STY139N65M5[1]	SJ MOSFET	1.61E+8	3.77E+9	3.04E+2	1.62E+8	-
STY145N65M5[1]	SJ MOSFET	1.61E+8	3.60E+9	3.23E+2	1.61E+8	-
PGA26C09DV[2,*]	GaN FET	2.45E+10	3.35E+10	1.56E+2	-	-

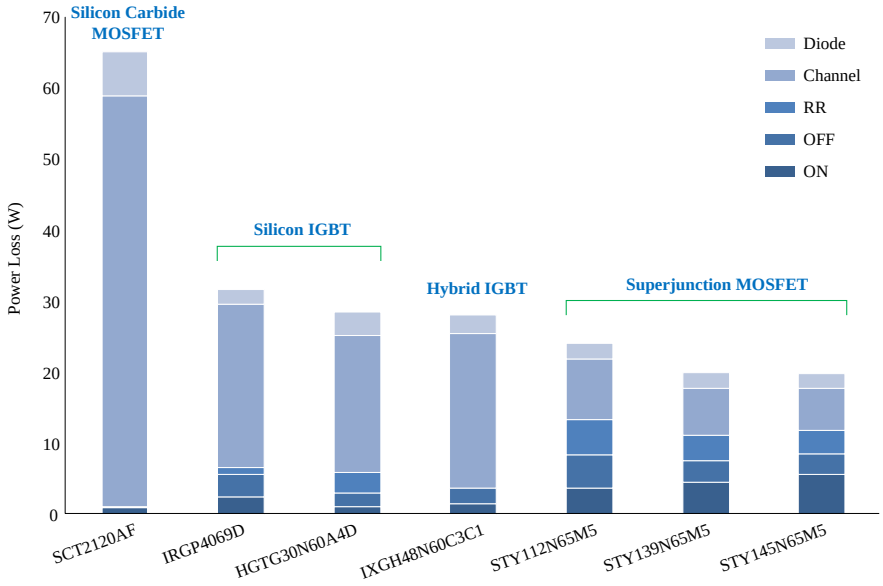
[1] 650V device.
[2] 600V device.
[*] Preliminary datasheet. Not all information provided.

Table 4.5: Device-specific FOMs for 1200 Volt rated devices.

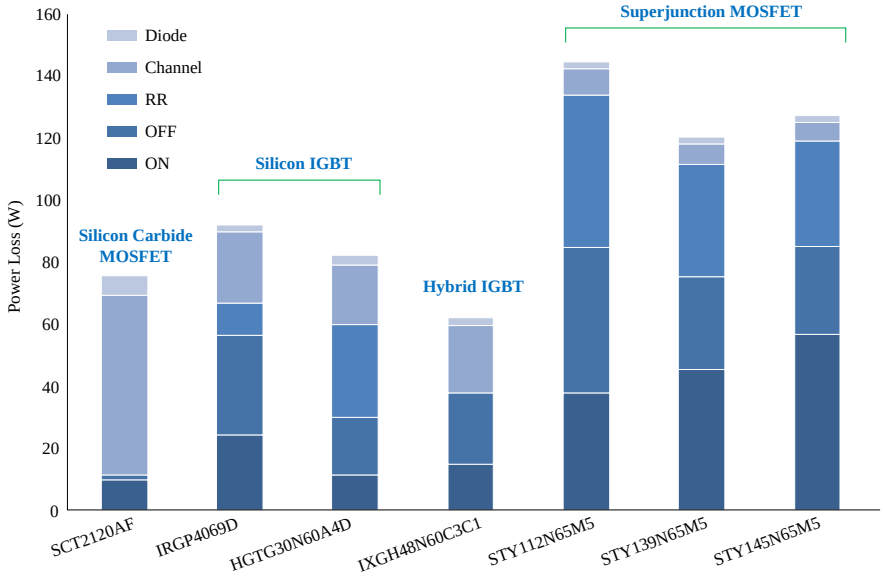
Device	Type	BHFFOM	NHFFOM	PDFOM	MOSFET FOM	IGBT FOM
C2M0025120D	SiC MOSFET	1.06E+8	8.34E+9	2.39E+2	1.44E+8	-
C2M0040120D	SiC MOSFET	7.94E+7	6.29E+9	1.41E+2	1.04E+8	-
IRG7PH42UD	Si IGBT	-	-	1.22E+3	-	2.42E+2
STGW40H120DF2	Si IGBT	-	-	1.47E+3	-	1.69E+2
GA35XCP12-247	Hybrid IGBT	-	-	3.67E+2	-	5.89E+1

would achieve the highest efficiency under different operating voltages and switching frequencies.

Under 600V operation at lower switching frequencies, the efficiency of the Superjunction MOSFETs is best, though not by much, owing to the very low on-state resistance. However, once the switching frequency is increased significantly, the two best switches are the hybrid IGBT and the Silicon Carbide MOSFET, with the hybrid IGBT being superior as a result of its lower conduction losses.

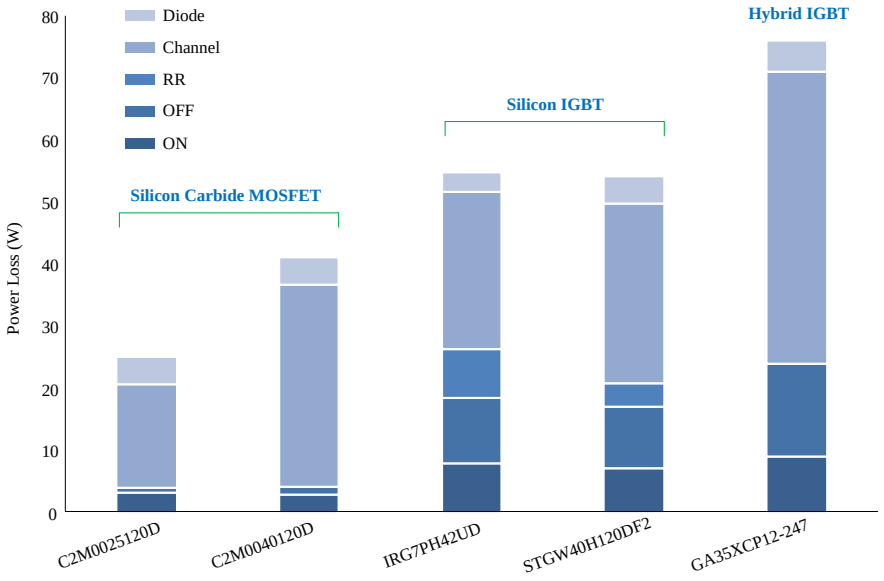


(a) f_s=10kHz.

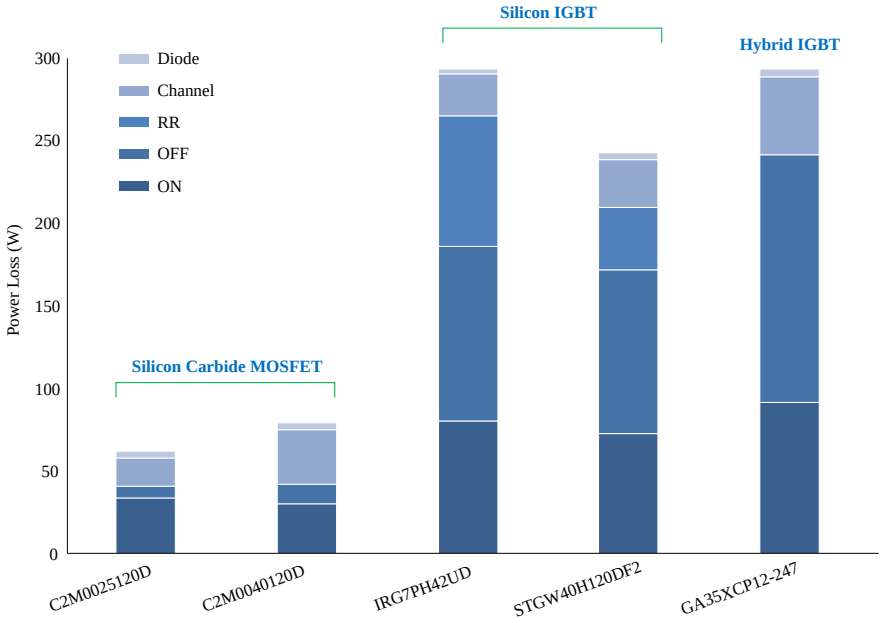


(b) f_s=100kHz.

Figure 4.1: Linear analysis applied to the switches in Table 4.2 with a DC-link voltage of 400V.



(a) f_s=10kHz.



(b) f_s=100kHz.

Figure 4.2: Linear analysis applied to the switches in Table 4.3 with a DC-link voltage of 800V.

The picture is drastically different under 800V operation with the 1200V switches: Silicon Carbide MOSFETs perform best under both switching frequencies, with the difference becoming much more pronounced at 100kHz. While this could be an artefact of the process by which switches were selected for analysis and comparison, great effort was expended searching for the best commercially available parts of all types.

Since the proposed inverter is to operate at 30kW with an 800V DC bus, the decision is made to use Silicon Carbide MOSFETs because of their all-around higher efficiency. Furthermore, high switching frequency is key to achieving a high power density via passive component size reduction, which further favours the employment of Silicon Carbide devices.

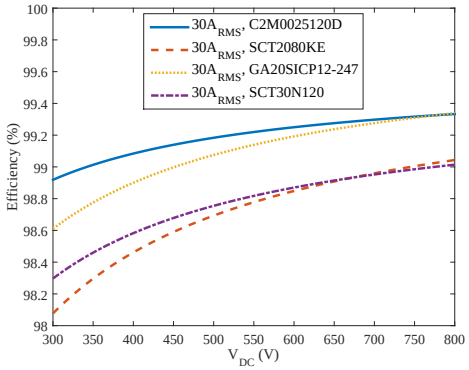
4.2.3 Silicon Carbide Switches

With the general conclusion being that Silicon Carbide MOSFETs offer superior performance with respect to their Silicon counterparts and the decision havng been made to pursue Silicon Carbide devices for the design, the next step is to evaluate several devices in a similar fashion to determine which performs the best. The list of switches and their parameters can be found in Table 4.6. The results of the analysis are shown in Figure 4.3.

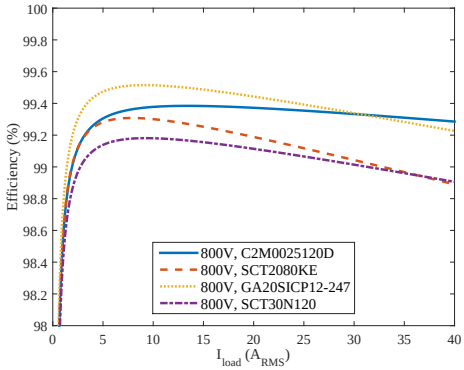
Table 4.6: Key Silicon Carbide device parameters.

Part	Datasheet $V_{DS}/I_{DS}(V/A)$	$E_{on}(mJ)$	$E_{off}(mJ)$	$R_{DS}(m\Omega)$	V_F
C2M0025120D	800/50	1.4	0.3	43	3.3
SCT2080KE	600/10	0.174	0.051	125	4.6
GA20SICP12-247	800/20	0.028	0.328	93	3
SCT30N120	800/20	0.5	0.4	90	3.5

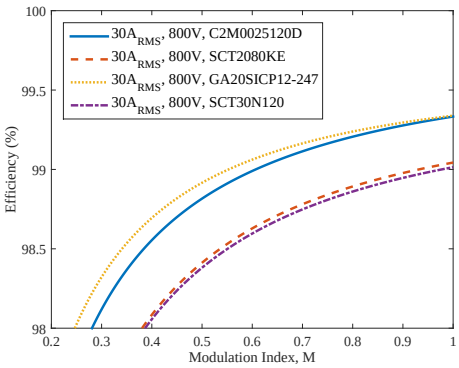
From the plotted results, a conclusion can be drawn about which switch is best



(a) DC-link voltage sweep, $M = 1$.



(b) Load RMS phase current sweep, $M = 1$.

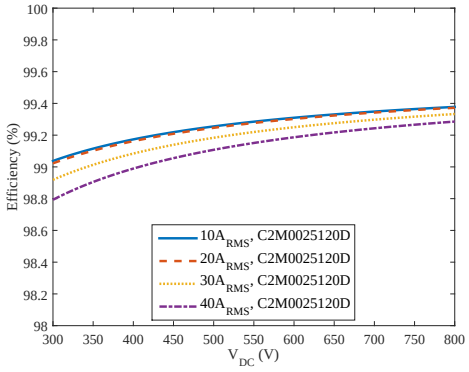


(c) Modulation index sweep.

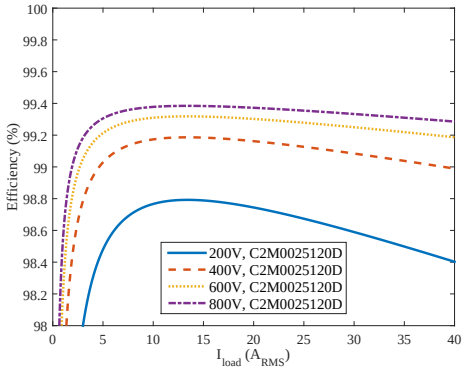
Figure 4.3: Silicon Carbide MOSFET efficiency maps with a switching frequency of 100kHz and unity power factor.

under a given set of operating conditions. For lower current and higher frequency applications, the GA20SICP12-247 transistor from GeneSiC offers higher efficiency, which can be attributed its lower switching losses. At higher currents, the Cree MOSFET, C2M0025120D, overtakes the GeneSiC device because of its lower on-state resistance in spite of its higher switching losses.

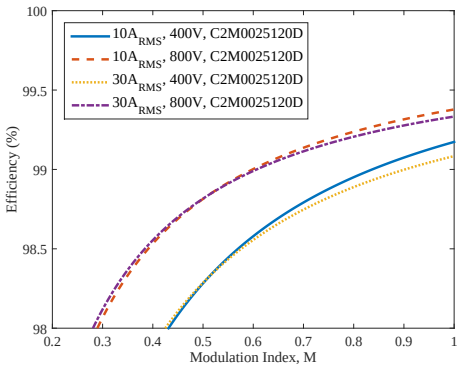
The estimated efficiencies of the two do not differ drastically under rated conditions; however, as the current increases, the Cree device begins to show greater performance. Therefore, the Cree transistor is chosen to progress with the design, as



(a) DC-link voltage sweep, $M = 1$.



(b) Load RMS phase current sweep, $M = 1$.



(c) Modulation index sweep.

Figure 4.4: Cree *C2M0025120D* efficiency maps with a switching frequency of 100kHz and unity power factor.

it affords greater flexibility should loading levels be increased in the future.

4.2.4 Chosen Switch

The same analysis used for switch selection can be applied to better understand the performance of the chosen MOSFET under several operating conditions. The results are shown in Figure 4.4. High efficiency is achieved over the expected operating range.

4.3 DC-link Capacitor

4.3.1 Optimality in Selection

DC-link capacitor bank design is, by itself, a simple task: the capacitor bank must meet a series of specifications, such as a minimum capacitance and maximum voltage and current handling capabilities. To find an optimal design, however, is a challenge. Little work has been done in this regard; indeed, many publications exist in the field of optimal capacitor placement or power level sizing for AC power distribution and reactive power compensation. Few, however, consider the optimal design of a capacitor bank, DC or AC, for power electronic applications. This is a significant gap, as research by Argonne National Laboratory on high temperature capacitors states that the DC-link capacitor bank for an automotive power inverter can occupy 35%, 23% and 23% of the volume, weight and cost, respectively, of the system (Balachandran *et al.*, 2014). When considering the number of power converters present in electrified vehicles and more-electric vehicles, even an optimistic approximation of the footprint of these capacitors on the system as a whole can be enormous.

Two previous studies have been published that consider this knowledge gap. The first analyses the switching waveforms to determine the form of the ripple current to be sunk by the capacitor, assuming the voltage source does not provide a return path. Then, a Fast Fourier Transform (FFT) is performed to determine which frequencies have the largest magnitude and are most likely to cause issues with Electromagnetic Interference (EMI). A lookup table populated with real capacitors is sequentially moved through, with each individual capacitor having objective functions evaluated to check that its capabilities to meet the requirements. If a bank is built that is capable

of sinking the RMS current and stays below a calculated threshold for minimising EMI, then it is accepted; else, continue searching. The full analysis and algorithm are described in (Anwar and Teimor, 2002).

The second study has a similar structure to the first, where the authors are most concerned with minimising EMI whilst meeting the baseline requirements of the system and ensuring long-term reliability. The biggest point of differentiation is the use of two types of capacitors, electrolytic and film, to create a filter to keep the EMI below a mandated standard (i.e. MIL-STD-461G, FCC Class B). Two databases are scoured, one for each capacitor technology, in search of possible solutions. Unique capacitor banks are built, the objective function is evaluated for every possibility and the minimum value from the set is selected. Nuances of the method can be found in (Pelletier *et al.*, 2009).

Neither of these methods are particularly optimal. The first terminates as soon as a satisfactory solution is found, which could prevent it from finding the best device and combination for the application. The second has serious reliability issues associated with it by combining different parts together and, most concerningly, in the paralleling of electrolytic and film capacitors; furthermore, the datasets need to be arranged in a very particular fashion, which removes a large degree of generality from the method. Neither approach is computationally efficient, as they both have the potential to require many iterations through large datasets to come to a conclusion. This drives the need for a more formal approach to optimisation.

4.3.2 Capacitor Bank Design

The optimal design of a capacitor bank involves the consideration of many parameters and the consequent minimisation of as many of them as possible. This does not mean that particular emphasis should not be placed on one area; indeed, in designs seeking high power density, volume is of the utmost concern. In engineering designs, there always exists a trade-off and capacitors are no different.

The following discussion will seek to maintain sufficient generality such that the developed optimisation method can be applied to any number of converter topologies and, even, applied to a variety of discrete component selection problems: switches, inductors, etc. The idea is to break the problem in to two separate components: the preprocessing of the data to tailor it to the application and the optimisation itself. By splitting in two, the problem can be decoupled from the solution method and the underlying algorithm can be used for any number of applications.

Parameters of interest for DC-link capacitor banks are: the continuous DC voltage rating, V_R; the transient voltage rating, oftentimes listed as a percentage increase of the continuous rating, V_{pk}; the maximum rated ripple current, I_C, that can be sustained without the capacitor overheating; the equivalent series resistance (ESR), R_{ESR}, resulting from the structure of the device, which goes hand in hand with the maximum rated ripple current; the equivalent series inductance, L_{ESL}; the capacitance, C; and the dimensions of the capacitor, l, w and h. The first three decide the bare minimum requirements for the bank. When preprocessing the data, each individual commercially available capacitor is evaluated according to these minimum requirements and a unique capacitor bank meeting them, and any other desired additional constraints, is designed.

The dominant capacitor failure mechanisms, irrespective of technology, are over-voltage and overheating from high ripple currents (Wang and Blaabjerg, 2014). Furthermore, along with the power semiconductors, capacitors are amongst the most vulnerable components in any converter (Ye, 2014); hence, the logical first step is to determine how many capacitors are required in series and parallel to meet the minimum requirements to sustain operation. The number of series capacitors, n_s, is a function of the voltage ratings and is calculated as,

$$n_s = \left\lceil \max\left(\frac{V_{DC}}{V_R}, \frac{V_{pk}}{V_S}\right)\right\rceil \tag{4.2}$$

where $\lceil x \rceil$ is the ceiling operator and V_S is the transient voltage rating of the capacitor, often referred to as the surge voltage. It is critical to ensure the rated and transient voltages are not exceeded, as it can lead to dielectric breakdown and failure of the component. This is a greater issue for electrolytic capacitors and, should they be designed in, additional margin is prudent.

The number of parallel components, n_p, is designed to meet the ripple specifications of the inverter. In this case, an additional constraint is placed on the voltage ripple, which adds the second term in the maximisation function. Were this not the case, the number of parallel capacitors would be determined solely by the current rating of each capacitor and the total current to be sunk. Under these conditions, it can be written that,

$$n_p = \left\lceil \max\left(\frac{I_{C,RMS}}{I_C}, \frac{n_s \cdot C_{DC}}{C}\right)\right\rceil \tag{4.3}$$

with I_C and C being the rated ripple current and rated capacitance, respectively, obtained from each individual capacitor's datasheet; $I_{C,RMS}$, the total ripple current

to be sunk by the capacitors, determined analytically or by simulation; and C_{DC}, the capacitance required to maintain a specified voltage ripple. Electrolytic capacitors are particularly vulnerable to ripple currents and excessive heating and, as a result, redundancy and as equal as possible current sharing are highly advised to minimise the probability of early failure.

These two expressions capture only the basics of what may be considered for capacitor selection. Other cases, such as those presented in (Anwar and Teimor, 2002) and (Pelletier *et al.*, 2009), may require a closer look at the total impedance of the capacitor bank for EMI filtering purposes. For high frequency switching, it would be beneficial to consider minimising the total parasitic inductance, L_{ESL}, so as to minimise voltage spikes during switching. In designs where the ambient temperature is high or efficiency is most sought after, the total power loss can be an additional constraint. As the number of parameters and constraints grow, the advantages of decoupling the data from the optimisation algorithm become clearer.

Determining the current ripple to be sunk by the capacitors is challenging and much work has been done by researchers on this subject. A reasonable approximation for preliminary bank sizing when using space vector PWM (SVPWM) is provided by (Kolar and Round, 2006),

$$I_{C,RMS} \approx \frac{I_{\phi,RMS}}{\sqrt{2}} \tag{4.4}$$

where $I_{\phi,RMS}$ is the per-phase load RMS current, assumed to be equal across all three phases. This approximation holds for power factors near unity. If the power factor is lower, then the ripple current would go down.

The voltage ripple, in percentage terms, on the DC-link can be estimated as

(Preindl and Bolognani, 2011),

$$\Delta V_{DC\%} \approx \frac{I_{\phi,RMS}}{4V_{DC}C_{DC}f_s} \tag{4.5}$$

with V_{DC} being the DC-link voltage and f_s the switching frequency of the transistors. Solving for the required capacitance for a specified ripple involves shifting terms around to get the C_{DC} on the left-hand side of the equality.

The power losses of an individual capacitor in a bank can be estimated as (4.6).

$$P_{loss} = \left(\frac{I_{C,RMS}}{n_p}\right)^2 R_{ESR} \tag{4.6}$$

A key assumption in this expression is that the ripple current is shared equally by all capacitors. While this is often not true, in a well-designed converter it is not significantly far from the truth and is a fair assumption to make. Capacitor power losses generate heat and lead to an eventual increase in its core temperature. For electrolytic capacitors, when the core gets too hot, the solution can begin to evaporate and cause an increase in pressure. Without sufficient venting, the capacitor will fail.

Auxiliary measures, such as the energy density (4.7) and power density (4.8), can be calculated and used as supplementary criteria when seeking an optimal capacitor bank.

$$ED = \frac{E_C}{Vol} = \frac{\frac{1}{2}CV_R^2}{Vol} \tag{4.7}$$

$$PD = \frac{P_C}{Vol} = \frac{V_R I_C}{Vol} \tag{4.8}$$

The volume, Vol, is the product of the dimensions and is most commonly worked

out in litres, L, which is equivalent to decimetres cubed, dm^3. The energy and power densities can be calculated, either for each individual capacitor or for the bank as a whole. Generally speaking, calculation for the bank is the preferred approach, as it is most representative of the final solution.

4.3.3 Capacitor Selection

With the theoretical capacitor banks built, it becomes a matter of choosing which one to use. Such a problem is difficult and time consuming, both in terms of computational and human resources. As previously discussed, no good method has been presented in literature to date; hence, an evaluation of several methods will be undertaken, outlining their relative benefits and drawbacks. Conclusions are drawn on the efficacy of the methods and the preferred one for design is stated and utilised to design the DC-link capacitor bank for the inverter.

Brute Force

The brute force algorithm is a simple technique to find the minimum value of a dataset. Some constraint(s) is (are) selected and the set is sifted through, with the result being returned upon completion. Its simplicity is countered by the amount of time that may be required in the case of an exceedingly large dataset; furthermore, it has some constraint-related sensitivity issues. Depending on the constraints selected, particularly in the single-objective case where only one parameter is considered, the brute force algorithm could return a component that is minimal in one regard but performs poorly in others. Take, for example, Figure 4.5: the smallest power losses

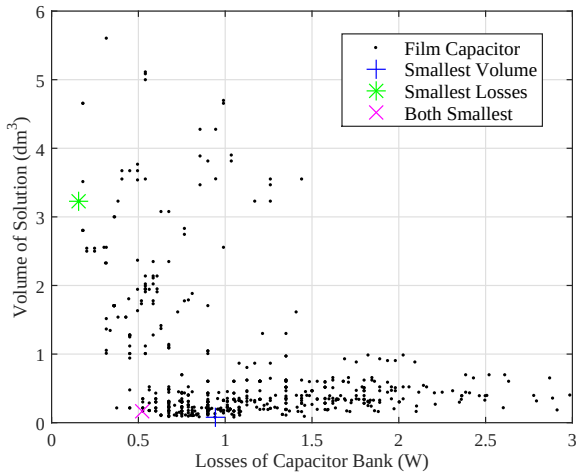


Figure 4.5: Single-objective and multi-objective minimum value searches using the brute force algorithm.

would correspond to a DC-link capacitor bank with a size just over $3dm^3$. In a space-constrained system, this would not be a good choice. If the focus were shifted to minimizing the volume, however, a very good solution would be found that results in a power loss that is acceptable. A multi-objective search, combining the previous two cases, as an example, returns a reasonable solution. Herein lies the problem: the result obtained will be only as good as the capacitor bank parameter constraints applied and their values.

While this algorithm offers some flexibility–namely, in terms of what constraints to apply and their values–its most significant detraction is that it lacks greater flexibility. Once a set of constraints have been applied, a solution is found. If the found capacitor bank is actually unsatisfactory, then further runs through the data must be executed with that specific case deemed inadmissible. This makes it an unfavourable method to use when seeking optimality.

Constrain and Filter

The constrain and filter approach applies a series of constraints to whichever capacitor bank parameters are under consideration. It can be thought of as being similar to, albeit more flexible than, the brute force algorithm. A set of constraints are placed on the dataset, eliminating banks that do not satisfy them. Where the two approaches diverge is in their handling of any dataset: brute force finds an explicit solution, whereas constrain and filter leaves a reduced-order dataset for a decision maker to analyse and choose from.

In a more mathematical sense, the constrain and filter technique can be reformulated as an optimisation in the epigraph form, where a transition is made from (4.9) to (4.10).

$$\begin{aligned} &\underset{f(x)\in\mathbb{R}^{n\times m}}{\text{minimize}} && f(x) \\ &\text{subject to} && f_i(x) \leq c_i, \quad i = 1,\ldots,n \\ &\text{subject to} && x \in \mathbb{R}^m, \quad x = 1,\ldots,m \end{aligned} \tag{4.9}$$

$$\begin{aligned} &\underset{t\in\mathbb{R}^{n}}{\text{minimize}} && \mathbf{t} \\ &\text{subject to} && f_i(x) \leq c_i, \quad i = 1,\ldots,n \\ &\text{subject to} && c_i = t_i, \quad i = 1,\ldots,n \\ &\text{subject to} && x \in \mathbb{R}^m, \quad x = 1,\ldots,m \end{aligned} \tag{4.10}$$

In both cases, $f(x)$ is a matrix with dimensions of the number of capacitor banks under evaluation, m, and the number of capacitor bank parameters to be constrained, n. The constraints, c_i, are applied such that each $f_i(x)$ is less than a prescribed value.

In (4.9), a single set of constraints is laid out to be met. An algorithm checks the value of each and, if all are met, it is kept within the set; if not, it is discarded.

Then, the best component within the reduced set is sought. In this work, the decision making process was manual.

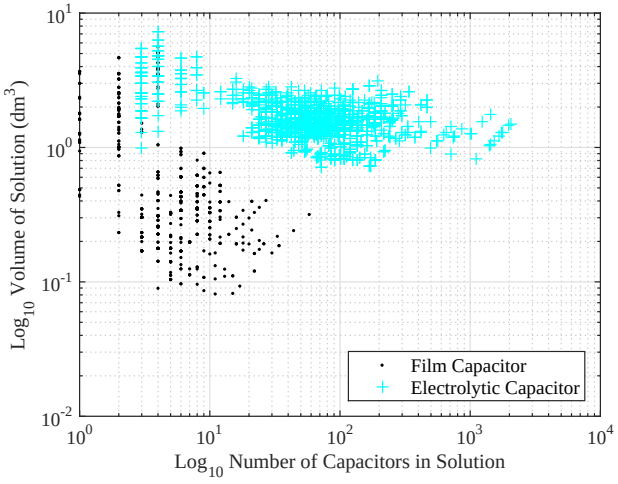
The reformulation to an epigraph-type problem in (4.10) makes it explicit that it is an iterative process. The vector, t, is composed of some arbitrary set of constraints, initially chosen to provide a solution that the designer could find satisfactory. The initial t constraints are applied to the set, similar to the formulation in (4.9). If a satisfactory solution is found by the designer within this iteration, the algorithm can be terminated; if not, the values of each t will be reduced downwards, tightening the constraints of the capacitor banks, imposing further reduction in the size of the set. This continues until the designer has chosen a proposed solution.

The result of a constrain and filter operation is presented in Figure 4.6. The selected capacitor for the design is already denoted as this approach is the one preferred for the design, as will be expanded upon in section 4.3.5.

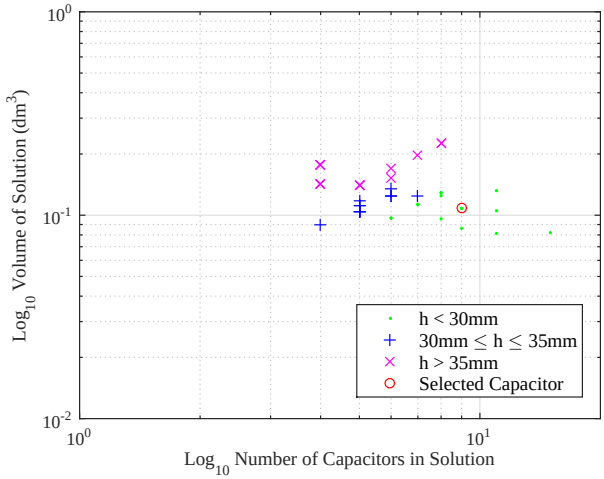
Cost Function

A cost function-based approach allows for a weighting to be applied to each parameter to more reasonably achieve a compromise. An additional benefit is that design parameters can be coupled together, allowing for a more complete evaluation of each capacitor bank in the dataset. The cost function, J, can take on infinitely many forms and is inherently arbitrary: it is the designer's discretion as to what is most important in the design. A simple weighted approach is described by (4.11),

$$J_i = \sum \left(w_1 v_{1,i} + w_2 v_{2,i} + \cdots + w_k v_i \right) \tag{4.11}$$



(a) Total data set being operated on.



(b) Result of constrain and filter operation.

Figure 4.6: Constrain and filter operation, reducing the dataset from 2000 to 40 items.

where w_k is the weight of the k-th design variable under consideration; and $v_{k,i}$ is the k-th design variable at the i-th position in the dataset. The weightings can be either a weighted average or they can take on any non-zero value. Whichever approach is used can have an impact on the results. The value of each weighting coefficient, w_k, can be selected by understanding whether the goal is minimise or maximise the

cost function, J, and whether the design variable, v_k, should be driven upwards or downwards. Alternative approaches can employ higher-order powers, as opposed to coefficients, when devising the cost function.

The cost function approach can be used on its own or in tandem with other approaches (i.e. brute force). A key benefit, which can be seen more clearly when discussing its application to simulated annealing, is that the data can be meaningfully manipulated such that an underlying structure can be built in to the dataset, which has already been seen to be lacking such a property.

An illustrative cost function is created of the form in (4.11). It is comprised of five variables with corresponding weights emphasising the importance of size: volume, $w_1 = 1$; power loss, $w_2 = 0.5$; height, $w_3 = 2$; surface area, $w_4 = 1$; and number of capacitors, $w_5 = 0.25$. A heavy penalty is placed on taller components and a smaller cost is incurred for solutions with many capacitors, as their paralleling can introduce additional benefits, such as a reduced AC loop inductance. The function applied to the data for a particular case is shown in Figure 4.7.

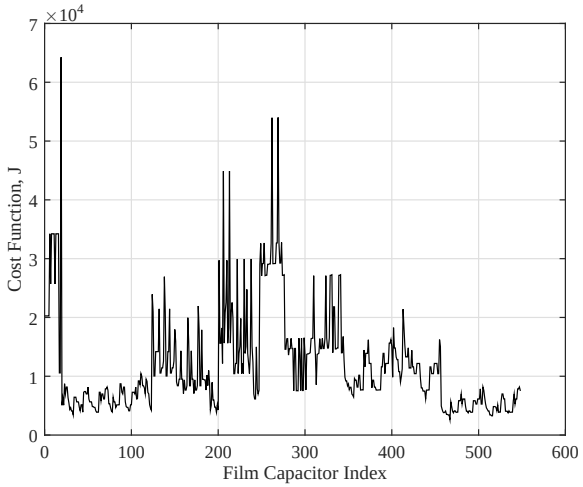


Figure 4.7: Cost function output given the film capacitor data.

Surface Fitting

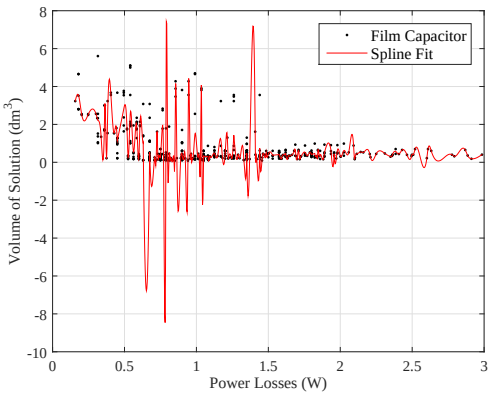
Surface fitting provides an avenue by which an analytical expression can be obtained, opening up the opportunity to apply gradient-based techniques; alternatively, the derived expression could be used in tandem with heuristic techniques to converge on a solution. Many approaches are possible with a closed-form expression of the data.

A surface is most easily visualized in two or three dimensions; if a higher order is desired, then it would make sense to couple several variables together with a cost function–as in the previous section–and then plot it in the desired dimension. The curves and surfaces herein will be generated in the easily visualized space. Plots for three cases are shown in Figure 4.8. The curves and surfaces are generated using the curve fitting toolbox in MATLAB. A better fit can be obtained by increasing the complexity of the fitting technique, with two examples provided by (Gálvez and Iglesias, 2012; Xie *et al.*, 2012), where a 3D surface is reconstructed from a set of scattered data points using non-uniform rational B-splines.

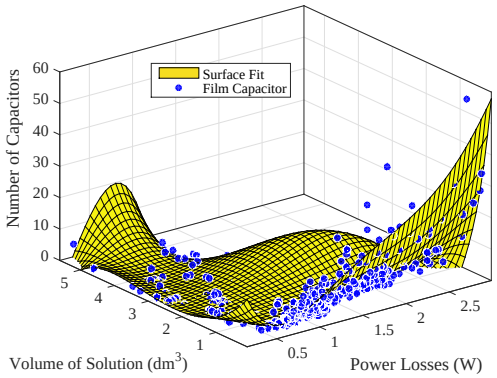
The quality of fit and the return of a function depends on what curve fitting algorithm is used in the toolbox. For example, with the spline, it is comprised of a series of functions, of an order selected by the designer, which connects as many points together as possible. An example of a spline fit is presented in Figure 4.8 (a). The toolbox does not cleanly return a continuous function for optimization and, hence, it is undesirable to use a spline to fit in this fashion. Indeed, a cost function approach would be better suited in this case. Furthermore, exploring other fitting techniques showed that, in a two-dimensional case, curve fitting is not a particularly good option with the utilized dataset.

In terms of a three-dimensional fit, a fifth-order polynomial (the highest order

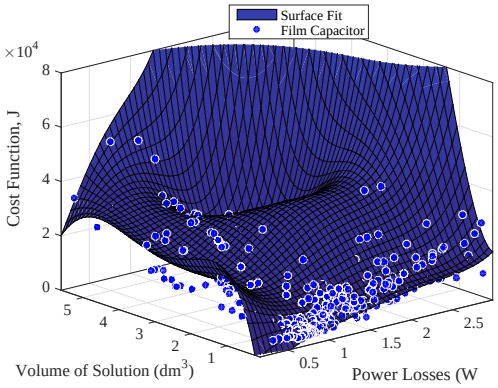
available in the toolbox) was used. The function has 21 coefficients and two cases are shown in Figure 4.8 (b) and (c). With a function like this, it is possible to find minima analytically and with gradient-based methods; however, since it may be non-convex, care needs to be taken to ensure that local minima are not found and declared to be the globally optimal solution. It is also entirely possible that the fit function returns inadmissible values (i.e. volume <0). Instances such as those would need to be recognized and the function traced back to an admissible point.



(a) 2D spline fit.



(b) 3D fifth-order polynomial.



(c) 3D fifth-order polynomial, cost function.

Figure 4.8: MATLAB curve fitting toolbox surface fits and the underlying data.

None of the returned functions fit the data particularly well, which is a result of both the restricted polynomial order and the chaotic nature of the input. In each case, the fitted function is non-convex, requiring either some form of appropriate restriction(s) to analyse over a convex range or to apply a heuristic technique to try to find the global minimum. No real benefits are obtained with this technique.

Pareto Optimality

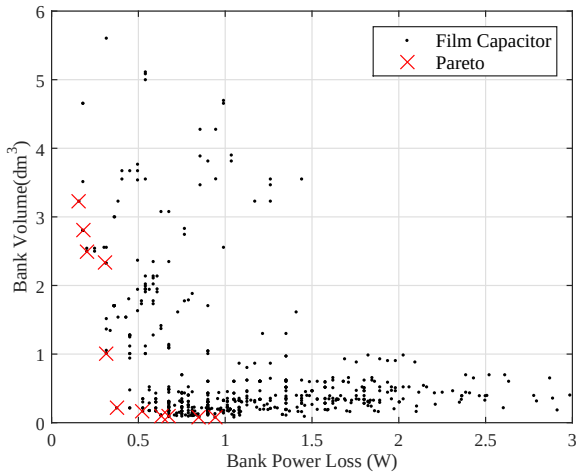
Pareto optimality generates a tradeoff surface, whereby the variable on the x-axis can only be enhanced by accepting a reduction on the y-axis, and vice-versa. Each member of this surface is considered optimal. An example of Pareto optimal points is illustrated in Figure 4.9, where the the goal is to minimize both values. A reduction in the power losses drives an increase in the volume in the Pareto optimal capacitor banks.

The Pareto front returns the best capacitors for a series of given design parameters and is conducive to providing the designer with a handful of devices to manually evaluate. Its use is more of a visual tool and a helping hand than a direct optimiser; nevertheless, its ability to distil a large dataset to a smaller one comprised of the optimal components for a given tradeoff provides substantial aid in the decision making process.

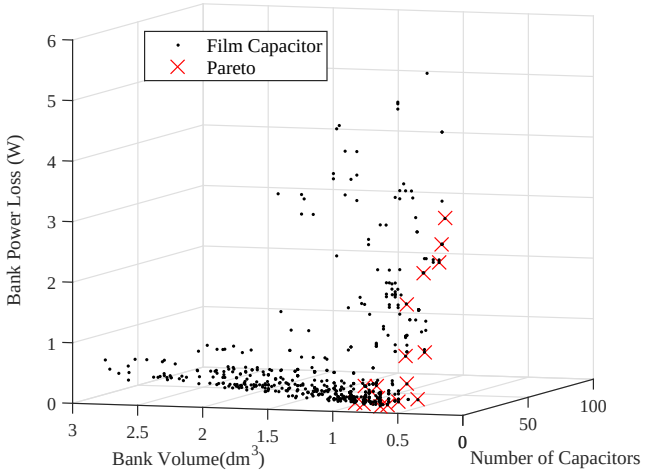
Simulated Annealing

Simulated annealing is discussed in detail in section 3.4.2. Its application to the example dataset can be seen in Figure 4.10.

The algorithm does a good job of finding small values for the individual parameters



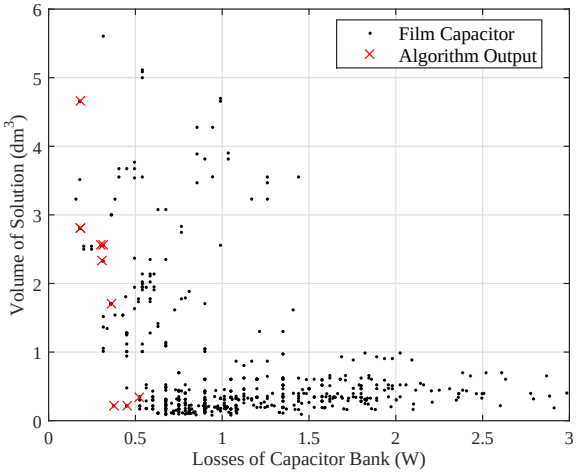
(a) 2D Pareto front.



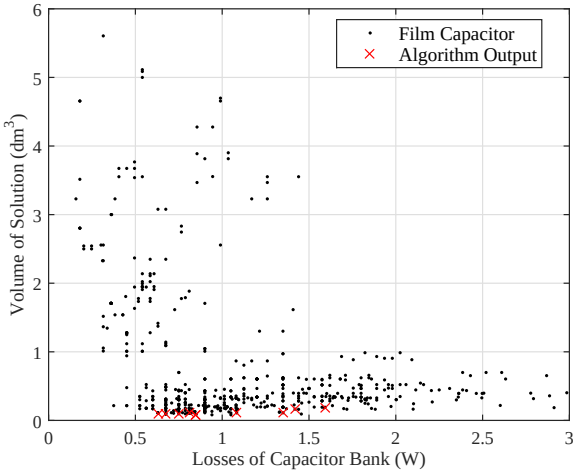
(b) 3D Pareto front.

Figure 4.9: 2D and 3D Pareto fronts for film capacitors.

it is asked to minimise. However, when not constraining several variables simultaneously, the algorithm can return components that would be considered unsatisfactory. For example, in Figure 4.10 (a), the capacitors with the absolute lowest losses are very large and would cause the converter's volume to increase by a significant amount relative to other possible configurations. In Figure 4.10 (b) the drift is less severe as the



(a) Simulated annealing to minimise losses.

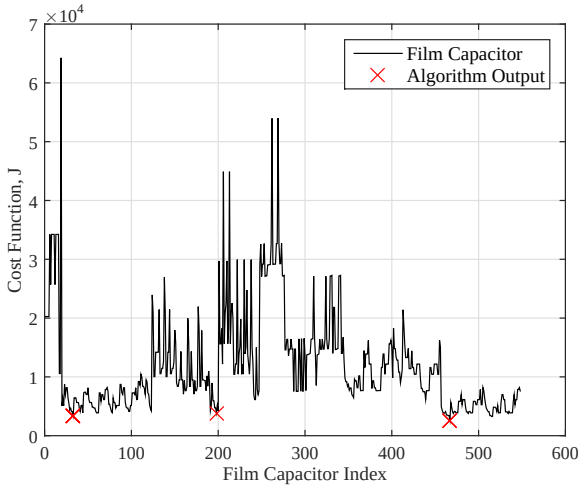


(b) Simulated annealing to minimise volume.

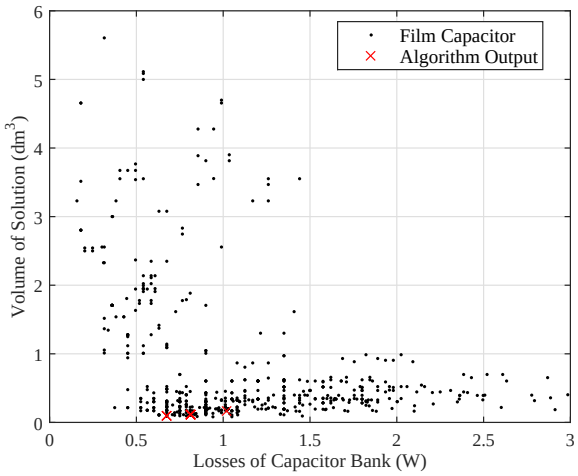
Figure 4.10: Ten runs of simulated annealing algorithm on dataset.

power losses increase by approximately 2W from one extremity to another; however, in a system seeking the highest possible efficiency, this may not be acceptable.

The coupling of parameters can be done in a fashion similar to the brute force algorithm; however, this can become cumbersome and frustrating to implement. A



(a) Simulated annealing on cost function.



(b) Algorithm results plotted with input data.

Figure 4.11: Results of ten runs of the simulated annealing algorithm on the cost function.

reasonable approach would be to employ a cost function and run the simulated annealing algorithm on it, coupling many variables together in the hope of achieving a more consistent result. By using the function defined in (4.11) to generate Figure 4.7, the simulated annealing algorithm can be used to obtain the results in Figure 4.11.

The results are quite good when compared to those presented in Figure 4.10. The final resting point of the algorithm finds small values of the cost function with regularity, including the global minimum. The resultant optimal capacitors are clustered together with low volume and little drift in the power losses; furthermore, the same capacitors are found more frequently than before, presenting less work for the designer should a decision need to be made based on component availability.

4.3.4 Additional Considerations

Selection via some algorithm can be the most efficient means to decide upon a component; indeed, automating the process frees engineering time for another task and is capable of finding the truly optimal solution for a given problem. However, the algorithm is only as smart as the data it is provided with and how it is implemented. There may even be cases where the smallest component volumetrically leads to a larger total system volume because of a lack of fit relative to package constraints, which is something that that cannot be easily encoded within an algorithm and is highly application specific. Any approach could very well settle on a capacitor that is not commercially available, depending on how the database is populated, meaning that the search itself was not fruitful and additional constraints must be added to avoid such a state; or, better prioritising the constraints, which is challenging to build in. At this point, direct designer input is required, rendering an automated approach to selection of reduced utility.

4.3.5 Conclusions

With these shortcomings noted, the constrain and filter approach is considered the most reliable, albeit more time consuming, due to the need for a decision maker to be directly involved. The primary benefit is that engineering intuition can guide the selection process to a capacitor that balances several requirements for finding a satisfactory solution. With tight enough constraints, the resulting set can be made sufficiently small so as to facilitate selection.

Of similar quality are Pareto optimality, for determining the best capacitors along a tradeoff curve, and simulated annealing, for stochastically finding a satisfactory minimum. Several runs of the simulated annealing algorithm on a representative cost function can return multiple results which, in turn, can be used in a fashion similar to the constrain and filter approach to determine which is best for the given application.

Figures 4.12 and 4.13 show the location of the selected capacitor in the dataset comprised of both electrolytic and film capacitors, and of only film capacitors in a format similar to the results of other techniques, respectively, after decision making using the constrain and filter technique. It can be seen that, when plotting the items with volume and power losses on the axes, the result is quite near the global minimum. Simulated annealing with the prescribed function returned a component, amongst several others, with the same volume, albeit slightly higher losses (1W as opposed to 0.8W), than the constrain and filter result, exhibiting its potential for effective usage.

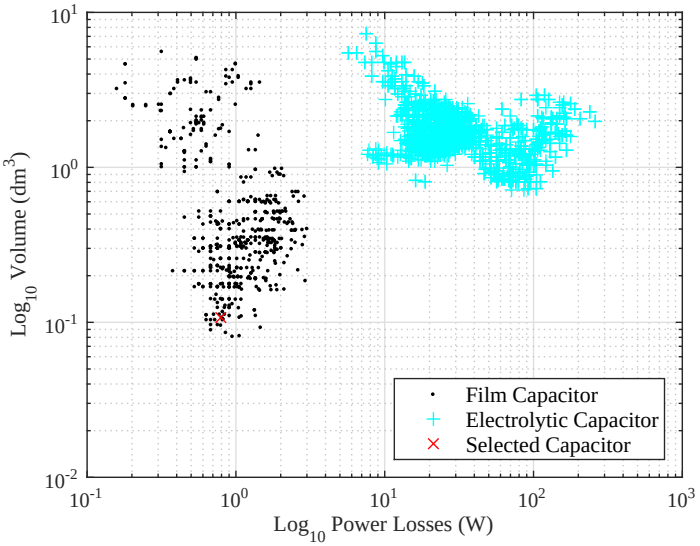


Figure 4.12: Entire data set with selected capacitor denoted.

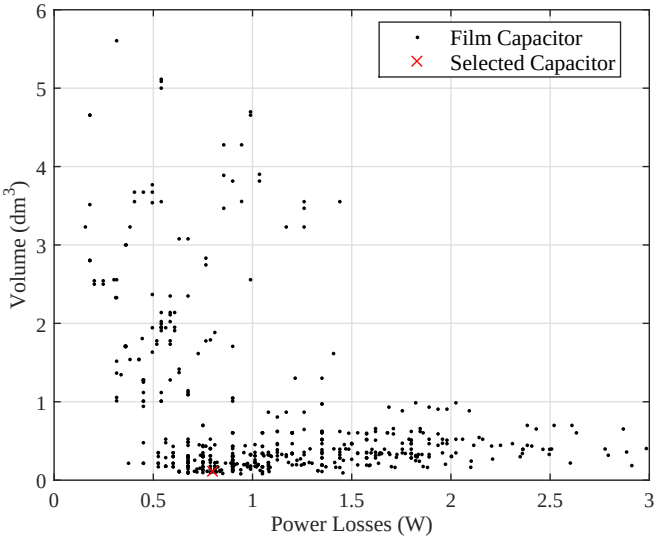


Figure 4.13: Film capacitor only dataset with chosen capacitor denoted.

4.4 PCB

A PCB can be thought of as a bus bar, albeit on a much smaller scale, as it is no more than layers of copper separated by an insulating material; therefore, the analysis undertaken in section 3.5 can be employed to assist in its design. The proper design of the PCB contributes significantly to reducing the parasitic inductance, helping to ensure transient voltage spikes remain below the maximum blocking voltage of the semiconductor devices. Detailed finite element simulations can be performed to obtain a very accurate measurement of the inductance, thereby allowing for the design to be pushed closer to its operating limits; however, this can take a significant amount of time to not only run, but to model as well. Any minor change would result in a change in the impedance, resulting in a need to resimulate and reinterpret the results. An approach employing best practices is often sufficient for obtaining satisfactory performance. The need for finite element simulations becomes increasingly apparent when a multi-layer PCB structure is defined, with several current routing and discontinuous planar arrangements existing.

Best practices dictate keeping forward and return current paths on opposing layers with as small of a spacing as possible. In this way, flux cancellation can be maximised and the stray inductance reduced. Furthermore, by ensuring capacitors are placed close to components requiring transient power, current loops can be minimised and the system's performance enhanced. Effective filtering can be used to shunt noise back to its source and reduce radiated emissions, as well as improving the quality of the power transmitted by the converter. These practices are put to work in (Khan *et al.*, 2014), albeit for bus bars, where best practices are followed to obtain a design with low impedance.

The maximum electric field strength is the key determinant of the thickness of the insulating and adhesive materials in a PCB stackup. The most common insulator is FR-4 and the layers of copper are held together by an epoxy resin mixture, normally referred to as "prepeg." The dielectric field strength of both are provided by the PCB manufacturer. In this design, both were in excess of 40kV/mm (Gold Phoenix, 2012). Knowing this and the maximum voltage to be encountered during operation, the minimum separation distance between layers can then be calculated as,

$$d_{min} = \frac{V}{E_{max}} \tag{4.12}$$

where E_{max} is the maximum electric field strength specified in the material's datasheet. The separation distance should be small so as to minimise the parasitic inductance of the conducting material but large enough to sustain the peak transient voltage expected. The prepeg layers require extra care as the conductor can reduce its effective thickness. A typical four-layer PCB stackup is shown in Figure 4.14 that shows this nuance.

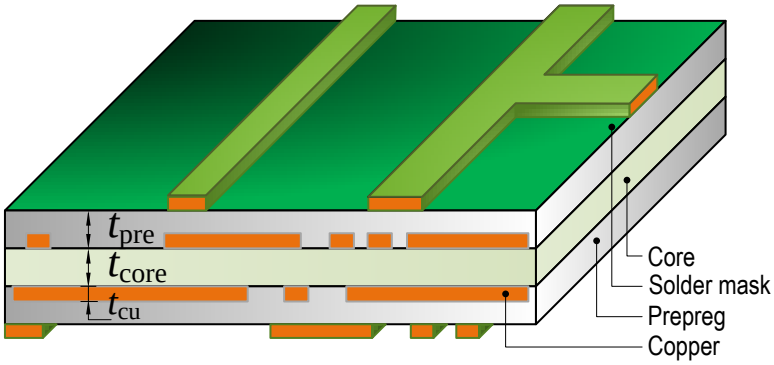


Figure 4.14: Prototypical four-layer PCB stackup.

The thickness of the prepreg, t_{pre} is affected by the thickness of the copper, t_{cu}.

Copper thickness for a PCB is normally specified in ounces, with one ounce (oz) of copper having a thickness of approximately 35μm. Attention must be paid to this aspect of the design as the erosion of prepreg thickness could cause the minimum separation distance, d_{min}, to not be met, resulting in the eventual failure of the board.

The decision on a copper thickness is the result of several considerations, including the current to be conducted, the width of the planes carrying the current and the temperature rise of the board that can be sustained. IPC-2221, the "Generic Standard on Printed Board Design," suggests good design principles for component spacing and isolation based off of the voltages to be seen and provides formulae for the calculation of the width of traces for a given copper thickness, current and permissible temperature rise. Internal and external layers will have different results due to the difficulty that internal layers have in evacuating generated heat.

Two versions of the inverter were designed and built. Their copper and insulation thicknesses are listed in Table 4.7.

Table 4.7: Inverter PCB thicknesses utilised.

	Version 1.0	Version 1.1
Copper Thickness (oz)	2	3
Layer 1-2 Thickness (mm)	0.5	0.45
Layer 2-3 Thickness (mm)	2	1.4
Layer 3-4 Thickness (mm)	0.5	0.45

4.5 Summary

In this chapter, the design of a three-phase inverter with a target of a high power density was discussed in detail. At each stage in the process, optimality in components must be sought: the best performance in the best package with the best overall fit. The transistors have the least flexibility in this regard, as they tend to dictate the converter's shape and performance most significantly. A capacitor or a gate driver is significantly more interchangeable than the power transistor in most cases, particularly for Silicon Carbide where the selection of devices is currently limited.

With respect to capacitor selection, novel techniques and methods were introduced to attempt to solve the problem of optimal component selection. The result from an intuition-based approach and an automated approach with the simulated annealing algorithm returned capacitors from the same series, albeit with marginally higher losses, showing the promise simulated annealing and other heuristic and stochastic algorithms have for discrete component selection.

The end result of applying these techniques and best practices is an inverter with a length, width and height of 238mm, 128mm and 33mm, respectively. This gives a volume of 1.084L and, at an output power of 30kW operating at 100kHz, this provides a power density of 29.84kW/L, well above other results reported in literature (Sato *et al.*, 2011; Sasaki *et al.*, 2013) with equal–or greater–on-board functionality and exceeding handily United States of America Department of Energy targets for 2020 and beyond (Rogers, 2012).

Components of this chapter were summarised in a paper presented at the 2016 IEEE Transportation Electrification Conference and Expo (ITEC) (Eull *et al.*, 2016).

Chapter 5

Inverter Prototype & Experimental Results

5.1 Parasitic Parameters

The parasitic parameters of a converter contribute greatly to its performance. A high inductance leads to large voltage transients during switching, higher losses due to the slowing of the current rise and fall times and increased electromagnetic emissions. The resistance acts as a power loss mechanism, causing temperature rises and can lead to the eventual failure of the PCB due to the expansion and contraction of the board under thermal stresses. The capacitance helps in reducing the characteristic impedance of the system, acting as a sort of basic filter to reduce emissions.

It becomes important, then, to estimate the parasitics in some fashion. As a result of the complex interconnection scheme, the analysis undertaken in section 3.5 can only act as a basic guidance to provide a rough estimate. Finite element simulations will give the best results; however, they can take significant amounts of time and require

special care when accounting for manufacturing tolerances and the solder used to electrically connect everything.

For these reasons, a precision impedance analyser was employed to measure several major aspects of the inverter. This data can be used to build a full impedance model of the AC commutation loops, as well as exploring the behaviour of each individual component. With respect to the PCB itself, it can be determined whether or not the stray inductance is too high for a given operating point, helping to improve the long-term reliability of the assembly. The impedance analyser was configured to apply an oscillating voltage signal with an RMS value of 500mV.

5.1.1 Measurement Preparation

To ensure accurate measurements, the equipment needs to be calibrated after turn-on to account for environmental noise. For each setup, some form of cabling was required; hence, the impedance of that connecting mechanism had to be measured as well. Once measured, the number of required cables were prepared with the same length from the same wire spool so as to keep the impedance of each wire approximately equal.

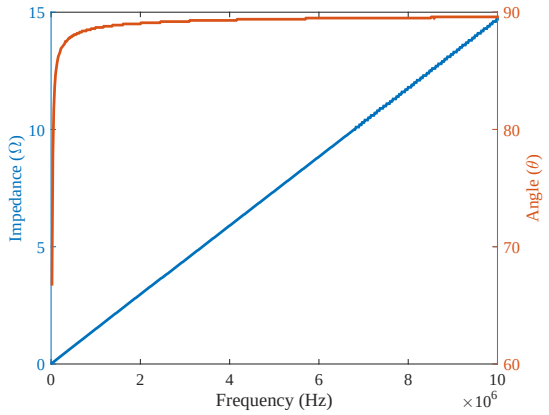
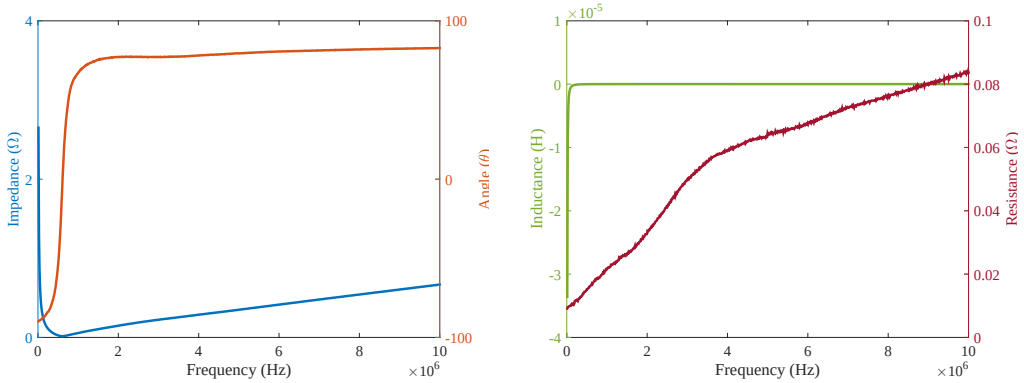


Figure 5.1: An example magnitude and phase characteristic for a wire.

While a measurement of the wire for each case has been prepared, the effects of the wires have not been subtracted from the data. It is provided as is from the impedance analyser.

5.1.2 DC-link Capacitor

Information pertaining to the DC-link capacitor is found in the datasheet; however, having the opportunity to measure it for a real device is beneficial as it takes in to account tolerances, reflecting what would most likely be seen during actual operation. The capacitor was directly placed on the terminals of the impedance analyser, introducing no new parasitics to the testing circuit.



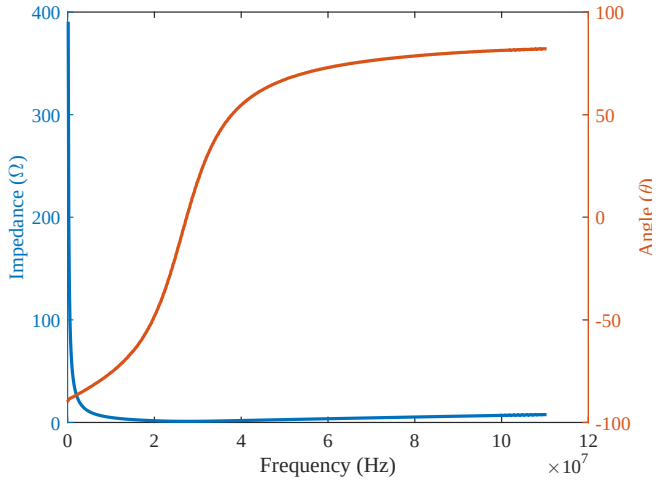
(a) Magnitude and phase. (b) Series inductance and resistance.

Figure 5.2: Impedance curves of the DC-link capacitor *B32774D8505K*.

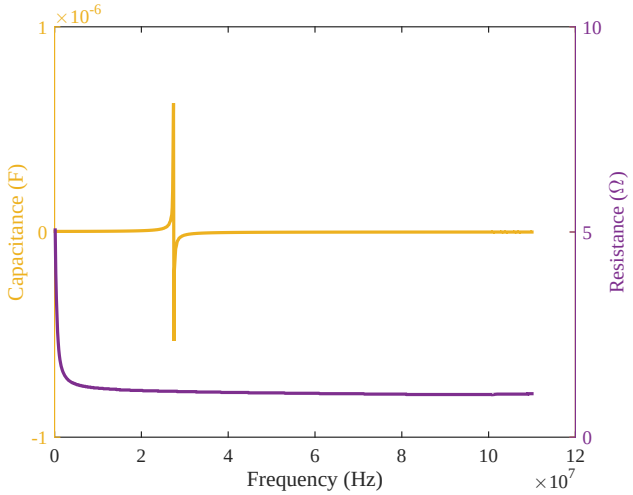
5.1.3 MOSFET

The MOSFET has several parasitics associated with it, as detailed in section 3.1.2. Understanding them, particularly the inductances, is integral to achieving the highest fidelity switching and loss model possible. While measurements can be taken when

it is connected to the PCB, as is done in section 5.1.7, its exact characteristics are drowned out by the rest of the board. Having data for the device itself increases its applicability to future research.



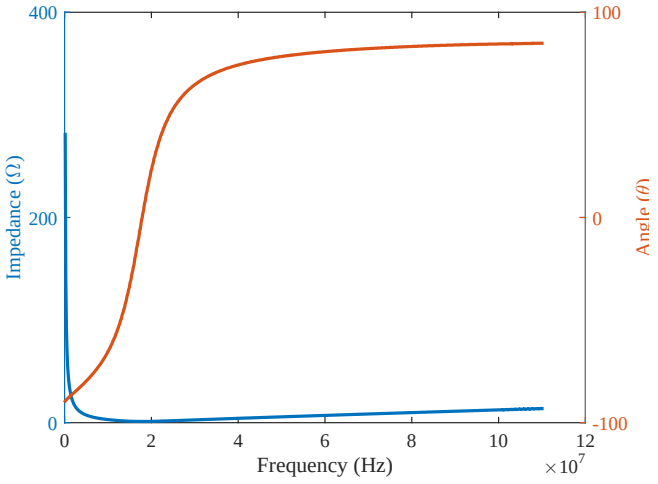
(a) Magnitude and phase.



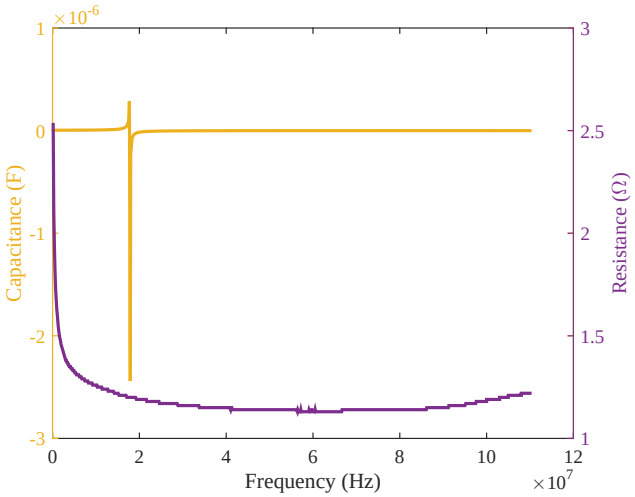
(b) Series capacitance and resistance.

Figure 5.3: Impedance curves of the gate-drain connection of the Silicon Carbide MOSFET *C2M0025120D*.

The results from the impedance analyser show good behaviour that correlate well



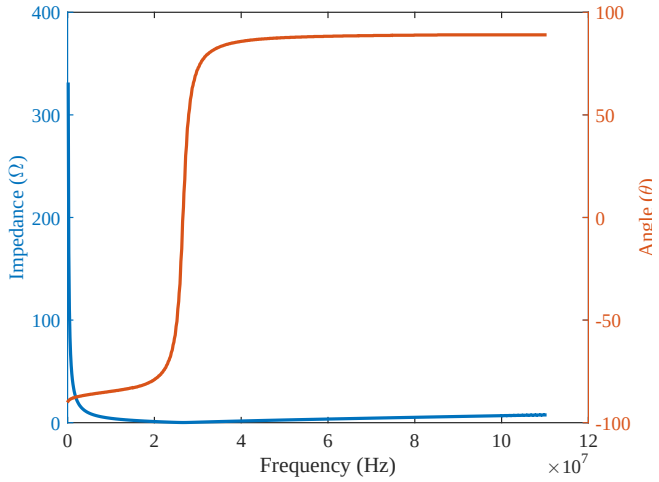
(a) Magnitude and phase.



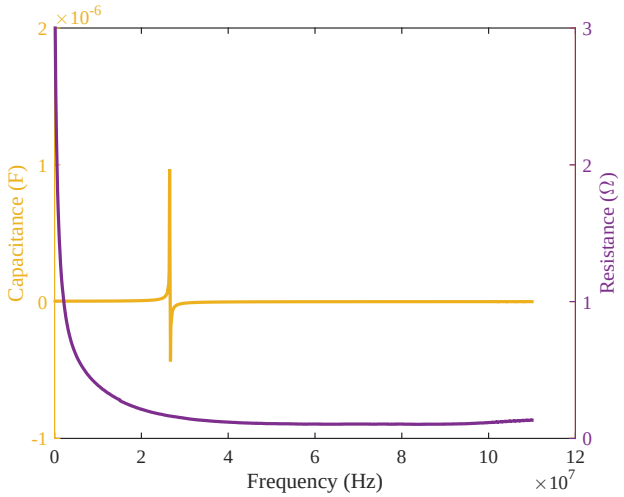
(b) Series capacitance and resistance.

Figure 5.4: Impedance curves of the gate-source connection of the Silicon Carbide MOSFET *C2M0025120D*.

with the model of a MOSFET with its parasitics included, per Figure 3.4. Resonances when the MOSFET is turned off can be observed, resulting from the interaction of the capacitances and the inductances from the leads and the bonding methods. When the gate is biased so as to turn the device on, no discernible resonance phenomenon



(a) Magnitude and phase.



(b) Series capacitance and resistance.

Figure 5.5: Impedance curves of the drain-source connection of the Silicon Carbide MOSFET *C2M0025120D* when off.

is observed (Figure 5.6).

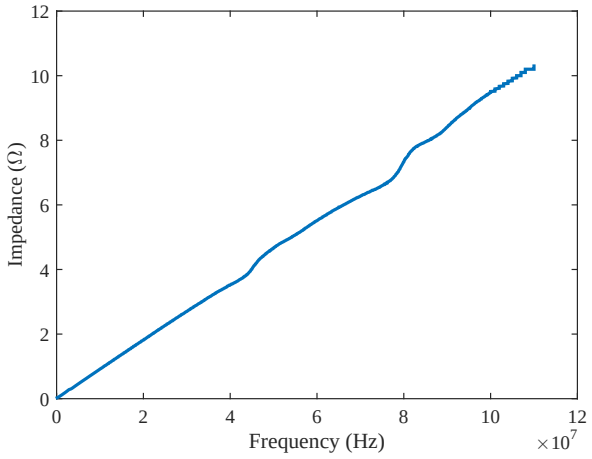


Figure 5.6: Impedance curve of the gate-source connection of the Silicon Carbide MOSFET *C2M0025120D* when on.

5.1.4 PCB Capacitance

The capacitance of the PCB is measured by leaving all terminals open and measuring across the DC bus, from positive to negative. This was done using the high-side drain and low-side source terminals of each individual phase leg, as shown in Figure 5.7.

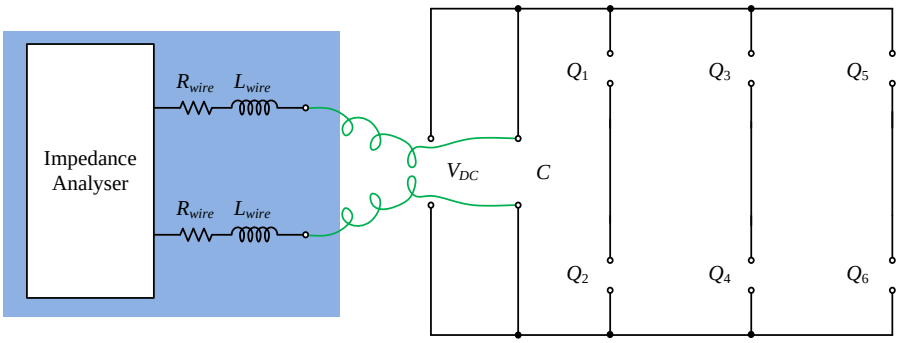


Figure 5.7: PCB capacitance measurement schematic.

A resonance appears to occur around 15MHz, as the impedance briefly drops to zero before increasing upwards, as seen in Figure 5.8. This most likely arises from the

parasitic capacitance of the PCB structure and the conductance of the FR-4 dielectric material separating the layers.

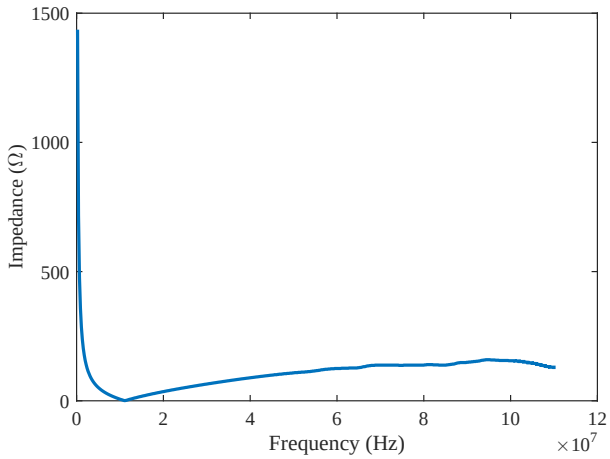


Figure 5.8: Impedance curve of the PCB alone when measuring from the positive terminal of capacitor 1 to the negative terminal of capacitor 9.

5.1.5 Commutation Loop Impedance

The impedance of the commutation loop is what most substantially contributes to the slowing of switching transients and voltage overshoots on the DC bus. Its estimation is integral to assessing whether a given switching scheme will result in the failure of the transistors from voltage transients. It can also be used for devising enhanced switching models. Its importance demands it be obtained in some form. Estimation via analytical expressions is challenging, as was outlined in section 3.5, making measurement an attractive option for obtaining data.

Two configurations were used to measure the AC current path impedances. The first was to use a small wire to short circuit the DC-link capacitor terminals and then sequentially solder a wire to the high-side drain and low-side source connections for

each individual phase. The path impedance from transistor to capacitor was measured for the individual phase legs. The second was to connect the positive and negative terminals of the impedance analyser to the positive terminal of the first capacitor and the negative terminal of the ninth capacitor. Then, each phase leg was sequentially short circuited, allowing for the progressive total impedance measurement.

Testing schematics, some results and discussion for these two approaches follow.

From the Transistor Terminals

The measurement of the impedance from the high-side switch's drain to the low-side switch's source is the first method by which the impedance of the commutation loop was obtained. The testing schematic for this subset of cases is shown in Figure 5.9.

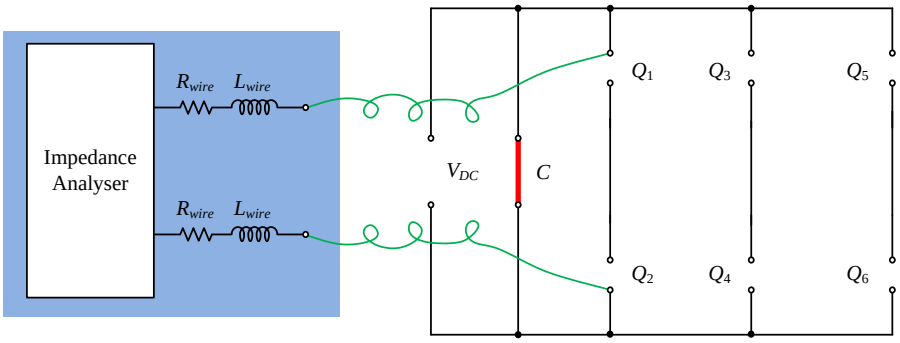


Figure 5.9: PCB impedance measurement schematic short circuiting the capacitors.

The physical test platform for a specific case in this configuration is given by Figure 5.10.

A single example, when measuring the impedance from the terminals of the phase C transistors to the capacitors is presented in Figure 5.11.

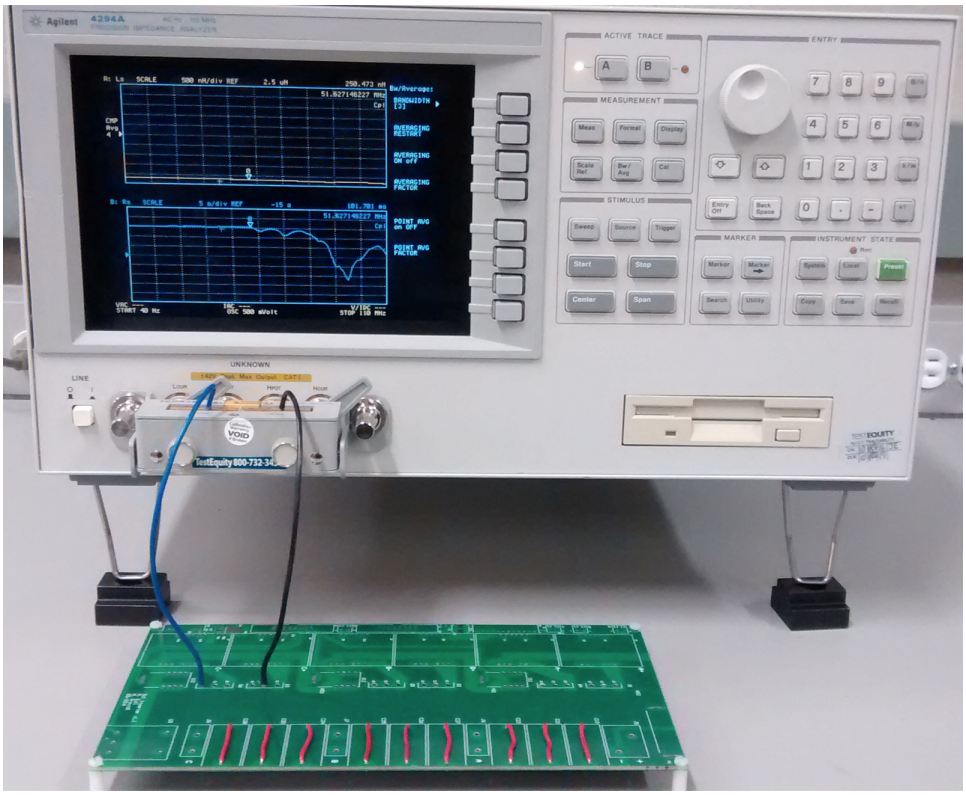


Figure 5.10: Physical measurement setup for the commutation loop with the capacitors shorted.

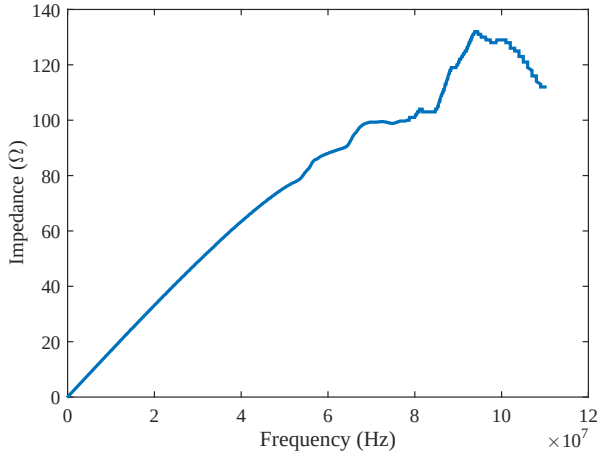


Figure 5.11: Impedance curve of the commutation loop from the transistor terminals.

From the Capacitor Terminals

The testing schematic for this case is shown in Figure 5.12.

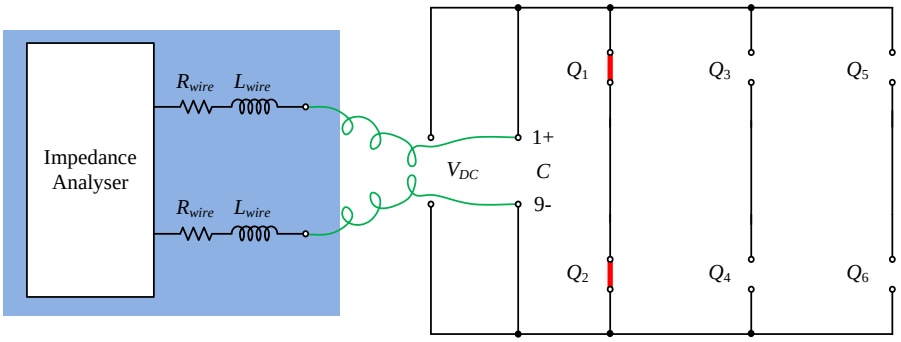


Figure 5.12: PCB impedance measurement schematic short circuiting the phase legs.

The physical configuration of this measurement scheme, where the positive contact of the analyser is connected to the positive terminal of capacitor 1 and the negative to the negative terminal of capacitor 9 and a phase leg is short circuited, is given in Figure 5.13.

In this approach, the total impedance of the AC path is measured. If each individual path is desired, some basic mathematics need to be performed to obtain the impedance for each leg. The first leg to be tested was phase A, followed by A and B, and then all three together. The total impedance of the two latter cases are described by (5.1) and (5.2).

$$Z_T = \frac{Z_A Z_B}{Z_A + Z_B} \tag{5.1}$$

$$Z_T = \frac{Z_A Z_B Z_C}{Z_A Z_B + Z_A Z_C + Z_B Z_C} \tag{5.2}$$

To obtain the individual phase leg impedances, the desired terms must be solved

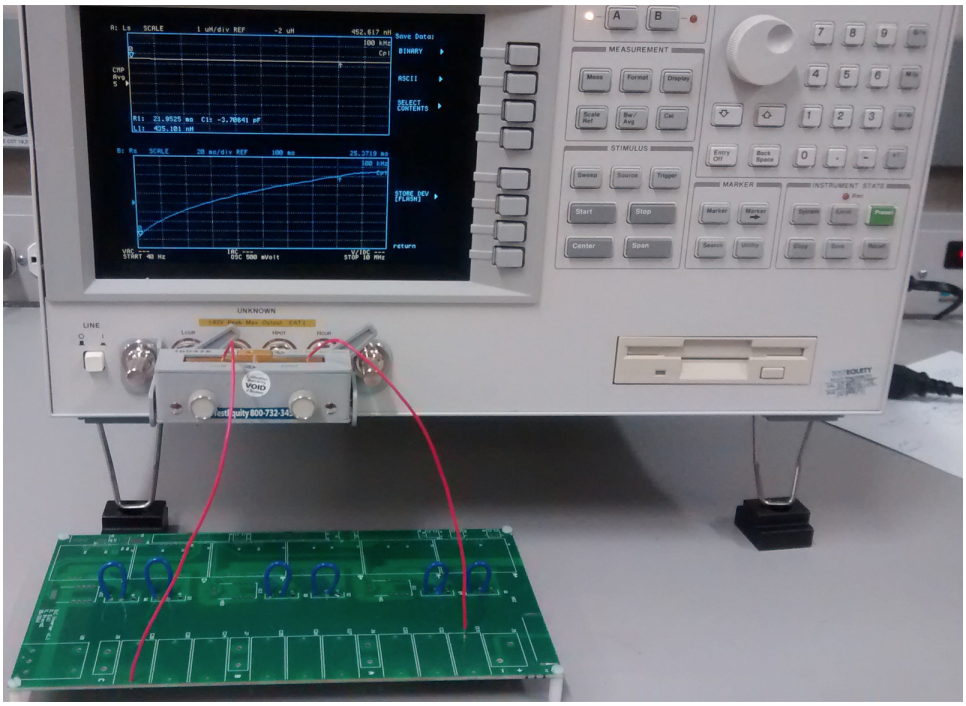


Figure 5.13: A test of the commutation loop with the transistor phases shorted.

for. The expressions are given by (5.3) and (5.4).

$$Z_B = -\frac{Z_T Z_A}{Z_T - Z_A} \tag{5.3}$$

$$Z_C = -\frac{Z_T Z_A Z_B}{Z_T Z_A + Z_T Z_B - Z_A Z_B} \tag{5.4}$$

The measured impedances are shown in Figures 5.14 through 5.16. With the effects of the wires removed, this data can be used to obtain the impedances of the individual phase legs and assist in voltage overshoot analysis.

The most significant difference between two measurement approaches is the clear resonance when measuring across the capacitor terminals as opposed to no discernible resonance when shorting the capacitors and measuring across the transistor terminals.

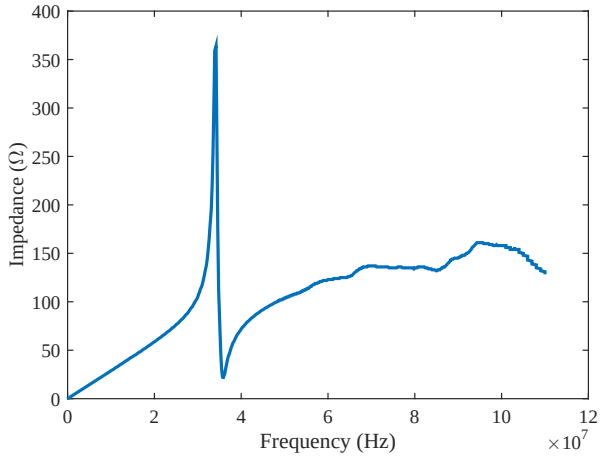


Figure 5.14: Impedance curve of the commutation loop from the capacitor terminals, phase A short circuited.

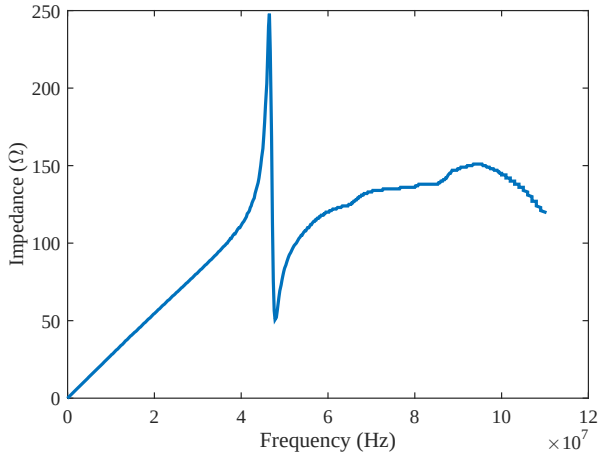


Figure 5.15: Impedance curve of the commutation loop from the capacitor terminals, phases A and B short circuited.

This result is logical, as in the former the signal must pass through the dielectric material of the PCB, whereas in the latter it strictly uses copper connections.

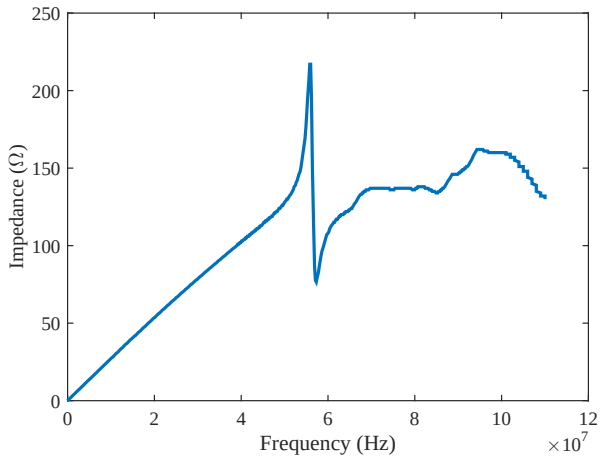


Figure 5.16: Impedance curve of the commutation loop from the capacitor terminals, phases A, B and C short circuited.

5.1.6 Output Stage Impedance

The output stage impedance is measured from the source of the high-side switch to the drain of the low-side switch, as shown in Figure 5.17. While covered implicitly when short circuiting the phase legs, having a set of curves describing it is useful.

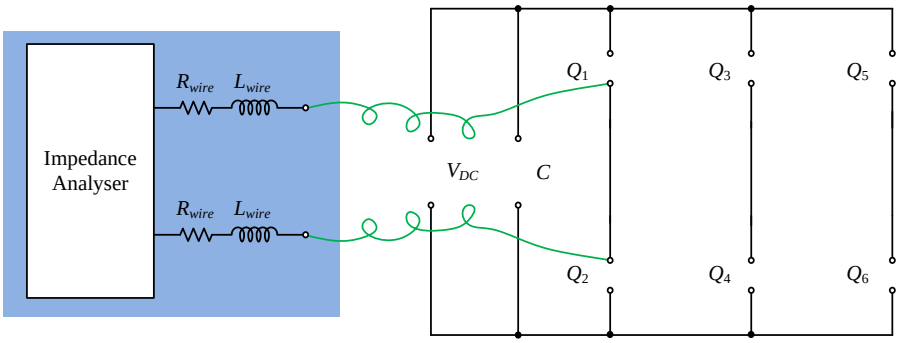


Figure 5.17: PCB impedance measurement schematic measuring the output stage.

Like in Figure 5.12, the signal passes through only copper connections and is predominantly inductive. This is shown in Figure 5.18.

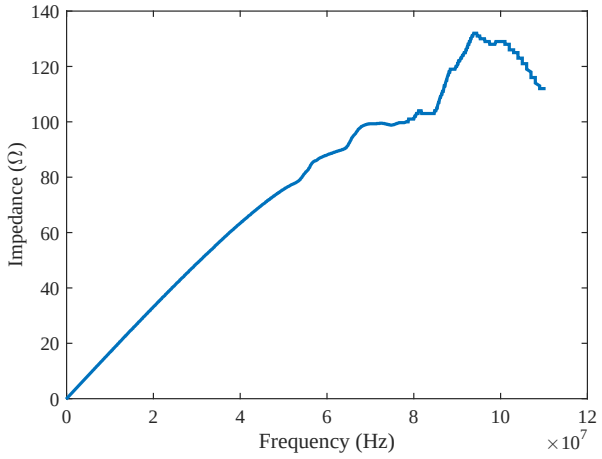


Figure 5.18: Impedance curve of the output stage of phase A.

5.1.7 Assembled PCB

The measurement of the impedance of an assembled PCB is the synthesis of all the individual components already discussed and investigated. It accounts for the interaction between the parasitic elements of each component and allows for an investigation of the actual system's impedance. The testing schematic is shown in Figure 5.19, which is similar to that shown in Figure 5.12, with the difference being that the tests are run on a populated PCB as opposed to an empty one.

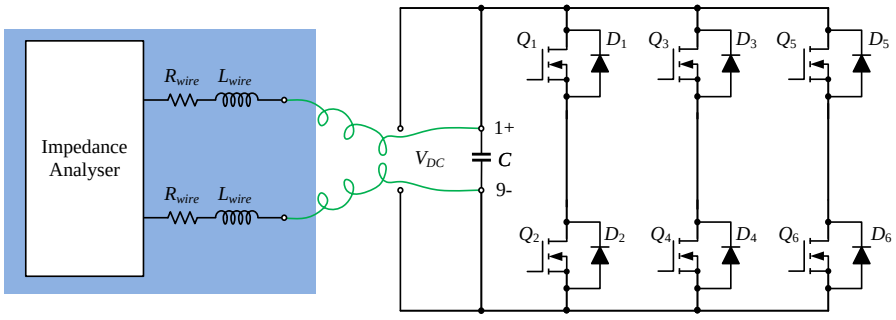


Figure 5.19: PCB impedance measurement schematic for an assembled inverter.

Measurements for when all transistors are off and when each leg is progressively turned on with a positive gate voltage bias are shown in Figures 5.20 through 5.23.

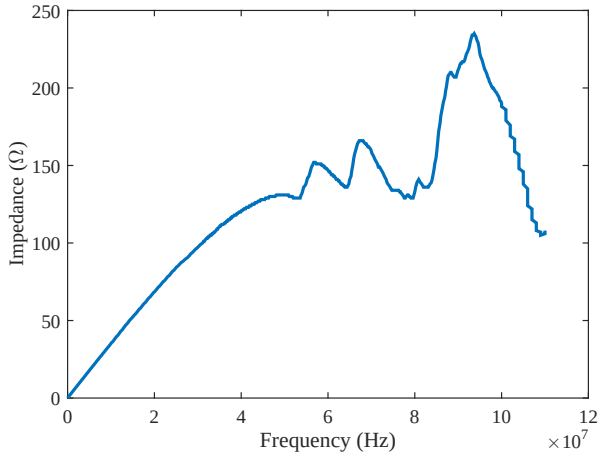


Figure 5.20: Impedance curve of the assembled PCB, all transistors off.

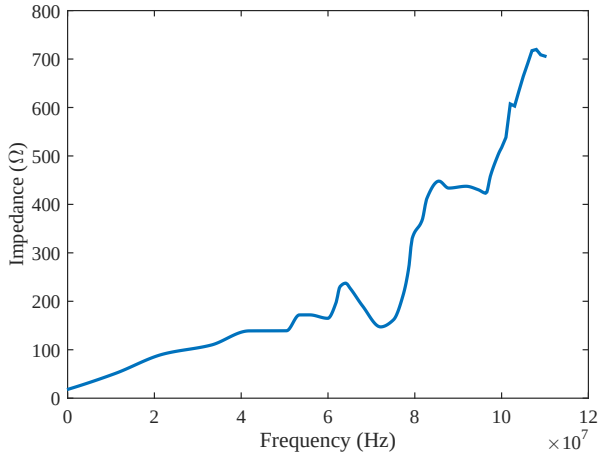


Figure 5.21: Impedance curve of the assembled PCB, phase leg A on.

Exceptional behaviours are observed with what look like many different resonant points on the assembled PCB. The underlying cause is likely the different impedance characteristics of each individual component, with nine paralleled capacitors and three

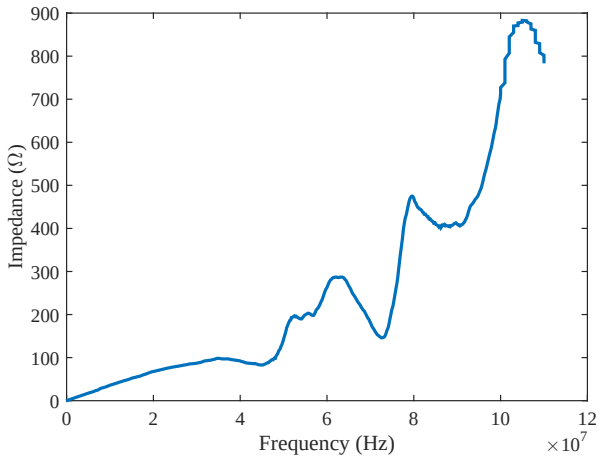


Figure 5.22: Impedance curve of the assembled PCB, phase legs A and B on.

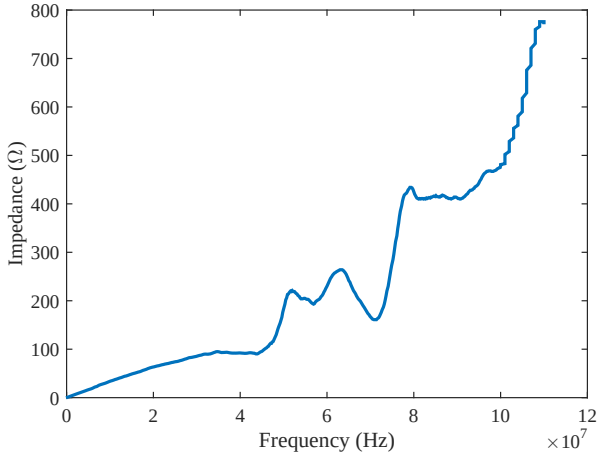


Figure 5.23: Impedance curve of the assembled PCB, phase legs A, B and C on.

sets of paralleled transistors with two devices total per phase leg. As more MOSFETs are turned on, the initial resonance point progressively reduces, which reflects the decreasing impedance from paralleled commutation loops.

5.1.8 Conclusions

The results of the parasitic parameter experiments show that the resonance point of the board, populated and unpopulated, is between 40 and 60MHz, depending on how many phases are switched in. It is at this point where it changes from being a capacitive to inductive transmission system. At 100kHz, the intended operating point, the inductance of the commutation loops are reasonable and are expected to drop to a lower value when the wire impedances are removed.

5.2 Low Power PMSM Configuration

To test the functionality and efficiency of the inverter, it is connected to a permanent magnet machine acting as a motor and an induction machine acting as a load. Both are rated at about 5kW. A picture of the setup as a whole is shown in Figure 5.24.

The efficiency of the inverter is obtained by using a power analyser. Due to the time-varying, switched nature of the voltage waveforms, the calculation of an RMS value of the output voltage is difficult; furthermore, the assessment of the power factor of the electric machine becomes more challenging. The use of a power analyser eliminates these problems and provides a highly accurate measurement. However, the accuracy depends directly upon the tolerances of the probes. The most accurate method is to feed the three-phase and DC current waveforms in to the back panel of the machine. Unfortunately, these are rated to only fives Amperes RMS, meaning the power levels must be kept low. The use of probes that measure magnetic flux have an error tolerance that is too high for precision calculations.

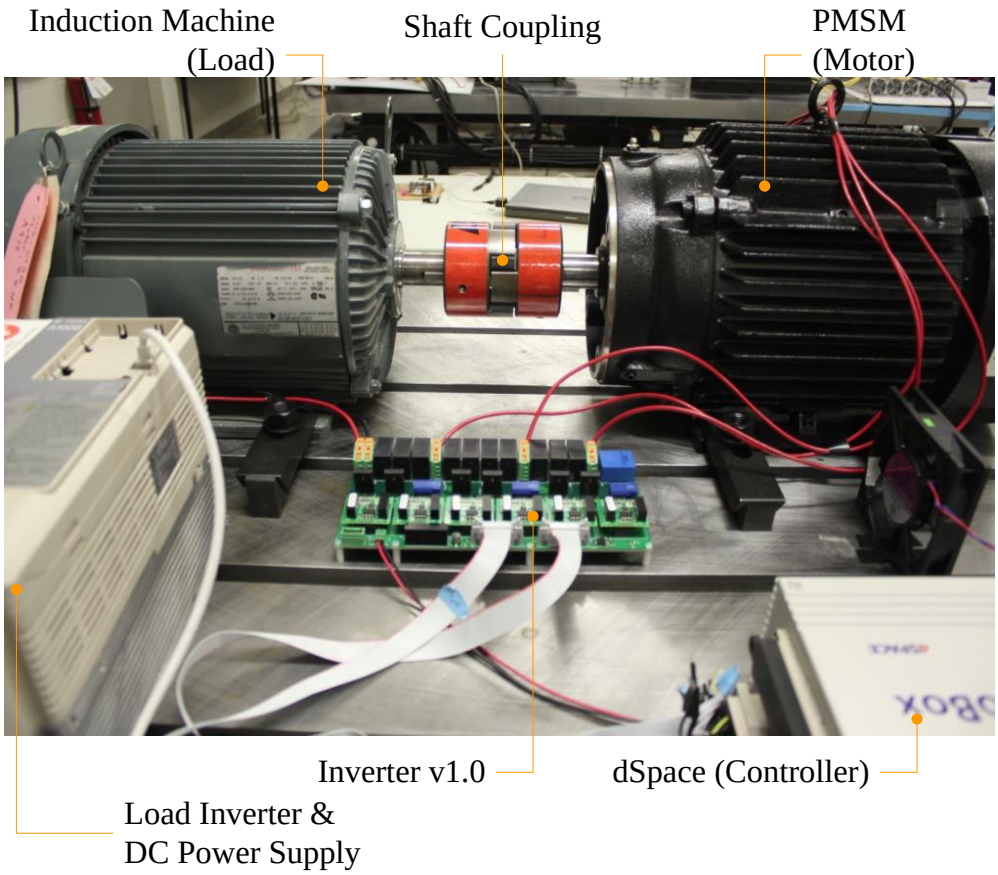


Figure 5.24: Full testing setup of inverter version 1.0.

Connecting as discussed, the efficiency of the inverter can be measured. Comparisons between the measured and estimated efficiencies are presented in Figure 5.25. The results show good correlation, with the sole caveat being that the output power is around 1kW in both cases. Nevertheless, it shows that, at low power levels, the loss modelling techniques employed for the MOSFETs give good results. The tests were performed at a switching frequency of 10kHz.

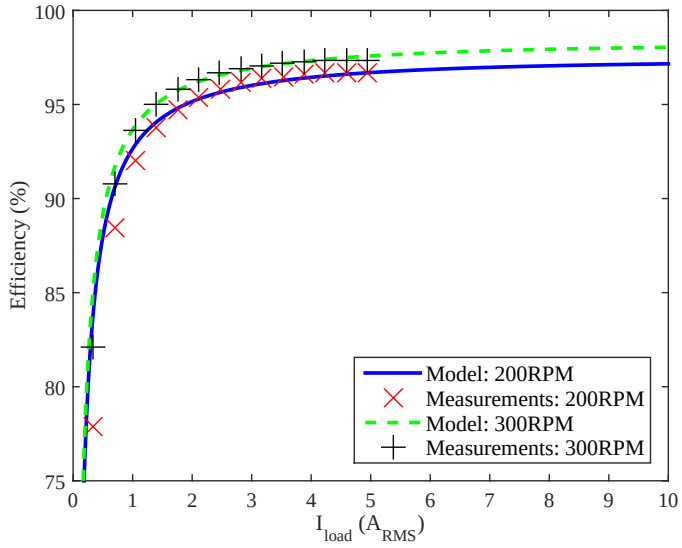


Figure 5.25: Comparison between model and measurements at a DC-link voltage of 300V and a switching frequency of 10kHz.

5.3 High Power Induction Machine Configuration

For this testing, the second version of the inverter with an on-board forced air heatsinking solution and other, more minor revisions was used. Figure 5.26 shows one fully assembled inverter without being connected to any setup.

Equipment limitations require two major changes in testing: the first is that a testbench change is required to push higher power levels; and the second is that efficiency measurements no longer become accurate as a result of probe tolerances. Nevertheless, the general performance of the inverter can be assessed and it can be shown to work under higher power levels. Case and heatsink temperature measurements can be made to show a certain rise above ambient, which gives an indication of the loss levels and an estimate of the amount of power that can be transmitted.

The testing configuration, shown in Figure 5.27, has the designed inverter driving

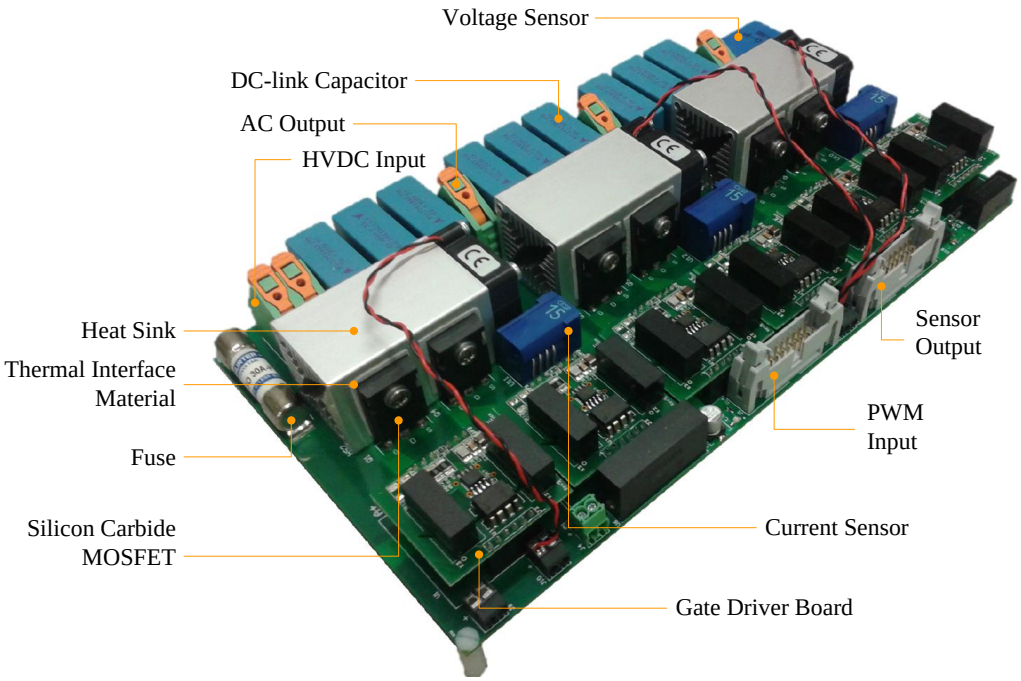


Figure 5.26: Inverter version 1.1.

a three-phase induction machine with a permanent magnet machine as the load. Torque and speed transducers allow the mechanical power to be calculated as (5.5),

$$P_{mech} = \tau \omega_r \tag{5.5}$$

where τ is the output torque and ω_r is the angular velocity in rad/s. An exact efficiency map of the load machine is not known and, hence, the electrical power delivered to the motoring machine cannot be readily determined. However, a generous estimate can be made on the mechanical system's efficiency of it being no more than 87% efficient, which is the machine's rated efficiency at rated power. A higher efficiency assumption would translate to the electrical power delivered being underestimated,

which is prudent when making such assumptions; hence, taking the nameplate efficiency of 87% is fair. This power is used primarily to categorise the power levels the inverter is delivering.

To acquire an idea of the relative efficiency of the inverter, a thermal camera can be used to observe the temperature rise over ambient of the heatsink and the cases of the MOSFETs. If, at a low mechanical power level, the case of a MOSFET is dangerously hot, then it would not bode well for pushing the inverter to higher voltages and currents; conversely, if the temperature rise is low, then it would indicate that the

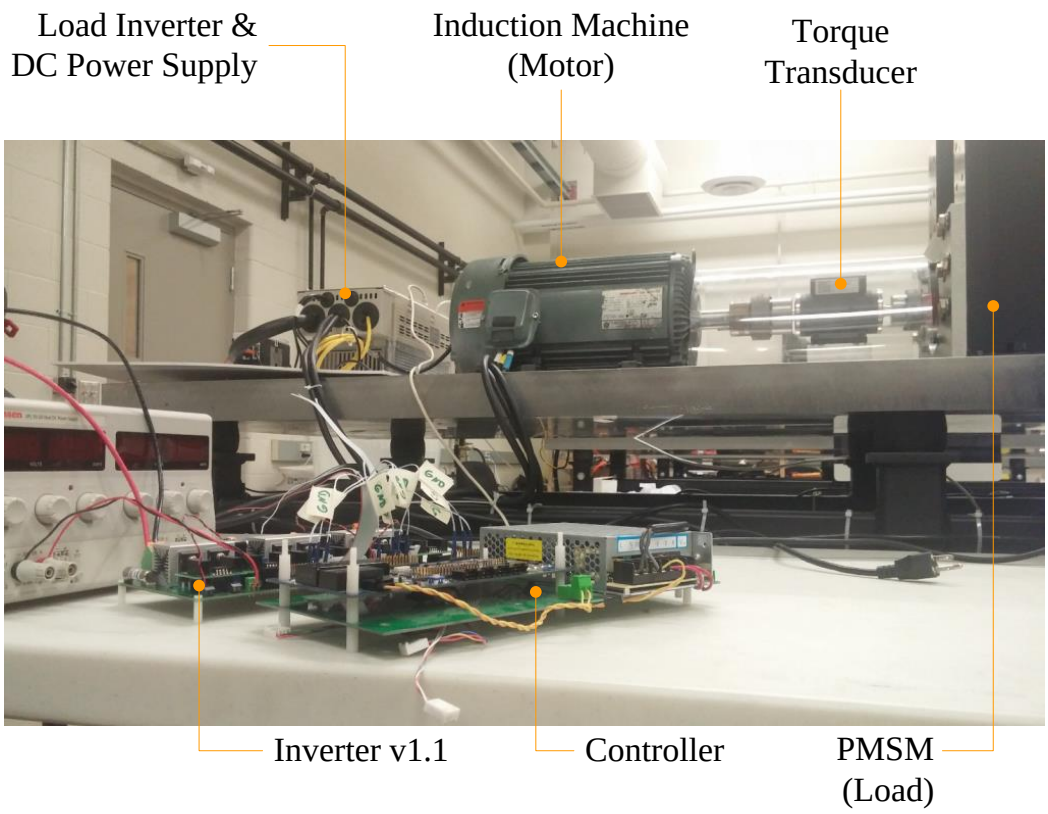


Figure 5.27: Testing setup of inverter version 1.1.

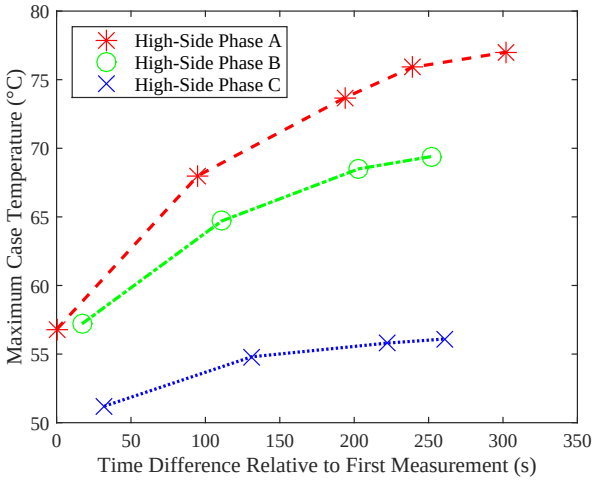
inverter can be pushed harder. A current probe can be used to obtain a waveform for the phase current, allowing for some understanding of its influence on the heating of the MOSFETs.

Several tests at different power levels were performed; however, the highest power case is of the greatest interest. The mechanical power delivered, as read from the sensors, is approximately 10.76kW. Assuming an optimistic efficiency of the motor of 87%, this would translate in to a delivered electrical power of around 12.37kW. Space Vector PWM was the switching scheme employed. In all tests, the switching frequency was 10kHz.

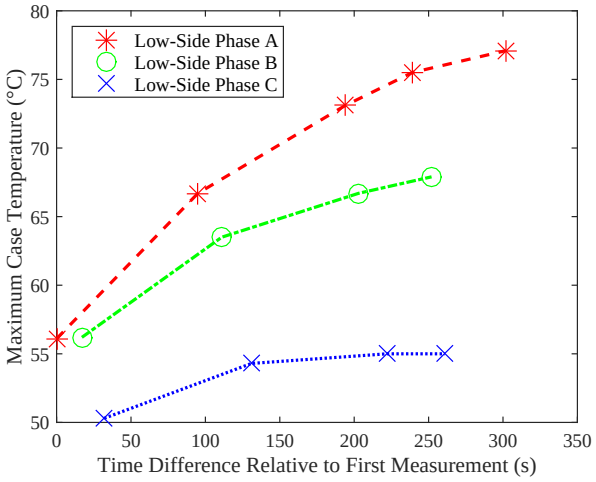
Figures 5.29 through 5.32 present a series of thermal camera images of the MOSFETs, per phase, as well as a view downwards, looking at the top of the heatsinks. The relative temperature rise can be observed over time. As would be expected, the MOSFETs on phase A operate much hotter than phase B and C due to the hot air from each phase being blown downstream. The result is more extreme than anticipated, with a temperature difference of over 20°C observed between phases A and C. The fuse, in the lower left-hand corner of Figure 5.32 is operating with a peak temperature over 100°C, indicating that the heatsink configuration is not optimal.

By analysing these images, a trend of the maximum hotspot over time can be observed. It is elucidated in Figure 5.28.

What can be observed from the thermal camera is that, in phase C, the temperature rise is not as significant as the other phases; furthermore, after approximately four minutes of operation, the maximum case temperature has peaked. It is difficult to extract the junction temperature from this side of the case, however, as no data has been provided in the MOSFET's datasheet for heat flow in that direction. It is



(a) High-side MOSFET hotspot temperatures.



(b) Low-side MOSFET hotspot temperatures.

Figure 5.28: MOSFET case hotspot temperatures over time, relative to the first measurement.

expected that the junction will be hotter, though by an indeterminate amount.

The temperature rises on phases A and B are significantly higher than that of phase C. Moreover, the temperatures of these transistors have yet to peak, though the data indicates would after several minutes pass. The testing of the inverter had to be

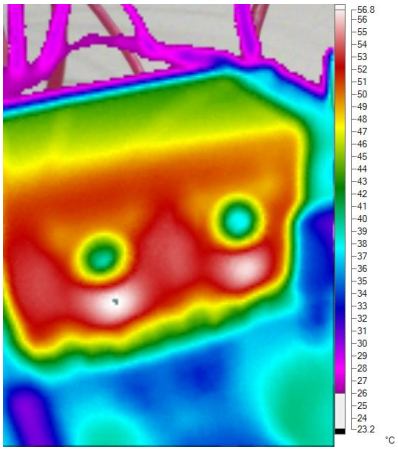
aborted before the peaking of the case temperature could be observed as the induction machine was being run in an overloaded condition and its internal temperatures were getting too high to continue to safely operate.

5.4 Summary

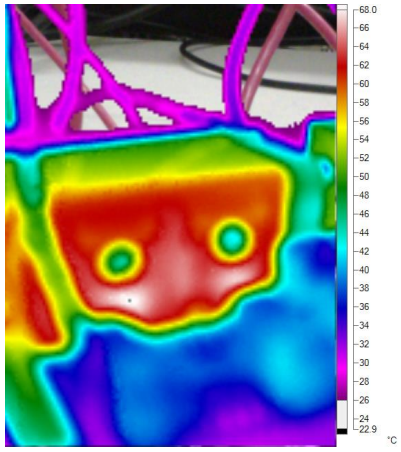
This chapter presented experimental results with the prototype inverter in two major regards: the first is in the analysis of the parasitic parameters and the second in the actual operation of the inverter.

The data and plots of the parasitics indicate that the PCB is well-designed with low inductance on the commutation loop. With low inductance, switching losses and overvoltages during switching operations can be minimised, thereby increasing the efficiency and reliability of the inverter. The resonance point of the DC-link capacitor matches that which was presented in its datasheet, showing that the measurements are good.

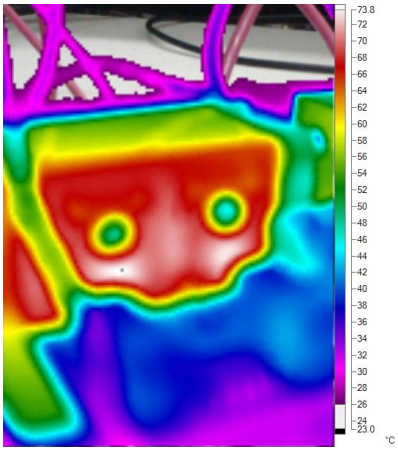
With respect to the testing of the inverter, it was shown that low power efficiency holds well with the simple linearised inductive switching model. Higher power testing–pessimistically estimated at around 12.3kW–showed that the inverter, with its current heatsinking solution, works well enough to switch in the vicinity of 15kW. However, the hot air being blown from the MOSFETs of phase C to A result in a large temperature gradient, with a difference in front-side case hotspots of 22°C after several minutes of operation, with the steady state not yet reached. The junction temperature will be higher than the value of the case, though by an indeterminate amount due to a lack of data with respect to the thermal resistances. This provides an opportunity for future work to design-in a superior heatsink.



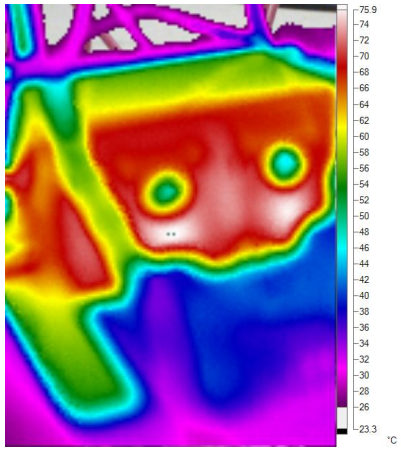
(a) $\Delta t = 0s$.



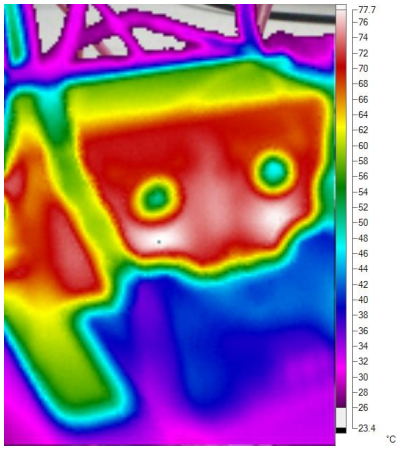
(b) $\Delta t = 95s$



(c) $\Delta t = 194s$.

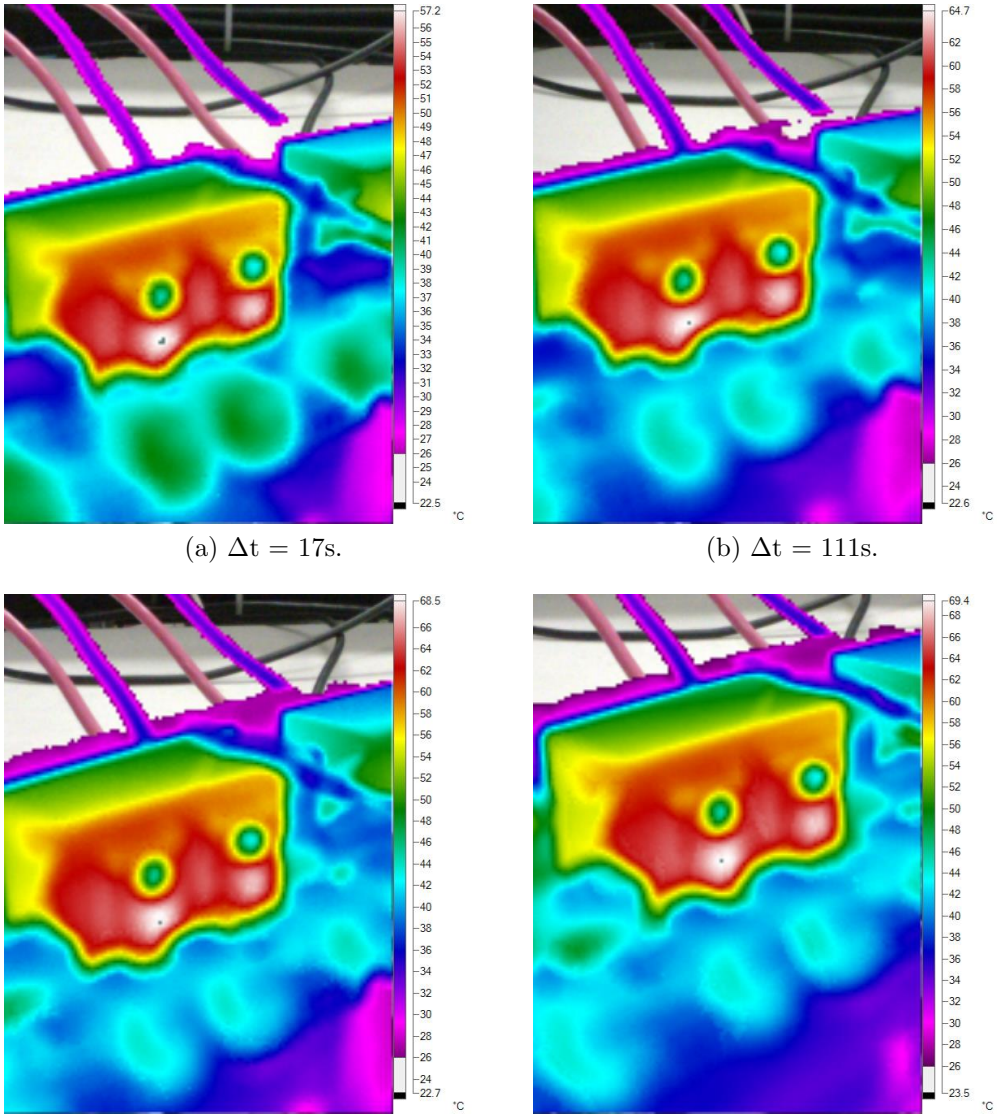


(d) $\Delta t = 239s$



(e) $\Delta t = 302s$

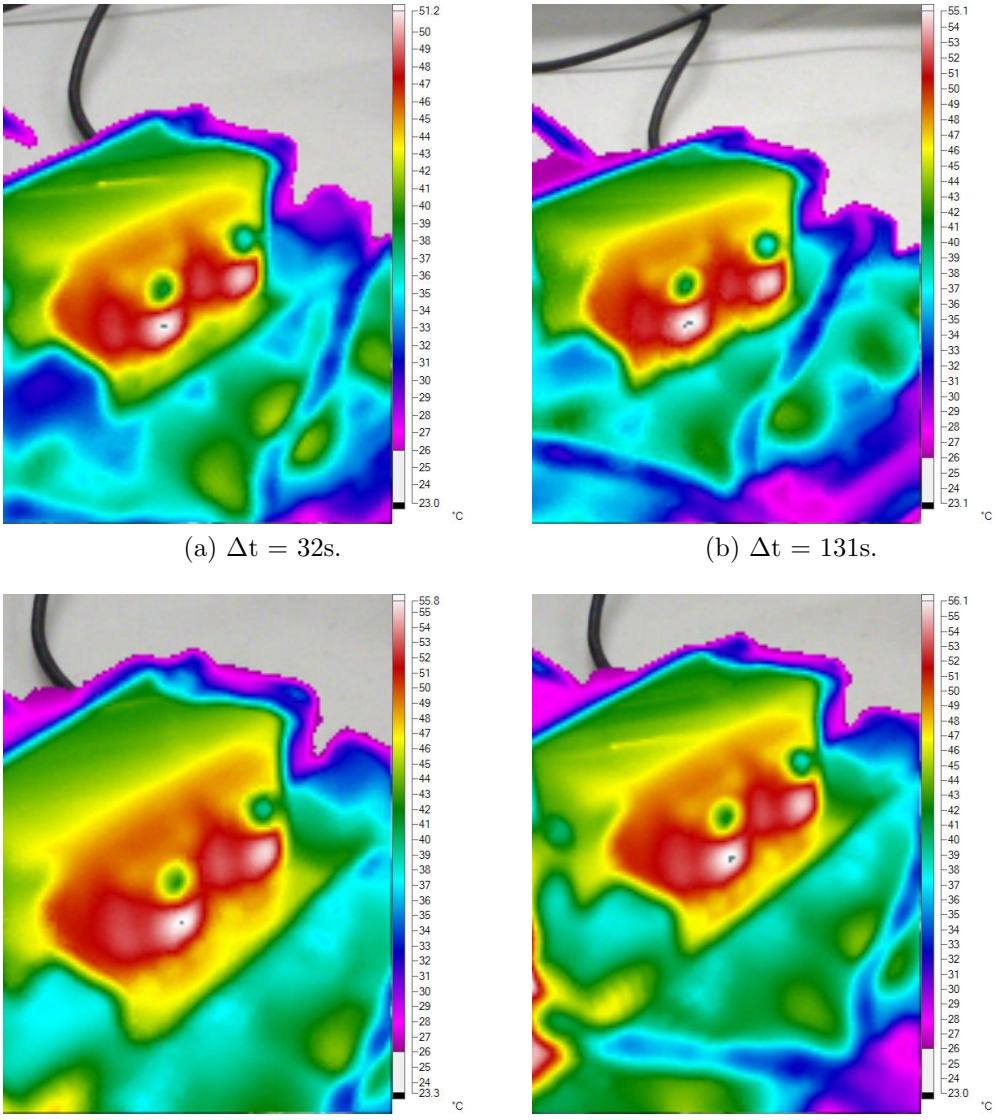
Figure 5.29: Phase A case temperatures over time, relative to the first measurement.



(a) $\Delta t = 17s$. (b) $\Delta t = 111s$.

(c) $\Delta t = 203s$. (d) $\Delta t = 252s$.

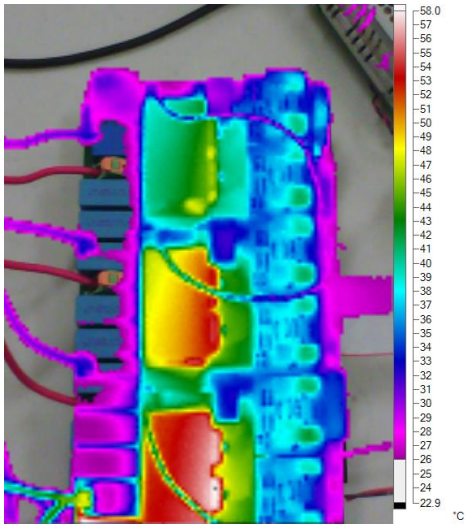
Figure 5.30: Phase B case temperatures over time, relative to the first measurement.



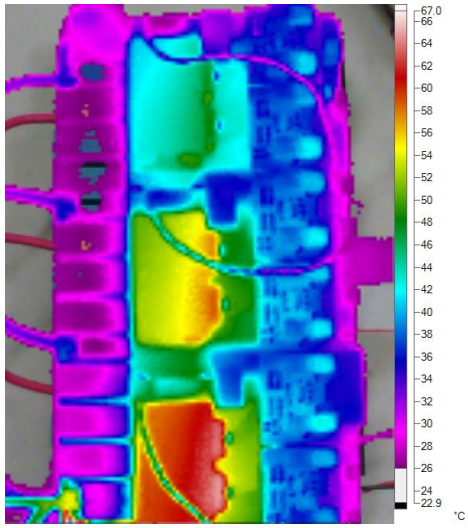
(a) $\Delta t = 32s$. (b) $\Delta t = 131s$.

(c) $\Delta t = 222s$. (d) $\Delta t = 261s$.

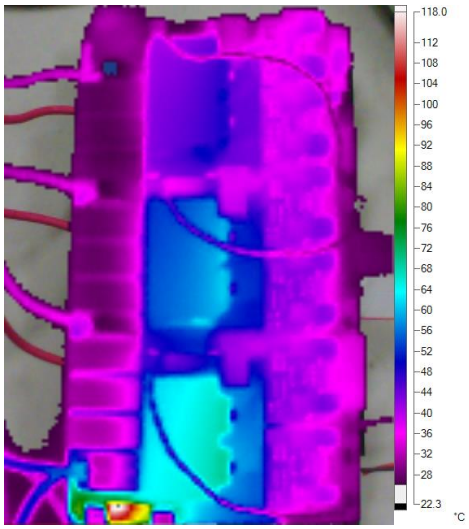
Figure 5.31: Phase C case temperatures over time, relative to the first measurement.



(a) Δt = 59s.



(b) Δt = 144s.



(c) Δt = 271s.

Figure 5.32: Heatsink temperatures over time, relative to the first measurement.

Chapter 6

Conclusions & Future Work

6.1 Conclusions

This thesis presented the analysis and design of a high power density three-phase inverter using simple techniques. A thorough review of figures of merit and modelling techniques, both for the switching and conduction losses, led to the development of an approach that can help a designer in determining which transistor will give the best performance out of a given group.

Novel work was undertaken for the discrete component selection problem, with a specific focus placed on DC-link capacitor selection. Several approaches were formulated and applied to determine which component would minimise several parameters while also having the best "fit," which is a belief of how well the item fits within the design, at the designer's discretion. The means by which the highly non-convex and non-linear problem could be optimised in a convex fashion were determined. Heuristic and pseudo-optimal methods were used as well, with the automated approach using the simulated annealing stochastic optimisation algorithm found to return a

result as good as that which was manually selected by progressively tightening a set of constraints, showing promise for automating a highly involved task.

Impedance analysis with an impedance analyser determined that the PCB designed for the inverter has low parasitic components and is well-designed. Altogether, under rated conditions, the power density of the assembly is slightly below 30kW, which is superior to other designs found in literature with the same, or worse, level of functionality. Greater functionality can be designed-in with the inclusion of an on-board controller.

Two sets of tests were conducted to assess the efficacy of the methods employed. The first was a low power arrangement that could accurately measure the efficiency of the inverter and the second was a higher power configuration to observe the temperature rise over ambient of the MOSFETs when subjected to an electrically equivalent load of approximately 12.5kW. The first tests matched the estimated efficiency quite closely, showing that the simple model employed can give a good estimate of the losses. The second testing showed that the thermal design of the converter needs work, with there being a significant temperature gradient from phase C to phase A, with the front-side case hotspot of phase A's MOSFETs being 20° higher than those of phase C. The low temperature rise of phase C indicates that, with a better cooling solution, the converter should be capable of reaching its rated power of 30kW.

Thus, it can be concluded that the techniques for electrical design presented herein are capable of producing a well-designed converter. It is the thermal aspect which is lacking and requires more work to allow for a designed converter to reach its rated levels.

6.2 Future Work

There exist several avenues of future work to be pursued. The first is to complete what could not be finished with the three-phase inverter: the development of a more comprehensive loss model; testing at rated voltages and currents; and efficiency measurements. Combined, these three major tasks will allow for the development of a full electrothermal model of the inverter, similar to what is shown in (Yang *et al.*, 2014) and (Ye *et al.*, 2014b).

The second grouping of future work involves an extension of the analyses undertaken in chapters 2 and 4: a comparative analysis between transistors of different semiconducting materials and technologies. This involves the development of an all-in-one double pulse testing setup for making an equal comparison between switching devices under the same operating conditions.

The last planned future work is to further develop and refine the optimal capacitor selection analysis introduced in sections 3.4 and 4.3. It is a relevant, practical problem requiring a robust solution. Once refined for capacitors, work can begin to extend it to other components that encounter similar issues: transistors, inductors and the like.

References

Ajram, S. and Salmer, G. (2001). Ultrahigh frequency DC-to-DC converters using GaAs power switches. *IEEE Transactions on Power Electronics*, **16**(5), 594–602.

Alkayal, F. and Saada, J. B. (2013). Compact three phase inverter in Silicon Carbide technology for auxiliary converter used in railway applications Keywords Advantages of SiC power switches comparing to Silicon ones for a power converter application. In *15th European Conference on Power Electronics and Applications (EPE)*, pages 1–10, Lille.

Alliance of Automobile Manufacturers (2016). ZEV Mandate.

Anwar, M. N. and Teimor, M. (2002). An analytical method for selecting Dc-link-capacitor of a voltage stiff inverter. In *Conference Record - IAS Annual Meeting (IEEE Industry Applications Society)*, volume 2, pages 803–810.

Arora, J. S., Huang, M. W., and Hsieh, C. C. (1994). Methods for optimization of nonlinear problems with discrete variables: A review. *Structural Optimization*, **8**(2-3), 69–85.

Atmel (2014). EMI Prevention in PCB Design of Atmel ARM-based Microcontrollers. Technical report, San Jose.

Balachandran, U., Ma, B., Lee, T., Emerson, J., and Dorris, S. (2014). Cost-Effective Fabrication of High-Temperature Ceramic Capacitors for Power Inverters.

Baliga, B. J. (1989). Power semiconductor device figure of merit for high-frequency applications. *IEEE Electron Device Letters*, **10**(10), 455–457.

Bertsimas, D. and Tsitsiklis, J. (1993). Simulated Annealing. *Statistical Science*, **8**(1), 10–15.

Biela, J., Badstuebner, U., and Kolar, J. W. (2009). Impact of Power Density Maximization on Efficiency of DC DC Converter Systems. *IEEE Transactions on Power Electronics*, **24**(1), 288–300.

Biela, J., Schweizer, M., Waffler, S., and Kolar, J. W. (2011). SiC versus Si - Evaluation of potentials for performance improvement of inverter and DC-DC converter systems by SiC power semiconductors. *IEEE Transactions on Industrial Electronics*, **58**(7), 2872–2882.

Bilgin, B., Magne, P., Malysz, P., Yang, Y., Pantelic, V., Preindl, M., Korobkine, A., Jiang, W., Lawford, M., and Emadi, A. (2015). Making the Case for Electrified Transportation. *IEEE Transactions on Transportation Electrification*, **1**(1), 4–17.

Blaabjerg, F. and Pedersen, J. K. (1997). Optimized Design of a Complete Three-Phase PWM-VS Inverter. *IEEE Transactions on Power Electronics*, **12**(3), 567–577.

Blaabjerg, F., Jaeger, U., Munk-Nielsen, S., and Pedersen, J. K. (1995). Power Losses in PWM-VSI Inverter Using NPT or PT IGBT Devices. *IEEE Transactions on Power Electronics*, **10**(3), 358–367.

Brown, J. (2004). Power MOSFET Basics : Understanding Gate Charge and Using it to Assess Switching Performance Power MOSFET Basics : Understanding Gate Charge and Using it to Assess Switching Performance.

Brown, J. (2006). Modeling the switching performance of a MOSFET in the high side of a non-isolated buck converter. *IEEE Transactions on Power Electronics*, **21**(1), 3–10.

Brown, J. and Moxey, G. (1995). Power MOSFET Basics : Understanding MOSFET Characteristics Associated With The Figure of Merit.

Dekkers, A. and Aarts, E. (1991). Global optimization and simulated annealing. *Mathematical Programming*, **50**(1-3), 367–393.

Elbeltagi, E., Hegazy, T., and Grierson, D. (2005). Comparison among five evolutionary-based optimization algorithms. *Advanced Engineering Informatics*, **19**(1), 43–53.

Emadi, A. (2015). *Advanced Electric Drive Vehicles*. CRC Press, Boca Raton.

Emadi, A., Williamson, S. S., and Khaligh, A. (2006). Power Electronics Intensive Solutions for Advanced Vehicular Power Systems. *IEEE Transactions on Power Electronics*, **21**(3), 567–577.

Emadi, A., Lee, Y. J., and Rajashekara, K. (2008). Power Electronics and Motor Drives in Electric, Hybrid Electric, and Plug-In Hybrid Electric Vehicles. *IEEE Transactions on Industrial Electronics*, **55**(6), 2237–2245.

Eull, M., Preindl, M., and Emadi, A. (2016). Analysis and Design of a High Efficiency, High Power Density Three-Phase Silicon Carbide Inverter. In *2016 IEEE*

Transportation Electrification Conference and Expo (ITEC), pages 1–6, Dearborn, MI. IEEE.

Gálvez, A. and Iglesias, A. (2012). Particle swarm optimization for non-uniform rational B-spline surface reconstruction from clouds of 3D data points. *Information Sciences*, **192**, 174–192.

Garcia-Rodriguez, L., Jones, V., Balda, J. C., Lindstrom, E., Oliva, A., and Gonzalez-Llorente, J. (2014). Design of a GaN-based microinverter for photovoltaic systems. In *2014 IEEE 5th International Symposium on Power Electronics for Distributed Generation Systems, PEDG 2014*.

Glaser, J. S., Nasadoski, J. J., Losee, P. A., Kashyap, A. S., Matocha, K. S., Garrett, J. L., and Stevanovic, L. D. (2011). Direct comparison of silicon and silicon carbide power transistors in high-frequency hard-switched applications. In *Conference Proceedings - IEEE Applied Power Electronics Conference and Exposition - APEC*, pages 1049–1056, Fort Worth.

Gold Phoenix (2012). Knowledge Center.

Graovac, D., Pürschel, M., and Kiep, A. (2006). MOSFET Power Losses Calculation Using the Data- Sheet Parameters. Technical Report July.

Gueguen, P. (2015). Market & Technology trends in Wide BandGap power packaging. In *Applied Power Electronics Conference and Exposition (APEC)*.

Guo, J., Ge, H., Ye, J., and Emadi, A. (2015). Improved method for MOSFET voltage rise-time and fall-time estimation in inverter switching loss calculation. In

2015 IEEE Transportation Electrification Conference and Expo, ITEC 2015, pages 1–6.

Gurpinar, E. and Castellazzi, A. (2016). Single-Phase T-Type Inverter Performance. *IEEE Transactions on Power Electronics*, **31**(10), 7148–7160.

Havanur, S. and Zuk, P. (2015). Power MOSFET Basics: Understanding Superjunction Technology.

Horio, M., Iizuka, Y., Ikeda, Y., Mochizuki, E., and Takahashi, Y. (2012). Ultra compact and high reliable SiC MOSFET power module with 200C operating capability. In *Proceedings of the International Symposium on Power Semiconductor Devices and ICs*, number June, pages 81–84, Bruges.

Hou, R., Magne, P., Bilgin, B., and Emadi, A. (2015). A topological evaluation of isolated DC/DC converters for Auxiliary Power Modules in Electrified Vehicle applications. In *Conference Proceedings - IEEE Applied Power Electronics Conference and Exposition - APEC*, pages 1360–1366.

Huang, A. Q. (2004). New unipolar switching power device figures of merit. *IEEE Electron Device Letters*, **25**(5), 298–301.

Huang, X., Liu, Z., Li, Q., and Lee, F. C. (2014). Evaluation and application of 600 V GaN HEMT in cascode structure. *IEEE Transactions on Power Electronics*, **29**(5), 2453–2461.

Ingber, L. (1993). Simulated annealing: Practice versus theory. *Mathematical and Computer Modelling*, **18**(11), 29–57.

Jahdi, S., Alatise, O., Fisher, C., Ran, L., and Mawby, P. (2014). An Evaluation of Silicon Carbide Unipolar Technologies for Electric Vehicle Drive-Trains. *IEEE Journal of Emerging and Selected Topics in Power Electronics*, **2**(3), 517–528.

Jeong, S.-G. and Park, M.-H. (1991). The analysis and compensation of dead-time effects in PWM inverters. *IEEE Transactions on Industrial Electronics*, **38**(2), 108–114.

Johnson, E. O. (1966). Physical limitations on frequency and power parameters of transistors. In *IRE International Convention Record*, volume 13, pages 27–34.

Jones, E. a., Wang, F., and Ozpineci, B. (2014). Application-based review of GaN HFETs. In *2nd IEEE Workshop on Wide Bandgap Power Devices and Applications, WiPDA 2014*, pages 24–29.

Kazimierczuk, M. K. (2009). *High Frequency Magnetic Components*. John Wiley & Sons, Ltd., West Sussex, third edition.

Khan, M., Magne, P., Bilgin, B., Wirasingha, S., and Emadi, A. (2014). Laminated Busbar Design Criteria in Power Converters for Electrified Powertrain Applications. In *2014 IEEE Transportation Electrification Conference and Expo (ITEC)*, pages 1–6, Dearborn, MI.

Kim, I.-J., Matsumoto, S., Sakai, T., and Yachi, T. (1995). New power device figure of merit for high-frequency applications. In *Proceedings of International Symposium on Power Semiconductor Devices and IC's: ISPSD '95*, number 1, pages 309–314.

Kolar, J. and Round, S. (2006). Analytical calculation of the RMS current stress on

the DC-link capacitor of voltage-PWM converter systems. *IEE Proceedings-Electric Power Applications*, **153**(4), 535–543.

Magne, P., Liu, P., Bilgin, B., and Emadi, A. (2015). Investigation of impact of number of phases in interleaved dc-dc boost converter. In *2015 IEEE Transportation Electrification Conference and Expo (ITEC)*, pages 1–6.

McArthur, R. (2001). Making Use of Gate Charge Information in MOSFET and IGBT Data Sheets. Technical report.

Merkert, A., Krone, T., and Mertens, A. (2014). Characterization and scalable modeling of power semiconductors for optimized design of traction inverters with si-and sic-devices. *IEEE Transactions on Power Electronics*, **29**(5), 2238–2245.

Mohan, N., Undeland, T. M., and Robbins, W. P. (2003). *Power Electronics: Converters, Applications and Design*. John Wiley & Sons, Inc., Hoboken, third edition.

Ozpineci, B. (2002). *System impact of silicon carbide power electronics on hybrid electric vehicle applications*. Ph.D. thesis, University of Tennessee, Knoxville.

Pelletier, P., Guichon, J.-M., Schanen, J.-L., and Frey, D. (2009). Optimization of a DC Capacitor Tank. *IEEE Transactions on Industry Applications*, **45**(2), 880–886.

Preindl, M. and Bolognani, S. (2011). Optimized design of two and three level full-scale voltage source converters for multi-MW wind power plants at different voltage levels. In *IECON Proceedings (Industrial Electronics Conference)*, pages 3634–3639.

Ren, Y., Xu, M., Zhou, J., and Lee, F. (2006). Analytical loss model of power MOSFET. *IEEE Transactions on Power Electronics*, **21**(2), 310–319.

Reusch, D. and Strydom, J. (2014). Understanding the effect of PCB layout on circuit performance in a high-frequency gallium-nitride-based point of load converter. *IEEE Transactions on Power Electronics*, **29**(4), 2008–2015.

Reusch, D. and Strydom, J. (2015). Evaluation of Gallium Nitride Transistors in High Frequency Resonant and Soft-Switching DCDC Converters. *IEEE Transactions on Power Electronics*, **30**(9), 5151–5158.

Rodriguez, L. A. G., Williams, E., Balda, J. C., and Stewart, C. (2013). A Comparison of Selected Silicon and Silicon-Carbide Switching Devices for PV Microinverter Applications. In *2013 4th IEEE International Symposium on Power Electronics for Distributed Generation Systems (PEDG)*, pages 1–7, Rogers, AR. IEEE.

Rodríguez, M., Rodríguez, A., Miaja, P. F., Lamar, D. G., and Zúniga, J. S. (2010). An insight into the switching process of power MOSFETs: An improved analytical losses model. *IEEE Transactions on Power Electronics*, **25**(6), 1626–1640.

Rogers, S. (2012). Electric Drive Status and Challenges.

ROHM Semiconductor (2015). SCT2120AF N-channel SiC power MOSFET datasheet.

Rosa, E. B. (1908). The self and mutual inductances of linear conductors. *Bulletin of Materials Science*, **4**(2), 301–344.

Sasaki, K., Sato, S., Matsui, K., Murakami, Y., Tanimoto, S., and Tanisawa, H. (2013). 40 kW/L High Switching Frequency Three-Phase AC 400 V All-SiC Inverter. *Materials Science Forum*, **740-742**, 1081–1084.

Sato, S., Matsui, K., Zushi, Y., Murakami, Y., Tanimoto, S., Sato, H., and Yamaguchi, H. (2011). Forced-Air-Cooled 10 kW Three-Phase SiC Inverter with Output Power Density of More than 20 kW/L. *Materials Science Forum*, **679-680**, 738–741.

Sedra, A. S. and Smith, K. C. (2010). *Microelectronic Circuits*. Oxford University Press, New York, sixth edition.

Shang, F., Arribas, A. P., and Krishnamurthy, M. (2014). A comprehensive evaluation of SiC devices in traction applications. In *2014 IEEE Transportation Electrification Conference and Expo (ITEC)*, pages 1–5, Dearborn, MI. IEEE.

Suzuki, K. and Masuoka, F. (2015). Technologies for Seventh Generation Power Chips. Technical report, Mitsubishi Electric.

Tolbert, L. M., Ozpineci, B., Islam, S. K., and Chinthavali, M. (2003). Comparison of Wide Bandgap Semiconductors for Power Applications. In *10th European Conference on Power Electronics and Applications*, pages 1–7, Toulouse.

Wang, H. (2007). *Investigation of Power Semiconductor Devices for High Frequency High Density Power Converters*. Ph.d, Virginia Polytechnic Institute and State University.

Wang, H. and Blaabjerg, F. (2014). Reliability of capacitors for DC-link applications in power electronic converters–an overview. *IEEE Transactions on Industry Applications*, **50**(5), 3569–3578.

Wang, J., Chung, H. S.-h., and Li, R. T.-h. (2013). Characterization and experimental assessment of the effects of parasitic elements on the MOSFET switching performance. *IEEE Transactions on Power Electronics*, **28**(1), 573–590.

Whitaker, B., Barkley, A., Cole, Z., Passmore, B., Martin, D., McNutt, T. R., Lostetter, A. B., Lee, J. S., and Shiozaki, K. (2014). A high-density, high-efficiency, isolated on-board vehicle battery charger utilizing silicon carbide power devices. *IEEE Transactions on Power Electronics*, **29**(5), 2606–2617.

Wrzecionko, B., Bortis, D., and Kolar, J. W. (2014). A 120C Ambient Temperature Forced Air-Cooled Normally-off SiC JFET Automotive Inverter System. *IEEE Transactions on Power Electronics*, **29**(5), 2345–2358.

Xie, W. C., Zou, X. F., Yang, J. D., and Yang, J. B. (2012). Iteration and optimization scheme for the reconstruction of 3D surfaces based on non-uniform rational B-splines. *Computer-Aided Design*, **44**(11), 1127–1140.

Xiong, Y., Sun, S., Jia, H., Shea, P., and Shen, Z. J. (2009). New physical insights on power MOSFET switching losses. *IEEE Transactions on Power Electronics*, **24**(2), 525–531.

Yang, K., Guo, J., Ge, H., Bilgin, B., Loukanov, V., and Emadi, A. (2014). Transient electro-thermal analysis for a MOSFET based traction inverter. In *2014 IEEE Transportation Electrification Conference and Expo (ITEC)*, pages 1–6.

Ye, H. (2014). *Reliability Improvements in Dual Traction Inverters for Hybrid Electric Vehicles*. Ph.d, McMaster University.

Ye, H., Bilgin, B., and Emadi, A. (2012a). Reduced-parts three-phase inverters: A comparative study. In *2012 IEEE Transportation Electrification Conference and Expo, ITEC 2012*, pages 1–6.

Ye, H., Yang, Y., and Emadi, A. (2012b). Traction inverters in hybrid electric vehicles. In *2012 IEEE Transportation Electrification Conference and Expo, ITEC 2012*, pages 1–6.

Ye, H., Magne, P., Bilgin, B., Wirasingha, S., and Emadi, A. (2014a). A Comprehensive Evaluation of Bidirectional Boost Converter Topologies for Electrified Vehicle Applications. In *40th Annual Conference of the IEEE Industrial Electronics Society, IECON 2014*, pages 2914–2920.

Ye, H., Yang, K., Ge, H., Magne, P., and Emadi, A. (2014b). A drive cycle based electro-thermal analysis of traction inverters. In *2014 IEEE Transportation Electrification Conference and Expo (ITEC)*, pages 1–6.

Yilmaz, M. and Krein, P. T. (2012). Review of Battery Charger Topologies, Charging Power Levels, and Infrastructure for Plug-In Electric and Hybrid Vehicles. *IEEE Transactions on Power Electronics*, **28**(5), 2151–2169.

Zhang, H., Tolbert, L. M., and Ozpineci, B. (2011). Impact of SiC devices on hybrid electric and plug-in hybrid electric vehicles. *IEEE Transactions on Industry Applications*, **47**(2), 912–921.