# A Stochastic Optimization Technique for Discrete DC Capacitor Bank Design

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Abstract—The DC capacitor bank is an expensive and bulky component, particularly in automotive applications. Its selection is subject to a number of competing constraints and is often sub-optimal. This paper proposes a generalized design methodology for the capacitor bank and introduces several optimization approaches under the umbrellas of convex, heuristic and pseudo optimization. Simulated annealing, a stochastic heuristic optimization algorithm, features prominently and shows good promise for automated selection. The discussed methods are assessed relative to one another for the design of the inverters and it was found that simulated annealing was able to reliably find the global minimum of the dataset, as well as returning solutions that were marginally less optimal than the ones obtained through careful manual optimization. The technique is general enough such that it can be applied to other components in a converter.

# I. INTRODUCTION

Demand for power electronic converters is growing rapidly with consumers and industry requiring smaller, cheaper and more efficient systems. System cost and volume are significant constraints, particularly for the automotive sector, where stringent targets have been laid out to drive vehicle costs down and fuel economy and adoption up [1]. To reach these, it becomes necessary to optimize the components in the system. Capacitors are no exception, given their ubiquity.

Little literature focuses on the problem of optimal discrete DC capacitor bank design and the subsequent component selection. Many focus on power level sizing and placement of capacitor banks for AC power distribution and reactive power compensation. For power electronic applications, many papers have considered the optimization of other facets of a design: the materials used to manufacturer power transistors [2]; converter topology to minimize voltage and current ripple [3], [4]; the control to minimize ripple [5], [6]; the gate drive voltages and output current for achieving maximum efficiency [7]; and the switching frequency [8]. Others have skirted the issue and considered preferred sizings, both in terms of capacitance and volume, but have not worked towards selecting an exact component [8]–[10].

Two studies, however, have broached the particular subject of interest, though not in any formal optimization sense. In [11], the authors analyzed the harmonic content of an inverter and determined which capacitor(s) from a dataset would best handle the resultant ripple current and minimize EMI. The second publication, [12], is similar in nature: a database of capacitors is prepared and their characteristics are evaluated using a cost function with the lowest cost electrolytic and film capacitors being selected. The use of two types of capacitors and a cost function are the most significant differences from [11]. Different technologies are used as each has a different frequency response, which helps to reduce EMI.

The aforementioned studies have problems, however. For the former, once a suitable device was found the algorithm terminated; in the latter, the entire database needed to be evaluated. Furthermore, the paralleling of electrolytic and film capacitors was encouraged, which is worrying from a reliability standpoint [13]. Considering that capacitors are a regular failure point in power electronic converters and they occupy significant space at high cost–35%, 23% and 23% of the volume, weight and cost, respectively [14]–a better approach is needed.

With these considerations in mind, this paper seeks to present a simple analysis technique for both designing and selecting the DC capacitor bank of a power electronic converter from a set of commercially available components. Several classes of optimization methods are discussed and applied to the design of two three-phase inverters. Their outputs are compared with the capacitor bank that was manually selected for each converter and conclusions are drawn.

## **II. OPTIMIZATION METHODS**

Three major categories of optimization are briefly introduced in this section. Several techniques are discussed for each grouping that were found to be effective in framing the problem and performing the optimizations themselves.

# A. Convex

A convex function is the ideal scenario when approaching an optimization problem as it guarantees that there exists only one minimum, which is the global minimum. Discrete optimization is an inherently non-convex problem as the data is not continuous. The component selection problem, which is discrete, is highly nonlinear and non-convex and, oftentimes, without any real pattern. Thus, a convex representation is unachievable without significant adjustments to the data itself.

One way to transform such a problem into a convex one is to employ the convex hull. While the convex hull intrinsically performs a discrete-to-continuous relaxation, it is beneficial to make it explicit; i.e.,

$$[D \mid D \in \mathbb{Z}_+\} \to \{D^* \mid D^* \in \mathbb{R}_+\},\tag{1}$$

where D represents the set of design parameters with discrete values and  $D^*$  is the relaxed, continuous set of parameters. It is also assumed that every parameter has a value greater than zero, as non-positive numbers would not be physically realizable.

Applying the convex hull, per (2), the system is bounded in a convex fashion. The application of the convex hull to two capacitor parameters from the dataset used in this work is shown in Fig. 1.

$$Co(D) = \cap \{D^* \mid D \subseteq D^*, \ D^* \text{ convex}\}$$
(2)



Fig. 1: The 2D convex hull.

The convex hull returns the coordinates of the extremities of the dataset. Using this information, a series of linear equations can be inferred and solved as an optimization problem of the form of (3) via linear programming or interior point methods.

$$\begin{array}{l} \underset{x}{\text{minimize}} \quad c^T x \\ \text{subject to} \quad Ax < b \end{array}$$
(3)

### B. Heuristic

Heuristic methods fill the gap where convex ones fail, which include when the function is non-convex or nonlinear, is prohibitively difficult to optimize analytically, or no analytical function exists. Heuristic methods tend to find a "close enough" solution which, depending on the problem at hand, may be acceptable.

Evolutionary algorithms, such as the genetic algorithm (GA) and particle swarm optimization (PSO), fall under the umbrella of heuristic optimization.

1) Pareto Optimality: Pareto optimality involves determining what is called the trade-off curve, or Pareto front, where one parameter can only be made better by making the other worse. In this way, a set of the "best" solutions can be provided to the decision maker (DM) for final analysis. An example of the Pareto front is shown in Fig. 2.



A drawback to this approach is that more than one feasible solution is returned to the DM, thus requiring human involvement, which may be undesirable. Conversely, depending on the problem, it may be advantageous for a human to be involved. The capacitor selection problem is one such example: Depending on the contents of the dataset, some components may not be commercially available or they may not have the best *fit* (e.g. the package is not volumetrically efficient in-system). A method that returns only one solution, then, may still need human involvement to manually adjust either the dataset or the constraints to avoid such pitfalls, rendering the emphasis on automation null and void.

2) Simulated Annealing: Simulated annealing uses stochastic methods to converge to a solution. A thorough treatment of the subject can be found in [15]–[17]. Probabilistically, it is capable of converging on the global minimum, which is encouraging when seeking the optimal solution.

The first step in the algorithm is to compute the acceptance probability, which is calculated as

$$p(T) = \begin{cases} \exp\left(-\left(\frac{E_{n+1}-E_n}{T}\right)\right), & \text{if } E_{n+1}-E_n \ge 0\\ 1, & \text{if } E_{n+1}-E_n < 0, \end{cases}$$
(4)

where  $E_{n+1}$  and  $E_n$  are the next energy state and current energy state, respectively; and T is the so-called temperature.

The acceptance probability is a number over the range [0, 1] that is used to determine whether a move should be accepted or rejected. The result from (4) is compared to a number drawn from a probability distribution–normally the uniform distribution–and a decision is made, per (5),

$$E = \begin{cases} E_{n+1}, & \text{if } p(T) \ge \rho \\ E_n, & \text{if } p(T) < \rho, \end{cases}$$
(5)

with  $\rho$  being a number drawn from the probability distribution. The comparison of p(T) with  $\rho$  allows for local minima to be escaped from by allowing movement to higher energy states in the hope of eventually converging on a lower value.

The selection of the neighbour,  $E_{n+1}$ , which is a potential next position for the algorithm, can be done in a multitude

of ways using any preferred probability distribution. It can be calculated as

$$n_{i+1} = n_i + X \times T,\tag{6}$$

where  $n_i$  is the current position in the data set and X is a random variable, drawn from a probability distribution of choice, with adjustments made, depending on the distribution, to allow for negative values, thereby enabling backwards movement in the dataset. For example, a Gaussian distribution would be biased towards its mean, whereas a uniform distribution would have less predictable movement.

As the temperature is lowered, an optimal solution should be approached; hence, at low T, movement when  $E_{n+1} > E_n$ is not favoured and simulated annealing becomes the greedy algorithm, where the program seeks only to minimize the system energy, E.

# C. Pseudo-Optimal

Pseudo-optimality is the process of finding the best solution within a dataset without using any explicit optimization technique. This is a significant step away from the previous two categories which relied on, to some degree, a mathematical formulation and solution of the problem at hand.

Pseudo-optimality permits arbitrary means of solution; hence, there are infinitely many approaches that can be taken, depending on how the DM wishes to find a solution. Only two will be discussed herein.

1) Brute Force: The brute force algorithm moves through the dataset, from the first entry to the last, searching out specific pieces of data. It has many permutations, with a popular one being to find the single smallest (or largest) metric(s) in the dataset. This approach was used in [12] to find the capacitor with lowest cost, per the authors' cost function. This technique has the added benefit of requiring no DM influence, assuming the returned result is to be automatically accepted.

This technique can be written in the form of an optimization problem despite not being an optimization per se. The expression is

$$\begin{array}{ll} \underset{f(x) \in \mathbb{R}^{n \times m}}{\text{minimize}} & f(x) \\ \text{subject to} & f_i(x) \leq c_i, \quad i = 1, \dots, n \\ \text{subject to} & x \in \mathbb{R}^m, \end{array}$$
(7)

where f(x) is a matrix with dimensions of the number of capacitor banks under evaluation, m, and the number of capacitor bank parameters to be constrained, n. The constraints,  $c_i$ , are applied such that each  $f_i(x)$  is less than a designer prescribed value. An example operation is shown in Fig. 3, where individual and coupled parameters are minimized. The designer must be careful in selecting which parameter to optimize as optimality in one may lead to sub-optimality in the other(s).



Fig. 3: Brute force algorithm results with different constraints.

2) Sequential Tightening: The sequential tightening approach applies an initial set of constraints and finds objects that satisfy them. Once the components are returned, the DM applies his/her insight and determines whether they need to be tightened or loosened, thereby increasing or decreasing the number of feasible solutions at every iteration.

This technique can be thought of as a reformulation of the constrained optimization problem of (7) to one of epigraph form, where the function is placed in the constraints and a vector of parameters, t, is tightened (loosened) until a satisfactory result is found. This is written as (8). In this way, it is made clear that the process is iterative in nature. However, it must be noted that the DM is involved at every step of t as, without this human influence, the algorithm would become the aforementioned brute force approach.

$$\begin{array}{ll} \underset{t \in \mathbb{R}^n}{\text{minimize}} & \mathbf{t} \\ \text{subject to} & f_i(x) \leq c_i, \quad i = 1, \dots, n \\ \text{subject to} & c_i = t_i, \qquad i = 1, \dots, n \\ \text{subject to} & x \in \mathbb{R}^m \end{array}$$
(8)

Sequential tightening was the method by which the capacitor bank of the inverter of [18] was designed. A special emphasis was placed on the height as it was found to be the driving factor in a volumetrically efficient and, consequently, power dense design. The first and last steps of the process are shown in Fig. 4, along with the selected capacitor.

An advantage of this method is the high level of DM involvement, which helps to guide the process to a result that best fits the design and avoids pitfalls such as components that are not commercially available. However, this is also a drawback insofar as automation is low.

## D. Additional Remarks

Nothing precludes the synthesis of different categories; indeed, in [19], the authors used PSO to build a continuous function from scattered discrete data points. However, since the function will likely be highly non-convex and nonlinear, little is gained by pursuing surface fitting.



Fig. 4: First and last steps of sequential tightening.

# III. OPTIMIZATION METHODOLOGY

In this paper, a two-step process is proposed to find the optimal device and design. By breaking the problem in two, the method can be easily adjusted to handle a wide range of problems. The purpose of such an approach is to decouple the problem from the solution. The first step is the preprocessing of the data, which generates the dataset to be optimized; the second step is to apply an optimization algorithm that the designer believes will deliver a satisfactory result.

This process was used to design the DC capacitor bank of two three-phase inverters, both of which are shown in Fig. 5. The overarching goal of the designs was to maximize the power density, which is calculated as

$$\rho_p = \frac{P_{out}}{Vol},\tag{9}$$

where  $P_{out}$  is the output power of the system and Vol is the volume, measured in cubic decimetres (dm<sup>3</sup>) or, equivalently, litres (L).

#### A. Dataset Preprocessing

The preprocessing of the dataset is accomplished by subjecting the raw data-in this case, a database of individual capacitors with their datasheet characteristics-to a series of



(b) The designed dual inverter.

Fig. 5: The two highly power dense inverters.

constraints imposed by the design. The capacitor banks are designed to meet the system specifications using one unique part number per bank. This generates the set of solutions.

The minimum design of the DC-link capacitor bank is dictated by the DC-link voltage, its expected overshoot and the ripple current to be sustained. The number of series and parallel components can be expressed as

$$n_s = \left\lceil \max\left(\frac{V_{DC}}{V_R}, \frac{V_{pk}}{V_S}\right) \right\rceil \tag{10}$$

$$n_p = \left| \left( \frac{I_{C,RMS}}{I_C} \right) \right|,\tag{11}$$

where  $\lceil . \rceil$  is the ceiling operator;  $V_{DC}$  is the DC-link voltage;  $V_R$  is the rated voltage of the capacitor;  $V_{pk}$  is the transient voltage arising from the switching operations;  $V_S$  is the surge voltage rating of the capacitor;  $I_{C,RMS}$  is the expected ripple current to be sunk by the capacitor; and  $I_C$  is the ripple current rating of the capacitor.

The DC-link ripple current for a three-phase inverter can be estimated as [20]

$$I_{C,RMS} \approx \frac{I_{\phi,RMS}}{\sqrt{2}},$$
 (12)

where  $I_{\phi,RMS}$  is the per-phase load RMS current, which is assumed to be equal across all three phases. This approximation is valid for power factors near unity. As the power factor reduces so, too, does the value of the ripple current. Together, (10) and (11) fully define the minimum characteristics of a proposed solution. It may be beneficial, however, to include other constraints and metrics. For example, if the voltage ripple is to be kept at a certain level, then (11) can be rewritten as

$$n_p = \left\lceil \max\left(\frac{I_{C,RMS}}{I_C}, \frac{n_s \cdot C_{DC}}{C}\right) \right\rceil,\tag{13}$$

with C being the rated capacitance obtained from each capacitor's datasheet and  $C_{DC}$  the required capacitance of the DC-link to obtain a certain voltage ripple.

The required DC-link capacitance can be estimated as [10]

$$C_{DC} \approx \frac{I_{\phi,RMS}}{4\Delta V_{DC(\%)} V_{DC} f_s},\tag{14}$$

where  $f_s$  is the switching frequency of the transistors.

The total number of capacitors required to meet the base specifications is the product of the required number of series and parallel capacitors, as expressed by (15).

$$N = n_s \times n_p \tag{15}$$

## B. Optimization

The second step in the process is to perform the optimization. This involves deciding what parameters are to be minimized, e.g. volume, power losses, surface area; whether one or several results are desired; and what technique should be employed. The last point is not trivial and, indeed, requires careful thought on the DM's part. For example, if the dataset is very large, then the brute force technique may be unacceptably slow, whereas poor constraint selection may render sequential tightening to be ineffective.

The choice of what parameter(s) is (are) to be minimized can lead to non-optimal solutions in others. Take, for example, Fig. 3: when only the losses are to be minimized, the volume is unacceptably high whereas, when the volume is to be minimized, the losses are low. A compromise, where the two are minimized, yields a good compromise. Similar results are obtained when using simulated annealing on the problem.

Hence, it is advantageous to couple parameters together to guide the solver to a more balanced solution. This can be achieved by employing a cost function. The cost function can take any form or level of complexity that the DM desires. In this work, a simple weighted sum is employed of the form

$$J_n = \sum \left( w_1 v_{1,n} + w_2 v_{2,n} + \dots + w_k v_{k,n} \right), \qquad (16)$$

where  $w_k$  is the weight of the k-th design variable under consideration and  $v_{k,n}$  is the value of the k-th design variable of the n-th capacitor bank.

## **IV. OPTIMIZATION RESULTS**

The figures presented pertain to the Silicon Carbide inverter of Fig. 5 (a). The capacitor bank was designed in [18] using sequential tightening, which acts as a benchmark for the performance of the other optimization algorithms.

The cost function of (16) was used to generate a cost for the data which was then fed into all algorithms. The results of the optimizations in terms of solver time and other relevant design parameters for each inverter are given in Table I. While sequential tightening did not achieve the lowest cost in both cases, the difference is not substantial when looking at a plot of the film capacitor bank costs (Fig. 6 (a)). For the dual inverter, the lowest volume did not correspond to the lowest cost. This is because the number of capacitors was penalized and, for an equivalent capacitor bank, 103 components would be required.

Specifically targeting the efficacy of simulated annealing, Fig. 6 shows the results of 10 runs of the algorithm on the cost function and its subsequent mapping to the dataset when considering the volume and power losses. The global minimum and a near-optimal local minimum are returned in cost which, when plotted on the dataset, show a good result.



(b) Algorithm output plotted on the film capacitor dataset.

Fig. 6: Ten runs of simulated annealing and the results.

The performance of simulated annealing can be graphically compared with the manually chosen capacitor of sequential tightening via Fig. 7. Both simulated annealing solutions have a lower cost and fewer capacitors in the bank; however, only one is smaller and has lower losses, whereas the other is comparable in both categories. The most important difference, though, is in height. The returned solutions have a height of 35mm and, thus, would be the inverter's tallest components, thereby increasing the system's volume. In that sense, they are sub-optimal solutions and the nuances of the design could

TABLE I: Optimization methods and their performance.

Optimization Method	Silicon Carbide Inverter				Dual Inverter			
	Time (ms)	Volume (dm <sup>3</sup> )	Height (mm)	Cost, J (k)	Time (ms)	Volume (dm <sup>3</sup> )	Losses (W)	Cost, J (k)
Convex	198.8	0.09	35	2.63	187.4	2.80	32	26.1
Pareto Optimality	0.45	[0.09, 2.57]	[25, 108]	[2.63, 49.1]	0.57	[2.80, 41.76]	[20, 601]	[26.1, 603.1]
Simulated Annealing	4.70	0.09, 0.12	35, 35	2.63, 3.43	4.8	2.80, 2.31	32, 18.6	26.1, 66.1
Brute Force	0.87	0.09	35	2.63	0.64	2.80	32	26.1
Sequential Tightening	18	0.11	25	4.37	1.5	3.20	32	85.4

not be captured by the algorithm without significant designer insight and influence.



Fig. 7: Manual (red) and automated (otherwise) selections.

### V. CONCLUSION

In this paper, a two-step method for the design and selection of DC capacitor banks was proposed. Several optimization methods were discussed and examined in detail. A novel approach to the selection process was introduced through the use of the simulated annealing algorithm to stochastically find optimal and near-optimal designs. Using this methodology, two highly power dense three-phase inverters were designed with the capacitor bank carefully selected by sequential tightening. The performance of the other optimization methods were assessed relative to sequential tightening and were shown to find the global optimum quickly and reliably. In terms of computational effort and accuracy, simulated annealing was shown to be a viable method for solving the discrete component selection problem.

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