A Balanced and Vertically Stacked Multilevel Power Converter Topology with Linear Component Scaling

Matthew Jahnes
Columbia University
matthew.jahnes@columbia.edu

Bernard Steyaert
Columbia University
bernard.steyaert@columbia.edu

Matthias Preindl
Columbia University
matthias.preindl@columbia.edu

***Abstract*—This paper proposes a novel multi-level power converter topology that is an adaptation of existing topologies. This topology is fully balanced, can function bidirectionally for both DC/AC and DC/DC modes of operation, and can be expanded to an unrestricted N levels. It is comprised of discrete switching cells across which the input voltage can be arbitrarily distributed. Each switching cell can operate as a standalone unit and is individually controllable. Fundamental equations for each cell and the converter as a whole are derived alongside methods for expanding to N levels. Validation of this topology and its fundamental equations are shown through high-fidelity simulation of a 7-level converter that is comprised of five individual switching cells. Two example methods of determining duty cycle combinations are explored, one basic and one optimized, and the characteristics of each discussed. Converter performance as N approaches ∞ are provided.**

I. Introduction

Multi-level power converters serve to bridge the gap between high-voltage systems and lower voltage components. Applications of multilevel power conversion are wide, ranging from high-voltage DC transmission (HVDC) [1], [2] to medical devices [3] and to automotive technology [4]. HVDC transmission systems see notable improvement when controlled through multilevel topologies over traditional 2-level topologies [5]. Electric vehicles can also benefit from the implementation of multilevel topologies [6], [7].

Multilevel topologies do not come without their flaws, most markedly their higher component count and more complex control. A variety of multilevel converters exist, each with their respective tradeoffs.

Component quantities as a function of N levels for a variety of multilevel converters can be seen in Table I [8], [9]. Diode-clamped, capacitor-clamped, and the generalized D-shaped converters have exponentially increasing component counts as a function of number of levels [9], [10]. Modular Multilevel converters (MMC) have unbalanced voltages in steady state, making DC/DC implementations of these topologies challenging [11]. The full-bridge MMC improves over the half-bridge MMC with respect to flexibility in capacitor voltages and balancing but comes at the cost of increased switching devices and control complexity [12]. Likewise, the diode-clamped, capacitor clamped, and generalized D-shaped topologies also require extra attention to keep capacitor voltages balanced, more so as the number of levels increases [13], [14], [15], [16].

The proposed topology is an adaptation of the high conversion ratio converters found in [17], [18], where the intended output voltage of the converter is a fraction of the input voltage. Designs with similar topologies intended for high conversion ratios can be found in [19], [20], [21]. AC/DC operation has been achieved in [22]. The proposed topology is not intended for high conversion ratios but rather as a multilevel topology with an output voltage that can swing across the full input voltage. It maintains capacitor voltage balance while bidirectionally converting AC/DC or DC/DC through its independently operable unit switching cells and component quantities scale linearly with the number of levels. This topology is referred to as the Manhattan Topology throughout this paper.

TABLE I
Number of Components in N-Level Converter Topologies

Topology	Semiconductors	Inductors	Capacitors
Diode-Clamped [9]	N^2-N	1	$N-1$
Capacitor-Clamped [9]	$2(N-1)$	1	$(N-1)+\frac{N^2-3N+2}{2}$
Generalized D-shaped [10]	$N(N-1)$	1	$\frac{N^2+N}{2}-N$
Half-Bridge MMC [1]	$4(N-1)$	2 or $4(N-1)$	$2(N-1)$
Full-Bridge MMC [1]	$8(N-1)$	2 or $4(N-1)$	$2(N-1)$
Manhattan (proposed)	$2(N-2)$	$N-2$	$N-1$

II. Topology Description

The generalized topology for the Manhattan converter is shown in Fig. 1, where N and K represent the number of levels and number of stackable unit cells, respectively, and $N = K + 2$. Although this circuit topology is capable of bidirectionally converting DC/DC or DC/AC, for the sake of brevity this paper considers the converter in DC/DC step-down buck-mode operation and the terms are labeled as such. Output is taken exclusively at the center node which is defined as having the same number of series capacitors above it as below it. The output node was chosen as the middle node as it is equal to one-half the input voltage which provides symmetric output voltage swing across its full range.

The stackable unit cell that composes this multilevel topology can be seen in the left circuit of Fig. 2. Dashed grey lines denote connections to adjacent cells. Current flows through each unit cell in the same way it does in a typical inverting buck-boost converter. The right circuit of Fig. 2 shows an inverting buck-boost converter with the nodes and components

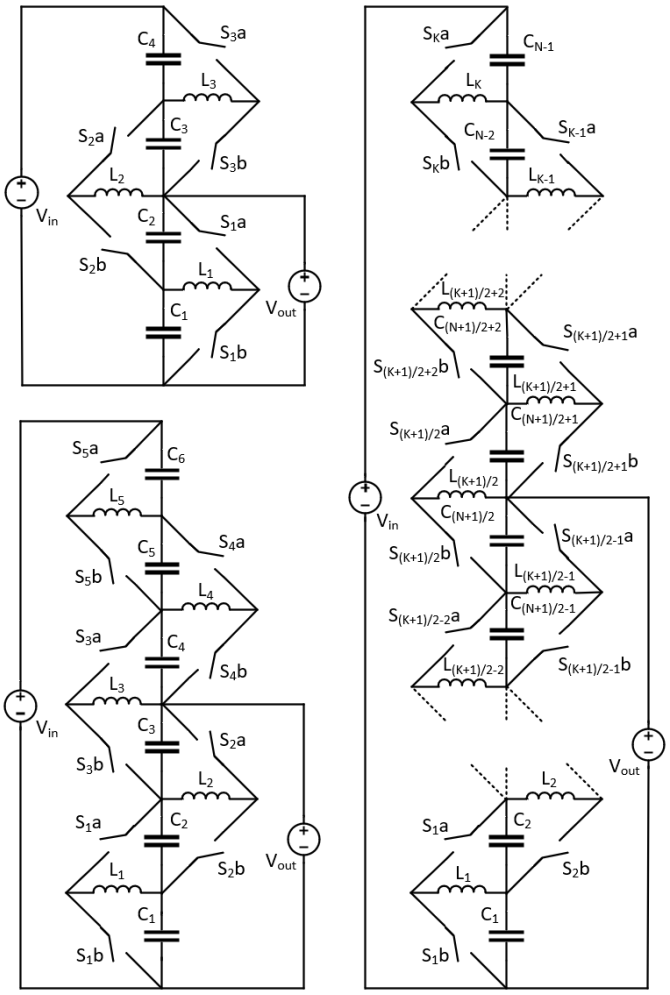

Fig. 1. Manhattan Topology. Upper left: 3 Cells, 5 Levels. Bottom left: 5 Cells, 7 Levels. Right: Generalized topology for K cells and N levels.

labeled as they align with the repeatable unit cell to its left. In this manner, each unit cell can be considered an individual inverting buck-boost converter, and the stacking of unit cells a quasi-cascade. The stacked cell nature of this

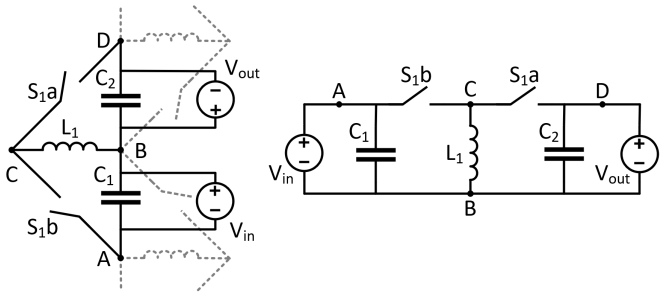

Fig. 2. Stackable unit cell as it relates to the inverting buck-boost converter (dashed lines show connections of adjacent cells).

topology eliminates the need for a bulk capacitance between the input to reference and/or the output to reference as the series combination of the cell capacitances serve to support both the input and output nodes as well as the voltages within each cell. The individual capacitor voltages can be controlled as a function of the duty cycles of each unit cell, allowing for the voltage across the entire stack to be balanced across each cell to any arbitrary ratio. This enables the control and conversion of voltages higher than the voltage rating of any individual semiconductor or passive component. As the output voltage is simply the sum of the capacitor voltages between the output node and reference, the ability to balance the capacitor voltages to any arbitrary ratio also allows for the output voltage to swing between full input voltage and reference.

The quasi-cascade nature of this topology induces circulating currents between adjacent cells. General current paths can be seen in Fig. 3. Following the path of the currents above and below L_i, it can be seen that the center most inductor L_i must support the inductor currents of the cells above and below it. The exact ratio of of currents between the inductors is a function of the duty cycles of each cell and the number of stacked cells. Methods of calculating cell voltages and currents as a function of duty cycles and input/output voltages are explored in the following section.

III. Derivation of Fundamental Equations

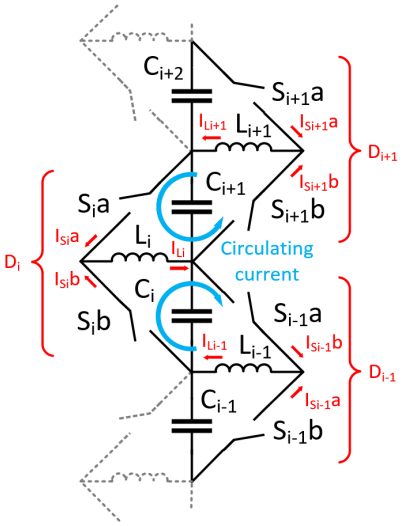

Fig. 3. Labeled Cell.

The first step in derivation is to define the governing equations within a single cell. Using the notation shown in Fig. 3, the equations for average switching current, inductor current, and capacitor voltages are as follows:

$$V_{Ci} = V_{C_{i+1}} \left(\frac{D_i}{1-D_i} \right) \tag{1a}$$

$$I_{L_i} = I_{s_i a} + I_{s_i b} \tag{1b}$$

$$I_{L_i} = I_{s_{i-1} a} + I_{s_{i+1} b} \tag{1c}$$

$$I_{s_i a} = I_{L_i}(1 - D_i) \tag{1d}$$

$$I_{s_i b} = I_{L_i} D_i, \tag{1e}$$

where (1a) - (1e) align with the equations for a typical inverting buck boost converter and hold true for each individual

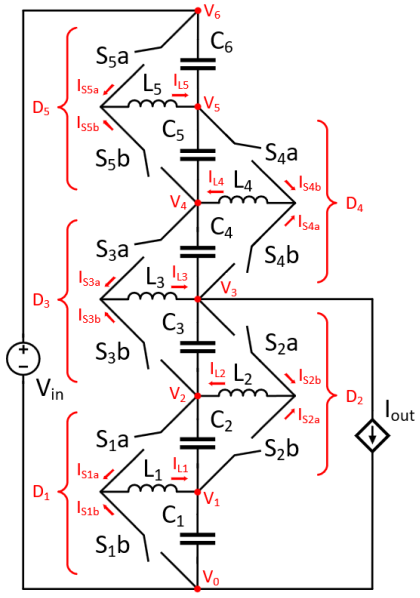

Fig. 4. Seven level converter with labeled nodes and currents.

unit cell within the multilevel converter. The 7-level converter of Fig. 4 is used during the derivation of the fundamental equations.

A. Derivation of Equations for Voltage

The output voltage, taken at the node labeled V_3 (fourth level), is the sum of all capacitors voltages between it and reference. Iteratively substituting in (1a) for each cell below the output and algebraically rearranging in terms of V_{C6} produces the following sequence of equations:

$$V_{out} = V_{C1} + V_{C2} + V_{C3} \tag{2}$$

$$V_{C1} + V_{C2} + V_{C3} = \left(\frac{D_1}{1-D_1}\right)\left(\frac{D_2}{1-D_2}\right)\left(\frac{D_3}{1-D_3}\right) \tag{3}$$

$$\begin{aligned} V_{out} = V_{C6}\Bigg(&\left(\frac{D_1}{1-D_1}\right)\left(\frac{D_2}{1-D_2}\right)\left(\frac{D_3}{1-D_3}\right)\left(\frac{D_4}{1-D_4}\right)\left(\frac{D_5}{1-D_5}\right) \\ &+ \left(\frac{D_2}{1-D_2}\right)\left(\frac{D_3}{1-D_3}\right)\left(\frac{D_4}{1-D_4}\right)\left(\frac{D_5}{1-D_5}\right) \\ &+ \left(\frac{D_3}{1-D_3}\right)\left(\frac{D_4}{1-D_4}\right)\left(\frac{D_5}{1-D_5}\right)\Bigg). \end{aligned} \tag{4}$$

Repeating this iterative process while moving from the bottom cell to the top cell produces results in:

$$\begin{aligned} V_{in} = V_{C6}\Bigg(&\left(\frac{D_1}{1-D_1}\right)\left(\frac{D_2}{1-D_2}\right)\left(\frac{D_3}{1-D_3}\right)\left(\frac{D_4}{1-D_4}\right)\left(\frac{D_5}{1-D_5}\right) \\ &+ \left(\frac{D_2}{1-D_2}\right)\left(\frac{D_3}{1-D_3}\right)\left(\frac{D_4}{1-D_4}\right)\left(\frac{D_5}{1-D_5}\right) \\ &+ \left(\frac{D_3}{1-D_3}\right)\left(\frac{D_4}{1-D_4}\right)\left(\frac{D_5}{1-D_5}\right) \\ &+ \left(\frac{D_4}{1-D_4}\right)\left(\frac{D_5}{1-D_5}\right) \\ &+ \left(\frac{D_5}{1-D_5}\right) \\ &+ 1\Bigg) \end{aligned} \tag{5}$$

where (4) and (5) provide equations for V_{in} and V_{out} as a function of V_{C6}. Combining these two equations, simplifying, and using series sum and series product notation yields (6) which gives V_{out}/V_{in} as a function of each cell's duty cycle:

$$\frac{V_{out}}{V_{in}} = \frac{\sum_{j=1}^{3}\left[\prod_{i=j}^{5}\left(\frac{D_j}{1-D_j}\right)\right]}{\sum_{j=1}^{5}\left[\prod_{i=j}^{5}\left(\frac{D_j}{1-D_j}\right)\right]+1}. \tag{6}$$

An identical process can be used to find the voltage at any node along the center capacitor stack for a converter of N levels. Level $n = 0$ is considered as reference voltage and level $n = N$ as the input voltage. For clarity, these nodes are labeled V_0 and V_6 in Fig. 4, respectively. Level n is the voltage being calculated. This adapted derivation is as follows:

$$\frac{V_n}{V_{in}} = \begin{cases} \dfrac{\sum_{j=1}^{n-1}\left[\prod_{i=j}^{N-2}\left(\frac{D_j}{1-D_j}\right)\right]}{\sum_{j=1}^{N-2}\left[\prod_{i=j}^{N-2}\left(\frac{D_j}{1-D_j}\right)\right]+1} & \text{for } 0 < n < N \\ 1 & \text{for } n = N \\ 0 & \text{for } n = 0. \end{cases} \tag{7}$$

It is important to note that (7) provides the voltage of the node in question relative to reference, and not the individual capacitor voltages. Individual capacitor voltages can be found by calculating the voltages of the capacitor's two adjacent nodes and taking the difference.

B. Derivation of Equations for Current

Deriving the equations for current begins at the middle node. The middle node is labeled V_3 of the example seven level converter in Fig. 4. (1c) serves to link two adjacent cells and is modified for taking the output at the middle node:

$$I_{L_3} = I_{s_4b} + I_{s_2a} + I_{out} \tag{8}$$

where I_{L_3} is the average current through the middle cell inductor. Iteratively substituting in (1c), (1d), and (1e) alongside algebraic manipulation produces:

$$I_{s_4b} = I_{L_3}\frac{D_3(1-D_4)}{1-D_4(1-D_5)} \tag{9}$$

$$I_{s_2a} = I_{L_3}\frac{D_2(1-D_3)}{1-D_1(1-D_2)} \tag{10}$$

which provides I_{s_4b} and I_{s_2a} as functions of exclusively D and I_{L_3}. Substituting (9) and (10) into (8) and algebraically rearranging results in:

$$\begin{aligned} I_{L_3} = I_{out}\Bigg(1 &- \frac{D_3(1-D_4)}{1-D_4(1-D_5)} \\ &- \frac{D_2(1-D_3)}{1-D_1(1-D_2)}\Bigg), \end{aligned} \tag{11}$$

which provides the average current through the middle inductor as a function of output current I_{out} and duty cycles D. This same process can be taken to find the average current through

the middle inductor for any odd-numbered level converter as a function of output current. This adaptation is as follows:

$$\frac{I_{out}}{I_{L_m}} = 1 - \frac{D_m(1-D_{m+1})}{1-\frac{D_{m+1}(1-D_{m+2})}{1-\frac{D_{m+2}(1-D_{m+3})}{\cdots}}} - \frac{D_{m-1}(1-D_m)}{1-\frac{D_{m-2}(1-D_m-1)}{1-\frac{D_{m-3}(1-D_{m-2})}{\cdots}}} \quad (12)$$

where m is used to denote the middle inductor (for the 7-level converter of Fig. 4, $m = 3$). Lastly, the relationship between a known inductor current I_{L_j} and any two adjacent inductor currents $I_{L_{j-1}}$ and $I_{L_{j+1}}$ can be calculated using the following equations:

$$\frac{I_{j+1}}{I_j} = \frac{D_j}{1-\frac{D_{j+1}(1-D_{j+2})}{1-\frac{D_{j+2}(1-D_{j+3})}{\cdots}}} \quad (13)$$

$$\frac{I_{j-1}}{I_j} = \frac{1-D_j}{1-\frac{D_{j-2}(1-D_{j-1})}{1-\frac{D_{j-3}(1-D_{j-2})}{\cdots}}} \quad (14)$$

resulting in (13), (14), and (7) allowing for all inductor current and node voltages of any odd-numbered level converter of this topology to be calculated. These equations have been validated through simulation, the results of which are discussed in the following section.

IV. Results

Unlike other multilevel topologies, the allowable switching states of the Manhattan topology do not depend on the entire converter as a whole, but rather each unit cell. Each unit cell can be treated as an individual switching converter, meaning that the only switching state limitation is that both switches within the same unit cell cannot be on simultaneously. Beyond that there are no other exclusions, duty cycles between different cells do not need to be synchronized or even operating at the same frequency. The results in the following sections are found using an open-loop constant duty cycle control for the purpose of topology validation.

A. Fundamental Operation

The circuit is validated using the parameters $V_{in} = 800V$, $I_{out} = 10A$, $F_{sw} = 50kHz$, $C = 10\mu F$, and $L = 450\mu H$ unless otherwise specified. All cells have the same component values and a constant duty cycle of 0.5.

There is an inherent tradeoff between location of output node and magnitude of circulating current, shown in Fig. 5. The two configurations where the circulating inductor current are minimized occur when the number of levels between the load to input or output voltage rail is minimized, resulting in either extremely high or extremely low conversion ratios. These areas of operation has been explored extensively [17]-[21].

Maximizing the number of levels between the load and both the positive and negative voltage rails allows for a full-voltage-swing converter. This places the load in the middle of the converter, skewing the tradeoff between circultating currents and output voltage swing towards maximizing the output voltage swing. Fig. 5 shows the maximum inductor current in the set of all inductor currents for a converter where all duty cycles are set to 0.5. The level where the output node is taken is varied and the maximum inductor current normalized, showing the general trend of circulating current as it relates to location of the output node.

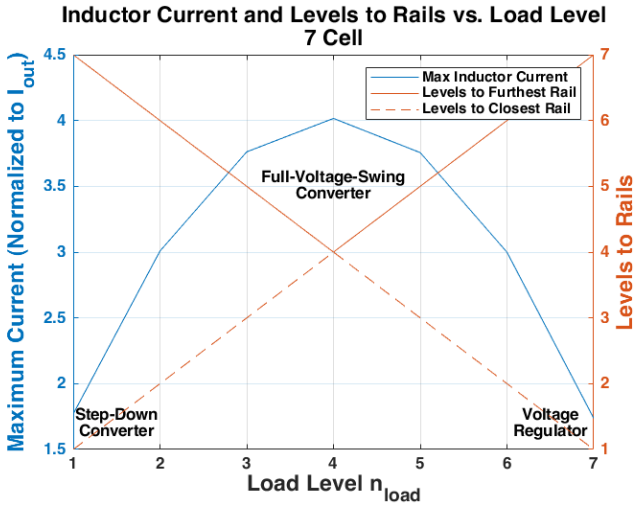

Fig. 5. Maximum inductor current as a function of the location of the output node.

B. Duty Cycle Combinations

Two example methods of determining duty cycle combinations are provided. It is important to note that other methods beyond the two shown may exist and it is not implied that the two are optimal for all applications. The seven level converter seen in Fig. 3 is used for this application. For both of the example duty cycle combinations the output voltage is swung from reference to input voltage with a constant output current equal to I_{out}.

1) Example Duty Cycle Combination 1 (Simplistic): The first example control method involves setting the duty cycles of all cells except the center cell (comprised of L_3, S_3a, S_3b, C_4, and C_5, controlled by D_3) to a static value of 0.5. The output voltage is controlled solely by the duty cycle D_3 of the center unit cell. The results of sweeping the duty cycle of the center unit cell from 0 to 1 while holding the the other cells constant at $D = .5$ can be seen in Fig. 6. This control method results in ideal splitting of cell voltages over the entire the duty cycle sweep. The capacitor voltages above the output node evenly split the voltage $V_{in} - V_{out}$ while the capacitor voltages below the output node evenly split the output voltage V_{out}. Furthermore, the relationship between D_3 and $\frac{V_{out}}{V_{in}}$ is linear. The average current through the center inductor L_3 is constant throughout the sweep at 3 times the output current,

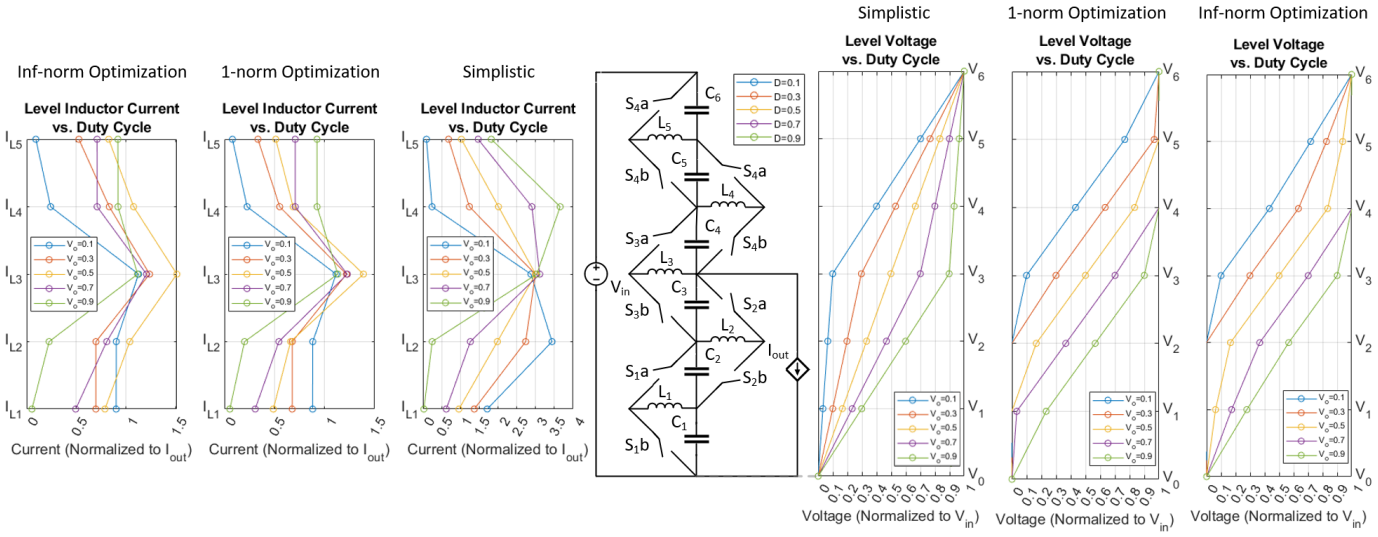

Fig. 6. Level current and voltages over V_{out} sweep. Outer: inf-norm optimization. Second outer: 1-norm optimization. Inner: simplistic.

which can be attributed to the circulating currents between adjacent cells.

2) Example Duty Cycle Combination 2 (Optimized): The second example control method involves using the derived fundamental equations alongside MATLAB's *fmincon* optimization function to provide the duty cycles for each cell. MATLAB's *fmincon* function is an optimizer that attempts to minimize the value of a configurable objective function for a given system with constraints. The system is the power converter, utilizing the previously derived fundamental equations. The equality constraint,

$$\sum_{j=1}^{(N-1)/2} V_{cj} = V_{out} \tag{15}$$

is configured to control the voltage of the middle node (output) to a predetermined desired voltage (which is iteratively swept from reference to V_{in}). The inequality constraint,

$$V_C \leq \frac{2V_{out}}{N-1} \tag{16}$$

is configured to ensure that no single capacitor voltage is greater than one-third of the input voltage. The value of one-third is chosen as at the extremes of the output voltage swing there are three capacitors in series that hold the full input voltage, and one-third represents ideal voltage splitting. Three objective functions are explored:

1) The 1-norm of all inductor currents, which represents a minimization of overall current rating.
2) The 2-norm squared of all inductor currents, which represents a minimization of overall power loss.
3) The inf-norm of all inductor currents, which represents a minimization of the maximum current in the set of all inductor currents.

The results of the optimization with the 1-norm and 2-norm squared are identical (only the 1-norm results are shown),

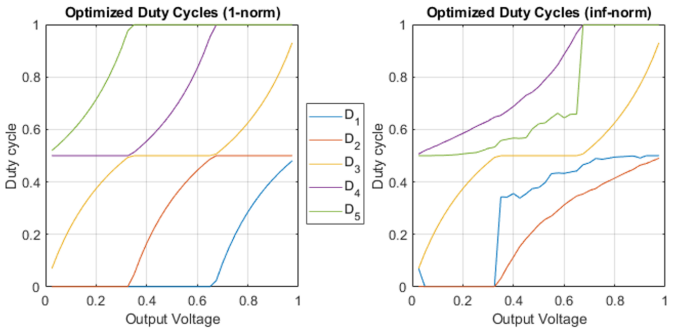

Fig. 7. Optimized duty cycles using 1-norm (left) and inf-norm (right) as a function of the output voltage normalized to V_{in}.

suggesting that the optimal duty cycles for minimizing the overall current rating and minimizing the I^2R power losses are the same. The results are similar for the inf-norm optimization. It is worth noting, however, that the 1-norm and 2-norm optimizations effectively turn cells off at the extremes of the output voltage swing while the inf-norm optimization keeps them on while allocating proportionally small voltage across them. The maximum current through any inductor throughout the output voltage sweep is less than 1.5x the output current for all optimization methods, a substantial reduction over the previous non-optimized method of determining duty cycle combinations.

C. Converter Scaling and Limitations

The steady-state limits of this multi-level converter can be shown by sweeping number of cells in the converter and analyzing resulting inductor currents. This is possible by choosing an arbitrary number of K cells, and solving for all inductor currents using equations (13) and (14). The control methods previously described can be used with generalized

forms of the equality (15) and inequality (16) capacitor voltage constraints.

The results from a $3 < K < 77$ cell sweep are shown in Fig. 8. The maximum and average inductor currents increase linearly with the number of levels of the converter, regardless of the control scheme chosen, which limits the number of levels as a function of inductor current rating. 1-Norm, 2-Norm, and Inf-norm max current traces overlap.

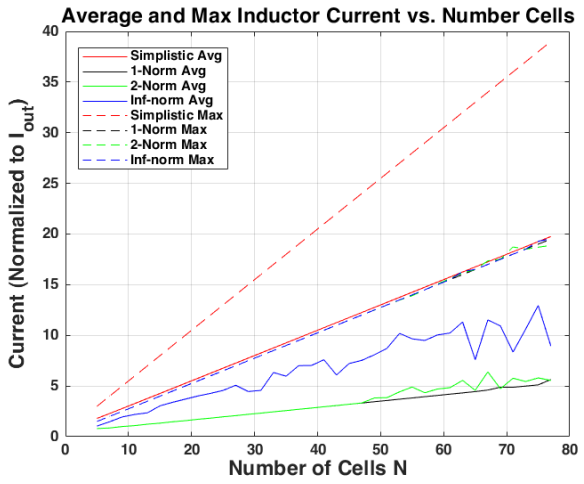

Fig. 8. Maximum and average inductor current vs K.

V. Conclusion

This topology has benefits over existing multilevel power converter topologies, with its simplicity at the forefront. Linear component quantity scaling along with individually controllable stackable cells that can be easily connected together lends this topology to a modular and readily expandable approach. The bidirectional and AC/DC or DC/DC capabilities of this topology can be used for a variety of applications, ranging from electric vehicles to HVDC transmission. Future work to further validate this topology includes implementing closed loop duty cycle control and investigating more methods of reducing the circulating current present at high numbers of levels.

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