Novel Upper Capacitor for Half-Bridge Switching Converter Topologies that reduces EMI and Capacitor Ripple Current

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***Abstract*—Electromagnetic interference (EMI) and power density are two highly studied fields as power converters become smaller and more numerous. Physical EMI filters can improve EMI performance at the cost of size. Passive components (inductors, capacitors) are often the limiting factor for improving power density. This digest presents a simple modification to the typical half-bridge buck converter that results in improved EMI performance and decreased required capacitance. The modification comes in the form of a single capacitance placed between the input and output nodes of the converter. This capacitor allows for the ripple currents at both nodes to be shared. As there is an element of correlation between these ripple currents, any differential mode currents can be canceled through this capacitance. This results in improved EMI performance and decreased total capacitor ripple current when compared with a typical half-bridge buck converter when the total capacitance (and therefore the required physical size of the capacitors) between the two converters is held constant. Furthermore, the reduction in total capacitor ripple current can allow for a decrease in capacitor size if capacitor ripple current drives capacitor sizing. Equations for capacitor current are derived and optimum capacitance ratios are found mathematically. Improvements over the typical half-bridge buck converter are demonstrated through both simulation and physical experiments. Experimental capacitor current measurements alongside input and output FFTs are provided.**

I. Introduction

Ripple limitations, in both voltage and current, drive many power converter design choices. It is not atypical to design towards predetermined levels of voltage ripple. For a bidirectional half-bridge buck topology, which is the topology that is considered in this paper and can be seen in Fig. 2, the two nodes where ripples are considered are the input (V_i) and the output (V_o).

The output voltage ripple is the typical design priority. However, voltage ripple at the input must also be considered, as unfiltered input currents of a switching converter can generate high frequency harmonic emissions that can couple into other circuits [1]. This is a widely studied phenomenon as numerous electromagnetic compatibility (EMC) standards exist to regulate these emissions in power line, information technology, aerospace, and commercial electronic applications [2].

Many solutions exist for mitigating EMI. Some involve additional active components [3]–[5] while others are rely on exclusively passive components [6], [7]. These are functional solutions, however, the EMI reduction they provide comes at the cost of increased component quantity and volume. EMI reduction schemes that involve control strategy [8], [9] and layout techniques [10] have also been proven to be effective. Topological solutions, which align more with what is presented in this digest, have also been proven [11], [12].

These solutions are exclusively for EMI reduction and do not mitigate the capacitor ripple current problems present in converters that leverage large inductor current ripples. These designs, such as those that involve variable frequency soft switching [13], have been shown to improve both efficiency and power density. However, they require filters that can also withstand these high ripple currents.

An easily overlooked specification of filter capacitors is their RMS current handling capabilities. This specification is largely a product of the capacitor's ESR and thermal characteristics [14]. This creates another limitation on the design choice of capacitance as the capacitance necessary to meet a desired ripple voltage may not be sufficient to handle the required capacitor ripple current. Therefore, the capacitor value needs to be set to the smallest value that satisfies both the desired ripple voltage and required ripple current specifications.

This effect is demonstrated in Fig. 1 where the switching frequency of a hypothetical buck converter is swept while the inductor ripple current is held constant. An example film capacitor with parameters $C = 12\mu F$ and $I_{RMS,max} = 13A$ is used, and the inductor current ripple is held constant at $60A_{pp}$. The desired V_o ripple is $5V_{pp}$.

As the switching frequency increases, the capacitance required to maintain the desired output voltage ripple decreases. However, the inductor ripple current is constant and thus the required current handling capabilities of the capacitor is also constant. At 95kHz the limiting factor in capacitor sizing switches from desired output voltage ripple to required current handling capabilities, and beyond this frequency the required capacitance is constant. The typical design approach of increasing the switching frequency to reduce the physical size of the output filter becomes inneffective beyond this frequency breakpoint.

The proposed topology modification reduces both the EMI and the total ripple current handling requirements of the converter without increasing the total capacitance or volume.

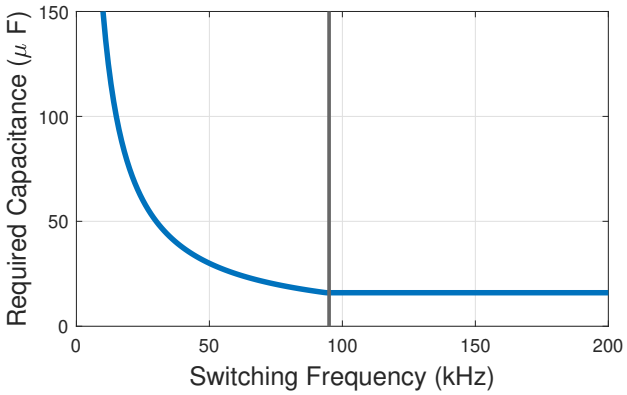


Fig. 1. Required capacitance as a function of switching frequency for hypothetical half-bridge converter.

The performance is proven through both simulation and experimental results.

II. Topology Description

The addition of C_A, highlighted in red of the right circuit in Fig. 2, introduces a capacative coupling between the input DC-link V_i and output V_o nodes that is not present in the typical half-bridge topology. The inclusion of C_A allows the ripple currents at the input and output nodes to be shared. Inductor current ripple will propagate to the input node and DC-link ripple current will propagate to the output node through C_A. The ripple current sharing between nodes allows for partial cancellation of any differential mode ripple between the input and output nodes.

Calculating the DC-link and output capacitor current ripples for a typical half-bridge converter is straightforward. However, the inclusion of upper capacitor C_A complicates this analysis. A model is derived where the load and ripple currents are decoupled and decomposed into individual current sources. This model is more conducive to being analyzed with traditional circuit analysis techniques, i.e. superposition.

Fig. 3 shows the process of decomposing the modified half-bridge topology, beginning with Fig. 3-(1) and ending with Fig. 3-(5). The first step in decomposition can be seen in Fig. 3-(2) where the transistors have been replaced with ideal switches and the inductor with an ideal current source. It is assumed that the capacitances of C_{DC}, C_A, and C_B

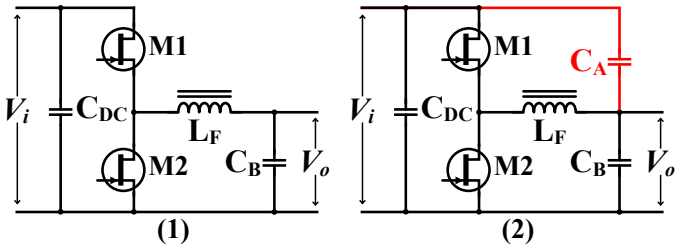


Fig. 2. Left: typical half-bridge topology. Right: modified half-bridge topology with the proposed upper capacitor C_A addition, highlighted in red.

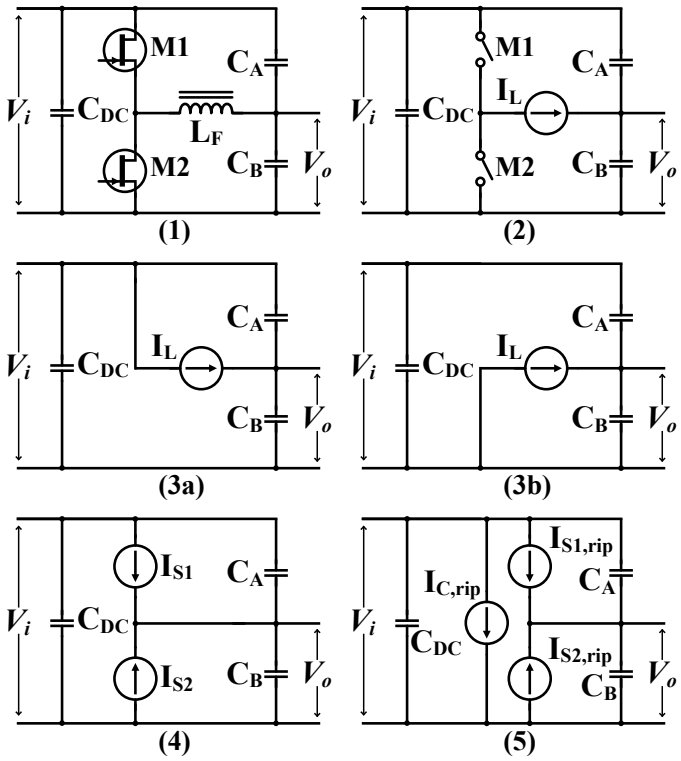


Fig. 3. Decomposition process of the proposed modified half-bridge switching converter operating in steady state into current sources and passive components.

are sufficient such that the voltage ripples present at nodes the input and output nodes can be considered negligible with respect to their DC values. This allows the current through the inductor to be approximated as a current source that is independent of capacitor values and only a function of the average values of V_i, V_o, the duty cycle D, the switching frequency f_{sw}, and the output current I_o according to:

$$I_{L,pp} = \frac{D\,(1-D)\,V_i}{f_{sw} L_f}, \tag{1}$$

where the total inductor current I_L is the sum of the inductor ripple current $I_{L,pp}$ and the output current I_o.

Trailing-edge modulation is also assumed. During $0 < t < DT$, S1 is closed and S2 is open. During $DT < t < T$, S1 is open and S2 is closed. This is typical operation for a half bridge converter and results in the division of the circuit seen in Fig. 3-(2) into both Fig. 3-(3a) and Fig. 3-(3b), where Fig. 3-(3a) corresponds to the the time period $0 < t < DT$ and Fig. 3-(3b) to $DT < t < T$.

I_L can be split along this same time division into current sources I_{S1} and I_{S2} and the circuits of Fig. 3-(3) can be recombined to form the circuit shown in Fig. 3-(4). The waveforms of currents I_L, I_{S1}, and I_{S2} can be seen in Fig. 4-(1), Fig. 4-(2), and Fig. 4-(3), respectively.

It is important to note that the waveforms I_L (1), I_{S1} (2), and I_{S2} (3) in Fig. 4 do not precisely describe the input/output ripple characteristics of the converter as they still contain a DC component. To remove the DC components of these

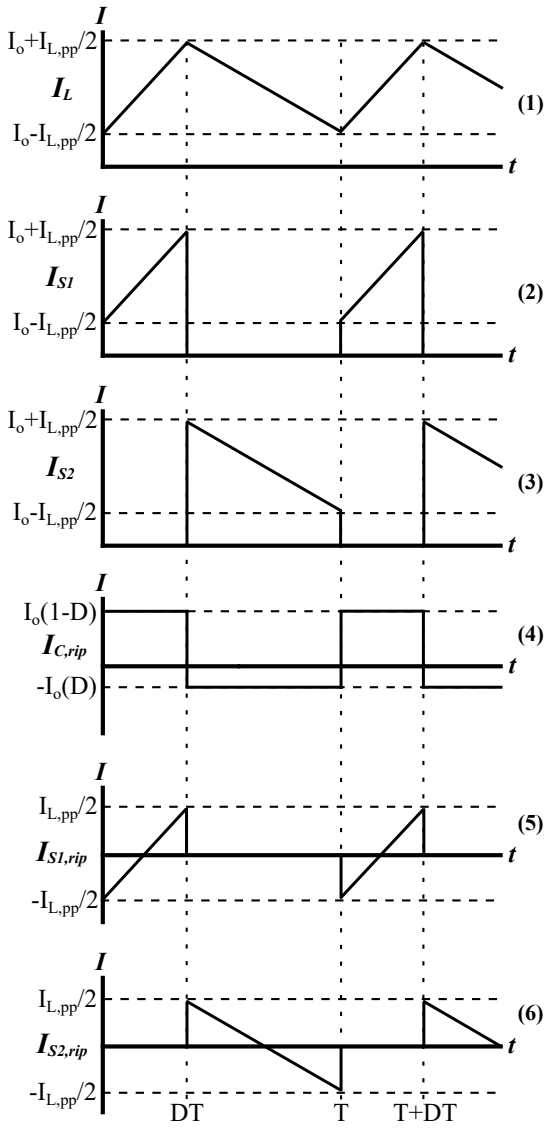


Fig. 4. Waveforms of I_L (1), I_{S1} (2), I_{S2} (3), $I_{C,rip}$ (4), $I_{S1,rip}$ (5), and $I_{S2,rip}$ (6).

waveforms it is first assumed that the connections across V_i and V_o are ideal constant current sources with current equal to the average current into their nodes. This assumption forces all current ripples to be absorbed in capacitances internal to the converter and not by any external components connected across V_i or V_o.

Removing the DC component present at the input node V_o is straightforward as I_o can simply be subtracted from I_{S1} and I_{S2}. Removing the DC current component present at node C requires an additional current source to be connected across V_i. The fully decomposed circuit with DC current components removed can be seen in Fig. 3-(5) and its corresponding current source waveforms in Figs. 4-(4), 4-(5), and 4-(6).

Decomposition of the modified half bridge converter allows for the circuit to be analyzed as three separate linear circuits with each circuit corresponding to its respective current source.

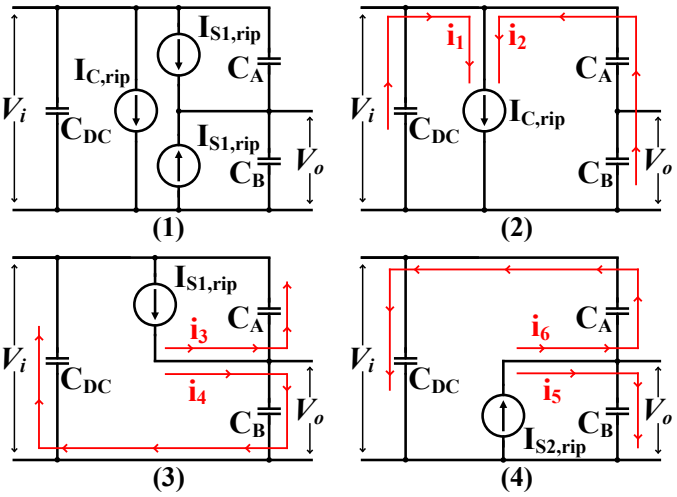


Fig. 5. Decomposition of the proposed modified half-bridge (1), Capacitor currents due to $I_{C,rip}$ (2), Capacitor currents due to I_{S1} (3), Capacitor currents due to I_{S2} (4).

As $I_{C,rip}$, $I_{S1,rip}$, and $I_{S2,rip}$ are all representative of ripple currents with average values of zero, any capacative charging phenomena can be neglected. The currents from each current source get split amongst all three capacitors according to the circuits in Fig. 5.

III. Capacitor Sizing

The process for calculating capacitor currents is straightforward. Variables a, b, and c can be assigned to describe how the currents from each current source split according to:

$$a = \frac{i_1}{i_{C,rip}} = \frac{C_{DC}}{C_{DC} + (\frac{1}{C_A} + \frac{1}{C_B})^{-1}}, \tag{2}$$

$$b = \frac{i_3}{i_{S1,rip}} = \frac{C_A}{C_A + (\frac{1}{C_B} + \frac{1}{C_{DC}})^{-1}}, \tag{3}$$

$$c = \frac{i_5}{i_{S2,rip}} = \frac{C_B}{C_B + (\frac{1}{C_A} + \frac{1}{C_{DC}})^{-1}}. \tag{4}$$

The currents i_1 to i_6 are then

$$i_1 = I_{C,rip}(a), \tag{11}$$

$$i_2 = I_{C,rip}(1-a), \tag{12}$$

$$i_3 = I_{S1,rip}(b), \tag{13}$$

$$i_4 = I_{S1,rip}(1-b), \tag{14}$$

$$i_5 = I_{S2,rip}(c), \tag{15}$$

$$i_6 = I_{S2,rip}(1-c), \tag{16}$$

and the individual capacitor currents are

$$I_{C_A} = i_2 + i_3 + i_6, \tag{17}$$

$$I_{C_B} = i_2 + i_4 + i_5, \tag{18}$$

$$I_{C_{DC}} = i_1 + i_4 + i_6. \tag{19}$$

The current through each capacitor is determined by the ratio of capacitance values between all three capacitors. Eqns. (17), (18) and (19) can be used in conjunction with geometric

$$I_{C_A,RMS}^2 = \frac{1}{T}\left[\int_0^{DT}(I_o(1-D)(1-a)+(\tfrac{-I_{L,pp}}{2}+t\tfrac{I_{L,pp}}{DT})(b))^2\mathrm{d}t+\int_0^{T-DT}(-I_oD(1-a)+(\tfrac{I_{L,pp}}{2}-t\tfrac{I_{L,pp}}{T-DT})(1-c))^2\mathrm{d}t\right] \quad (5)$$

$$I_{C_B,RMS}^2 = \frac{1}{T}\left[\int_0^{DT}(I_o(1-D)(1-a)-(\tfrac{-I_{L,pp}}{2}+t\tfrac{I_{L,pp}}{DT})(1-b))^2\mathrm{d}t+\int_0^{T-DT}(-I_oD(1-a)-(\tfrac{I_{L,pp}}{2}-t\tfrac{I_{L,pp}}{T-DT})(c))^2\mathrm{d}t\right] \quad (6)$$

$$I_{C_{DC},RMS}^2 = \frac{1}{T}\left[\int_0^{DT}(I_o(1-D)a+(\tfrac{-I_{L,pp}}{2}+t\tfrac{I_{L,pp}}{DT})(1-b))^2\mathrm{d}t+\int_0^{T-DT}(-I_oDa-(\tfrac{I_{L,pp}}{2}-t\tfrac{I_{L,pp}}{T-DT})(1-c))^2\mathrm{d}t\right] \quad (7)$$

$$I_{C_A,RMS}^2 = \frac{D}{12}(3a^2I_o^2-6aI_o^2+I_{L,pp}b^2+3I_o^2)+\frac{1-D}{12}(3a^2I_o^2-6aI_o^2+3I_o^2+c^2I_{L,pp}^2-2cI_{L,pp}+I_{L,pp}^2) \quad (8)$$

$$I_{C_B,RMS}^2 = \frac{D}{12}(3a^2I_o^2-6aI_o^2+I_{L,pp}b^2-2bI_{L,pp}^2+3I_o^2+I_{L,pp}^2)+\frac{1-D}{12}(3a^2I_o^2-6aI_o^2+3I_o^2+c^2I_{L,pp}^2) \quad (9)$$

$$I_{C_{DC},RMS}^2 = \frac{D}{12}(3a^2I_o^2+I_{L,pp}^2b^2-2bI_{L,pp}^2+I_{L,pp}^2)+\frac{1-D}{12}(3a^2I_o^2+c^2I_{L,pp}^2-2c^2I_{L,pp}^2+I_{L,pp}^2) \quad (10)$$

interpretations of $I_{C,rip}$, $I_{S1,rip}$, and $I_{S2,rip}$ to calculate the RMS values each capacitor's ripple current. The RMS^2 values for each capacitor can be found in (5) to (10).

These equations can be used to optimize the ratio of capacitor values to achieve a minimum total ripple current. The following cost function is considered:

$$F = I_{C_A,RMS}^2 + I_{C_B,RMS}^2 + I_{C_{DC},RMS}^2, \quad (20)$$

where F can be minimized by setting the following partial derivatives to zero:

$$\frac{\partial F}{\partial a} = I_o^2\left((1-D)(a-1)+\tfrac{1}{2}+D(a-1)\right), \quad (21)$$

$$\frac{\partial F}{\partial b} = I_{L,pp}^2(\tfrac{D}{6})(3b-2), \quad (22)$$

$$\frac{\partial F}{\partial c} = I_{L,pp}^2(\tfrac{1-D}{6})(3c-2), \quad (23)$$

$$\frac{\partial F}{\partial a} = 0; \quad \frac{\partial F}{\partial b} = 0; \quad \frac{\partial F}{\partial c} = 0. \quad (24)$$

The solution to (21) to (24) is a value of $a = b = c = \frac{2}{3}$. Substitution of these values into (2) to (4) yield a capacitance relationship of $C_{DC} = C_A = C_B$, suggesting that the optimal capacitance ratio for minimizing the total capacitor RMS ripple current is 1:1:1.

IV. Results

The proposed upper capacitor C_A modification to the typical half-bridge topology has been validated through both physical experiments and hi-fidelity simulation. The parameters used in both the experimental and simulated setups can be seen in Table I. For each experiment and simulation the duty cycle D is swept from 0.1 to 0.9 to demonstrate the effectiveness of the upper capacitor C_A over the full duty cycle range. Results using these parameters over the D sweep can be seen in Figs. 6 to 10. The simulated results match the experimental results.

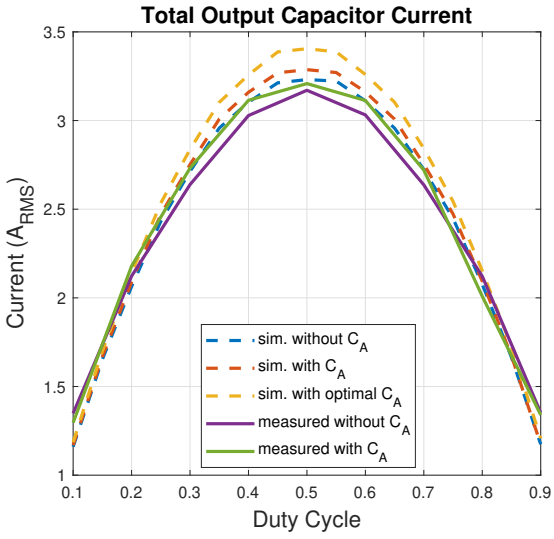


Fig. 6. Sum of current through capacitors connected to V_o.

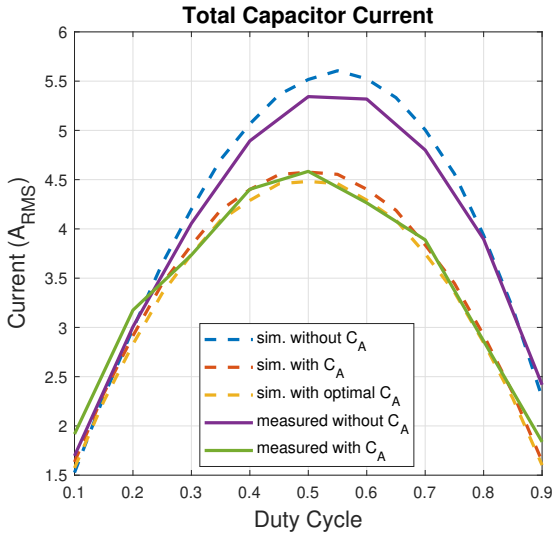


Fig. 7. Sum of all capacitor currents.

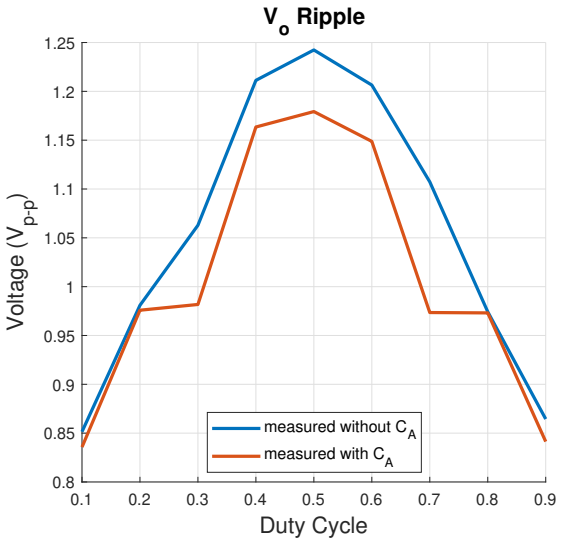


Fig. 8. Output voltage ripple.

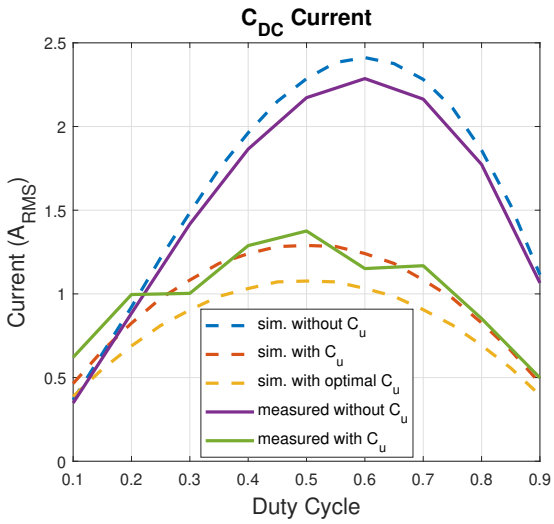


Fig. 9. Ripple current through C_{DC}.

The FFTs are experimentally measured at each point in the duty cycle sweep and then averaged together to produce Fig. 10. On both V_i and V_o nodes the switching frequency harmonic has been reduced and for V_o this reduction is more than 50%. There is also a reduction at the higher frequencies in the FFTs of for both V_i and V_o with the strongest reduction occurring at 300kHz on node V_o. These reductions in harmonics can be attributed to the current sharing that occurs across C_A that effectively spreads out the spectrum.

The RMS values of the sum of ripple currents in all capacitors is also reduced and can be seen in Fig. 7. The total output capacitor current, which is the current through the capacitors connected to V_o, is largely unchanged with the addition of C_A. However, the DC bus capacitor current sees a reduction over nearly the entirity of the D sweep, resulting in a peak reduction in total capacitor current of 20% occurring at $D = 0.6$. Furthermore, the improvement in capacitor currents through the optimized capacitance ratio is insignificant, suggesting that the value of the upper capacitor is less relevant than its presence.

The peak-to-peak value of the output voltage ripple is largely unchanged but reduced slightly with the addition of C_A, which can be seen in the experimental results of Fig. 8. This has the implication that the inclusion of C_A reduces the current ripple without incurring additional voltage ripple at the output node.

The value of C_A can be used to tradeoff reduction in total output capacitor current and C_{DC} capacitor current. This can be seen in Figs. 7 and 9 where the optimal C_A value effectively minimizes the sum of all capacitor ripple currents but the output capacitor current is increased while the DC bus capacitor current is decreased. This provides the circuit designer with another option for balancing the DC bus capacitance current ripple and the output capacitance current ripple.

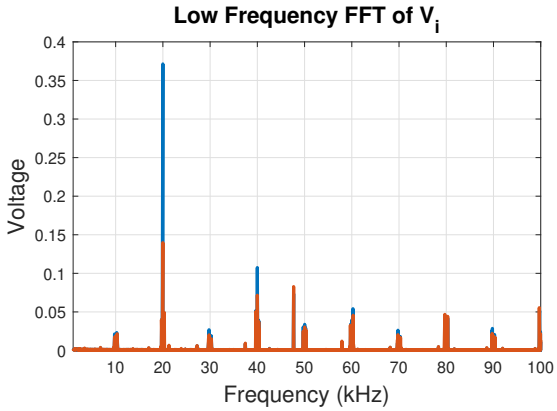
V. Conclusion

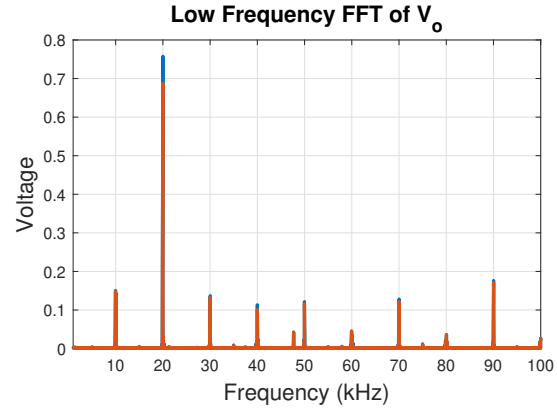
This addition of C_A to the typical half-bridge buck converter topology has marked benefits. The overall capacitor ripple current is reduced, which can potentially offer a reduction in required capacitance and volume. Both high frequency and low frequency harmonics are reduced, with an over 50 % reduction at the switching frequency for V_o. If any hypothetical design requires two parallel capacitors at the output, then it would offer increased performance to connect one as the upper capacitor (C_A) instead of both as lower capacitors C_B.

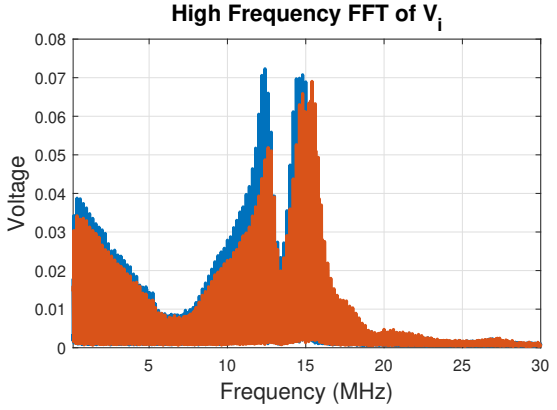
Further work regarding this topology includes the application of closed-loop control, examining the effect of C_A on multiple interleaved converters, and exploring the possibilities of connecting a similar capacitor between the input and output of different converter topologies.

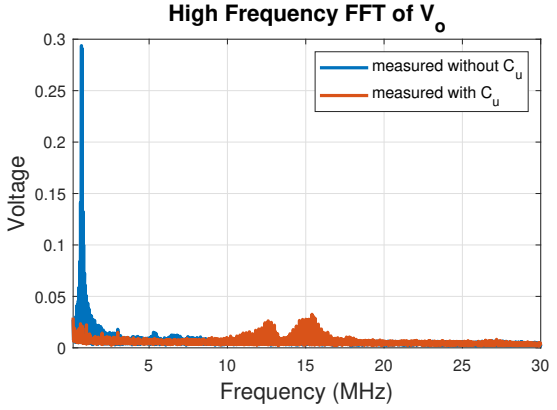
TABLE I
Simulated and Experimental Circuit Parameters

Setup	V_i	f_{sw}	L	C_{DC}	C_A	C_B	Capacitance Sum
Experimental without C_A	400V	20kHz	$450\mu H$	$24\mu F$	$0\mu F$	$24\mu F$	$48\mu F$
Experimental with C_A	400V	20kHz	$450\mu H$	$24\mu F$	$12\mu F$	$12\mu F$	$48\mu F$
Simulated without C_A	400V	20kHz	$450\mu H$	$24\mu F$	$0\mu F$	$24\mu F$	$48\mu F$
Simulated with C_A	400V	20kHz	$450\mu H$	$24\mu F$	$12\mu F$	$24\mu F$	$48\mu F$
Optimized Simulated with C_A	400V	20kHz	$450\mu H$	$12\mu F$	$12\mu F$	$24\mu F$	$36\mu F$









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