

Design of a 22kW Transformerless EV Charger with V2G Capabilities and Peak 99.5% Efficiency

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Abstract—This paper outlines the design process of a high-efficiency (99.5% peak) transformerless DC EV fast charger in conjunction with relevant UL standards on conducted harmonics and leakage current. The topology is a non-isolated transformerless design which allows for the elimination of the additional transformer volume and losses that are present in galvanically isolated topologies. Methods for calculating optimal switching frequency and inductance to minimize loss as a function of chosen switching device and power level are provided. Filter sizing and component values are chosen in conjunction with the previously determined optimal switching frequency and inductance. Heatsink design rationale are then derived. Experimental efficiency, switching waveforms, and output voltage and current quality results are provided. Industrial topology feasibility is shown through experimental adherence to relevant UL, IEC, IET, and IEEE standards.

Index Terms—Bidirectional EV charger, DC/DC converter, electric vehicle supply equipment (EVSE), inverter, silicon carbide (SiC), transformerless.

I. INTRODUCTION

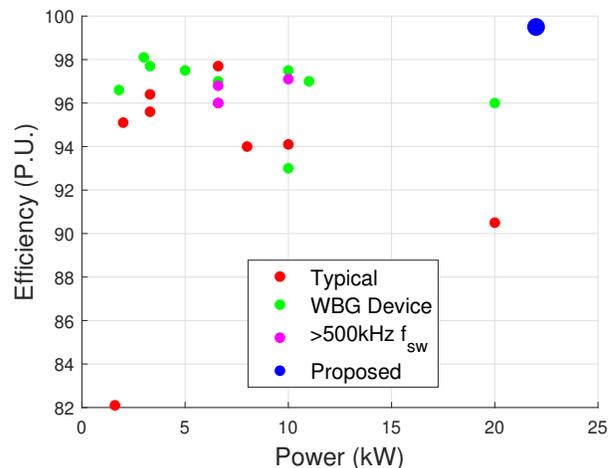
RECENT years have brought significant advancements in both the technology and popularity of Electric Vehicles (EVs) [1], [2]. EV exclusive automakers have been proven competitive and almost all previously combustion engine exclusive automakers now have some form of EV in their lineup. Many automakers have stopped the development of new internal combustion engine designs, further affirming the eventually inevitability of an EV centric future. EVs, however, still lack both the refueling infrastructure and refueling times associated with internal combustion vehicles. Methods of improving charging times on the battery chemistry side are a current area of research [3]–[5], however, it is also necessary to ensure that the associated power electronics can support the sufficient charging infrastructure and quick recharging times required for mass adoption of EVs.

Society's move towards EVs is also occurring at the same time as its move towards renewable energy sources. This presents a problem, as many renewable energy sources, such

as wind and solar, are intermittent. Their power output is not constant and depends on uncontrollable factors such as the weather [6]. There are times when renewable energy production is in excess and as a result gets curtailed, and times when renewable energy production is insufficient and requires fossil fuel plants to compensate. Some manner of grid supporting energy storage, both on large and small scales, can mitigate this intermittent renewable energy production problem by charging when excess power is being generated and discharging when increased power is demanded.

EVs have the unique ability to be used as energy storage devices as their large internal batteries can be leveraged as local grid supporting energy storage. This is a benefit for both the EV owner as well as the grid it connects to. Owners can save money by charging their EV when electricity prices are at their lowest and then using that power when electricity prices are at their highest [7]–[9]. The grid can use the charger and EV as sources or sinks of reactive and real power during spikes in demand [10]–[12]. [13] provides methods for this integration, [14] discusses the effect mobile storage has on the grid, and [15] gives methods for varying load compensation. Utilizing an EV in this manner, however, requires both the EV as well as the charger to be capable of bidirectional power flow.

Care must be taken to ensure that the energy cost of using



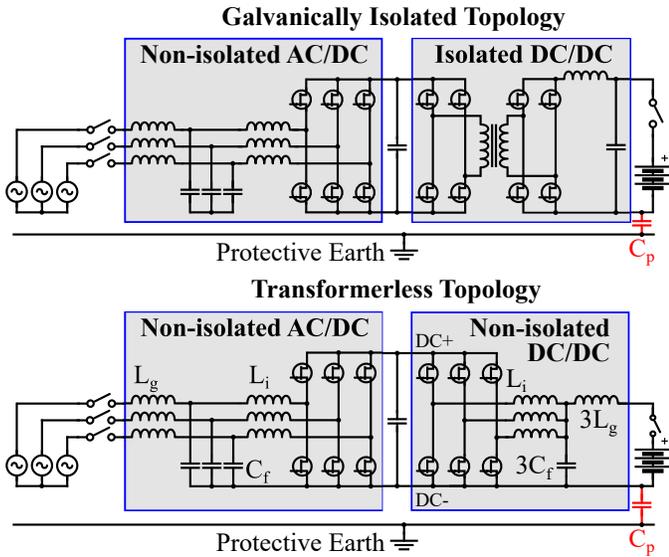


Fig. 2. Galvanically isolated topology (top) vs equivalent transformerless topology (bottom).

an EV as local power storage is minimal. The efficiency of the power converter that interfaces the vehicle and the grid is of increased importance in these applications as energy passes through it twice. A symmetric converter with a one-way efficiency of η will have a two way efficiency of η^2 , denoting the increased emphasis on efficiency. Therefore, any EV charger that can also provide grid services must maintain high efficiency in both vehicle to grid (V2G) and grid to vehicle (G2V) modes. Bidirectional chargers are already present both in academia as well as industry, and the push towards higher efficiencies is ever-present.

State of the art bidirectional academic chargers are exclusively galvanically isolated and have peak efficiencies up to 99% which can be seen in Fig. 1. The charger proposed in this paper is also bidirectional, but reaches peak efficiencies up to 99.5%, improving upon the present state-of-the-art. This is done through the use of a transformerless topology, uniquely applied to this charger and described in the following sections, which eliminates the losses and additional weight associated with galvanic isolation. This type of transformerless topology has been shown to be successful in photovoltaic system applications in [39]–[42] as well as other automotive applications [43], [44], but its application to EV charging is unique.

This paper details the novel design process used to maximize the efficiency of chargers using this transformerless topology. One charger is designed and built with all trade-offs leaning towards efficiency. Another charger is built, using the same design process, but with a compromise between efficiency and volume. Equations for calculating the average losses in the switching devices and inductors are derived. Optimization for efficiency is then carried out using those derived equations. Heatsink calculations are also provided. Experimental switching waveforms and efficiencies are provided. Grid quality and leakage current results are shown to prove this transformerless topology can be standards compliant.

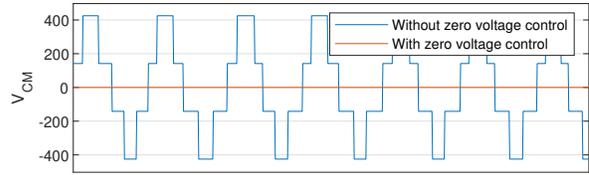


Fig. 3. Intended effect of zero voltage control on common mode voltage.

II. TOPOLOGY DESCRIPTION

The transformerless topology of this charger can be seen in Fig. 2, included is a galvanically isolated equivalent topology for reference. Removing the transformer has the potential to remove the losses, volume, weight, and size associated with it as well as decrease the minimum number of required switching devices on the DC/DC side. For reference, the high frequency isolation transformer used in [36], a 10kW 1MHz bidirectional converter, has a rough volume and price of .046L and \$20 which can be removed through the use of this topology. There are, however, additional control complexities associated with removing the transformer that are out of the scope of this paper but can be found in [45], [46]. [47] contains the control design, including the requirements for internal power flow balancing, for the hardware developed in this paper. Furthermore, the transformer also provides voltage step-down or step-up abilities, but these attributes are not necessary for this application as the DC bus is set to a higher voltage than both the AC and DC sides of the charger.

An important difference between the two topologies, aside from the lack of galvanic isolation, is the connection of the star point of the grid-side filter capacitors. The transformerless topology connects this star point to the negative DC bus (DC-) while the galvanically isolated topology allows this node to float. As described in [45]–[47], these grid capacitor voltages are measured and controlled to achieve a constant common-mode voltage through zero voltage control. This results in constant voltage between DC- and protective earth as the neutral point of the grid can be assumed constant with respect to protective earth, illustrated in Fig. 3. Controlling the voltage between DC- and protective earth allows for the current through the parasitic capacitance C_p to be driven to nearly zero, resulting in the elimination of leakage current without the use of galvanic isolation.

III. DESIGN PROCESS

A. Target Design Requirements

The hardware design requirements can be found in Table I. In addition to these design requirements, this charger is intended to be compliant with the UL 2231-2 and IEEE 1547 standards. The portions of these standards that are most relevant to this paper relate to the limits on leakage current and conducted current harmonics injected into the grid. UL2231-2 limits the leakage current by setting the limit on voltage across the parasitics between DC- and protective earth to $10V_{RMS}$ for frequencies above 20Hz and less than 1MHz. IEEE 1547 places limits on the current harmonics which can be seen in

TABLE I
 DC FAST CHARGER REQUIREMENTS

Parameter	Value
Grid Voltage	480V _{RMS,L-L}
Grid Current	32A _{RMS}
DC Bus Voltage	900V _{DC}
Battery Voltage	150-650V _{DC}
Battery Current	0-80A _{DC}
Real Power	22kW
Apparent Power	25kVA

Tables II and III. IEC and IET standards in [48]–[50] dictate that the maximum leakage current for human safety is 30mA.

The feasibility of chargers of this transformerless topology in non-academic applications is demonstrated by proving compliance with leakage current and grid harmonic standards.

B. Loss Estimation

There are two main sources of loss in chargers of this topology, FET losses and inductor losses, that will dominate its efficiency. FET losses can be split into two components, switching loss (the energy lost during each switching event) and conduction loss (associated with the nominal on resistance of the FET). Similarly, inductor losses can be split into a resistive loss within the winding and a hysteresis loss within the core due to the switching produced varying magnetic field. It is necessary to consider all four sources of loss simultaneously during the design process as it is possible to trade off loss in one area to another.

1) *FET Losses*: Rigorous quantification of FET losses must consider the instantaneous operating point of the converter. The DC/DC side of the charger can be considered to operate in steady state, however, the AC/DC side output is a sine wave, and as such output voltage V_{out} , output current I_{out} , and duty cycle D are dynamic and can be written as

$$V_{out}(\theta) = \frac{V_{DC}}{2} + \sqrt{2}V_{out,RMS} \sin(\theta) \quad (1)$$

$$I_{out}(\theta) = \sqrt{2}I_{out,RMS} \sin(\theta - \phi) \quad (2)$$

$$D(\theta) = \frac{V_{out}(\theta)}{V_{DC}}. \quad (3)$$

where θ is the instantaneous phase of the output sine wave voltage. ϕ is the phase difference between the output current and the output voltage and can be considered a static value.

 TABLE II
 ODD ORDER HARMONIC CURRENT DISTORTION LIMITS.

Odd Harmonics	1-9	11-15	17-21	23-33	35-49	THD
% Distortion	4.0	2.0	1.5	0.6	0.3	5.0

 TABLE III
 EVEN ORDER HARMONIC CURRENT DISTORTION LIMITS.

Even Harmonics	2	4	6	8-50
% Distortion	1.0	2.0	3.0	Associated range in Odd Harmonics

The peak to peak inductor ripple current $I_{L,p-p}$ can then be calculated with

$$I_{L,p-p}(\theta) = \frac{D(\theta)(1-D(\theta))V_{DC}}{f_{sw}(\theta)L_{sw}}. \quad (4)$$

The value of $I_{L,p-p}(\theta)$ is used when quantifying both the conduction loss and the switching loss. The conduction losses can be calculated using

$$P_{cond}(\theta) = R_{on} \left(I_{out}(\theta)^2 + \left(\frac{1}{2\sqrt{3}} I_{L,p-p}(\theta) \right)^2 \right) \quad (5)$$

where R_{on} is the datasheet specified nominal on resistance of the FET and $\frac{1}{2\sqrt{3}} I_{L,p-p}^2$ is the RMS value of the inductor current ripple component.

The process for calculating the switching losses used in this paper relies heavily upon a quantification of switching energy as a function of drain current I_d , gate resistance R_g , and FET drain-source voltage V_{ds} . The datasheet of the SiCFETs used in this converter provides these values which allows for the mapping of switching energies $E_{on}(I_d, R_g, V_{ds})$ and $E_{off}(I_d, R_g, V_{ds})$ to be formulated. R_g and V_{ds} can be considered static values as they will not change for a given operating point and are not included in the following equations for the sake of clarity.

As previously mentioned, the output current and voltage of a single phase can be considered dynamic and therefore the distinction between hard and soft switching over one cycle of the grid must be considered. Analytically, this distinction can be made with

$$E_{sw}(\theta) =$$

$$\begin{cases} E_{off}(I_a(\theta)) + E_{off}(I_b(\theta)) & I_a(\theta) > 0, I_b(\theta) < 0 \\ E_{on}(I_a(\theta)) + E_{off}(I_b(\theta)) & I_a(\theta), I_b(\theta) < 0 \\ E_{off}(I_a(\theta)) + E_{on}(I_b(\theta)) & I_a(\theta), I_b(\theta) > 0 \end{cases} \quad (6a)$$

$$I_a(\theta) = I_{DC} - \frac{I_{L,p-p}(\theta)}{2} \quad (6b)$$

$$I_b(\theta) = I_{DC} + \frac{I_{L,p-p}(\theta)}{2} \quad (6c)$$

where I_a and I_b are the peak and valley inductor current values, respectively. Visually, the hard and soft switching distinction can be seen in Fig. 4. This distinction is important to make as turn-on energies can be significantly greater than the turn-off energies.

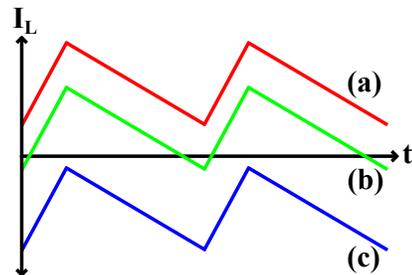


Fig. 4. Three different I_L cases used in calculating FET switching loss per cycle. a) turn-on loss at peak, turn-off loss at valley, b) turn-off loss at peak, turn-off loss at valley c) turn-on loss at peak, turn-off loss at valley.

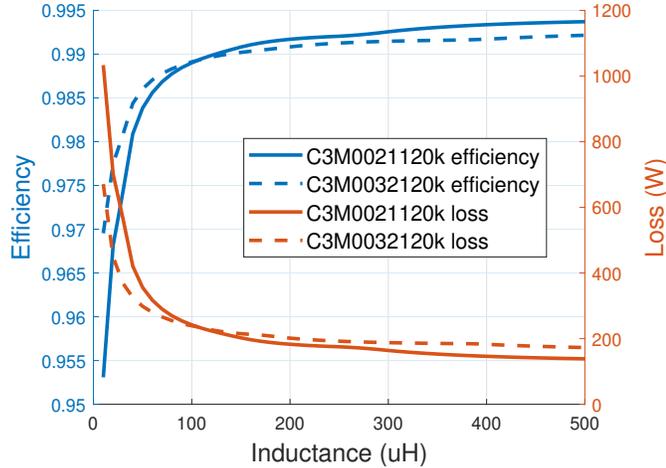


Fig. 5. Pareto front of inductance and FET loss/efficiency.

The switching loss P_{sw} can then be found with

$$P_{sw}(\theta) = f_{sw}E_{sw}(\theta). \quad (7)$$

Finally, the total FET loss P_{FET} over one cycle of the grid can be found by averaging the sum of both FET loss mechanisms from $0 < \theta < 2\pi$

$$P_{FET} = \frac{1}{2\pi} \int_0^{2\pi} (P_{cond}(\theta) + P_{sw}(\theta))d\theta. \quad (8)$$

2) *Inductor Losses*: Rigorous quantification of inductor losses can be a complex exercise. Inductor losses are calculated by splitting the total loss into two components, core loss and copper (winding) loss. Copper loss can be calculated with

$$P_{winding}(\theta) = R_{DC}I_{out}(\theta)^2 + R_{PWM}(\theta) \left(\frac{1}{2\sqrt{3}}I_{L,p-p}(\theta) \right)^2 \quad (9)$$

where R_{DC} is the DC winding resistance and $R_{PWM}(\theta)$ is the frequency dependant winding resistance of the inductor. As the fundamental frequency within the inductor is the switching frequency, and the switching frequency will change over one cycle of the grid, $R_{PWM}(\theta)$ is dynamic. The frequency dependant component of the winding resistance is an intrinsic value of the chosen winding wire gauge and type.

The core loss of the inductor can be calculated with

$$\begin{aligned} P_{core}(\theta) &= kf_{sw}(\theta)^a B_{pk}(\theta)^b \\ &= kf_{sw}(\theta)^a \left(\frac{4\pi NI_{pk}(\theta)10^{-2}}{l_g + (l_m/\mu_r)} \right)^b \end{aligned} \quad (10)$$

where k, a, b are coefficients of the core, typically supplied by its manufacturer. $B_{pk}(\theta)$ and $I_{pk}(\theta)$ are the peak flux and current densities, respectively, and are dynamic. N, l_g, l_m , and μ_r are the turn number, air-gap, and length of the magnetic path and permeability, respectively, and are static values of the inductor.

In a similar manner to calculating the FET loss, the average inductor losses are found by taking the average of the losses over one cycle of the grid according to

$$P_{Inductor} = \frac{1}{2\pi} \int_0^{2\pi} (P_{core}(\theta) + P_{winding}(\theta))d\theta. \quad (11)$$

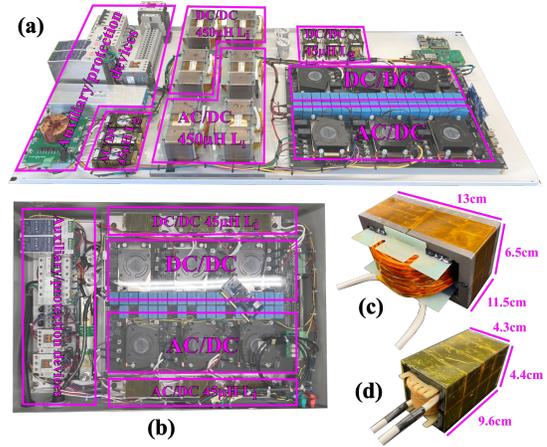


Fig. 6. Experimental charger prototypes. (a): Charger version 1. (b): Charger version 2. (c) $450\mu H$ inductors used in version 1. (d) $50\mu H$ inductors used in version 2.

Lastly, the total loss is simply

$$P_{total} = P_{FET} + P_{Inductor} \quad (12)$$

C. Switching Frequency and Inductance Optimization

The optimization is done by simultaneously sweeping the L and f_{sw} operating parameters. At each point in this two-dimensional sweep the loss is calculated and recorded. These sweeps are performed for two SiCFET variants to determine the best for this application:

- CREE C3M0021120k SiC FET
- CREE C3M0032120k SiC FET

These sweeps are performed with the charger operating at its rated power with the parameters found in Table I. The common-mode voltage of the grid is placed at one-half of the DC bus voltage. The battery parameters are held constant at 300V and 73.3A (22kW). The results of these sweeps can be seen in Fig. 5, where the inductance is swept and the switching frequency that produces the lowest loss at each value of inductance is saved and recorded, which produces a Pareto front of inductance vs. loss.

The general trend that can be seen in these plots is that efficiency increases with inductance. The optimal operating point to maximize efficiency was placed in the range of $L = 450\mu H$ and $f_{sw} = 20kHz$ as inductances higher than this



Fig. 7. One of the six segments used to create the battery.

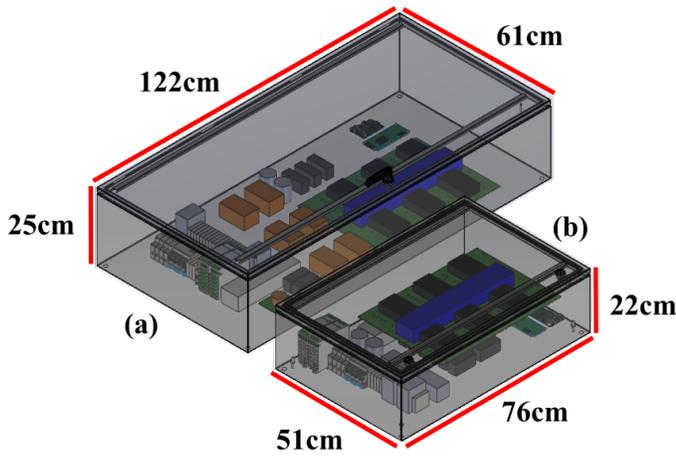


Fig. 8. 3d charger prototype renderings. (a) Charger version 1. (b) Charger version 2.

value can be considered past the point of diminishing returns with respect to efficiency. However, by modern standards, this is a relatively low switching frequency and a high inductance. This will result in a relatively large charger volume. Another point along this curve at $L = 45\mu H$ and $f_{sw} = 80kHz$, is explored to demonstrate the relationship between size and efficiency. Two prototypes are constructed, version 1 at the $450\mu H$ point and version 2 at the $45\mu H$ point, and the results are discussed in Section IV.

D. LCL Filter

Design of the LCL filter, highlighted in Fig. 2 of the overall topology, hinges on two requirements. First, the filter as a whole has to remove sufficient high frequency components of the PWM waveform to maintain compliance with the standards listed in Tables II and III. The resonant frequency of this filter is calculated in conjunction with the switching frequency, and is set to be less than one half of the switching frequency in conjunction with. The resonant frequency of this filter is calculated with

$$f_{res} = \frac{1}{2\pi} \sqrt{\frac{L_i + L_g}{L_i L_g C_f}}. \quad (13)$$

With L_i chosen in the previous section for maximum efficiency, C_f can be sized in conjunction with ripple voltage

TABLE IV
PARAMETERS OF VERSION 1 AND VERSION 2 PROTOTYPES

Parameters	Values
Rated power	22kW
Grid voltage	480V _{AC, L-L}
Battery voltage	200 – 650V _{DC}
DC Bus voltage	900V
Switching frequency	V1:20kHz ; V2:80kHz
Switching inductor	V1:450μH ; V2:45μH
Output inductor	45μH
Filter capacitance	V1:36μF ; V2:12μF
DC bus capacitance	216μF
Peak Efficiency	V1:99.5 % ; V2:98.3 %
Charger power density	V1:0.12kW/L ; V2:0.26kW/L
Power electronics power density	V1:1.54kW/L ; V2:2.31kW/L

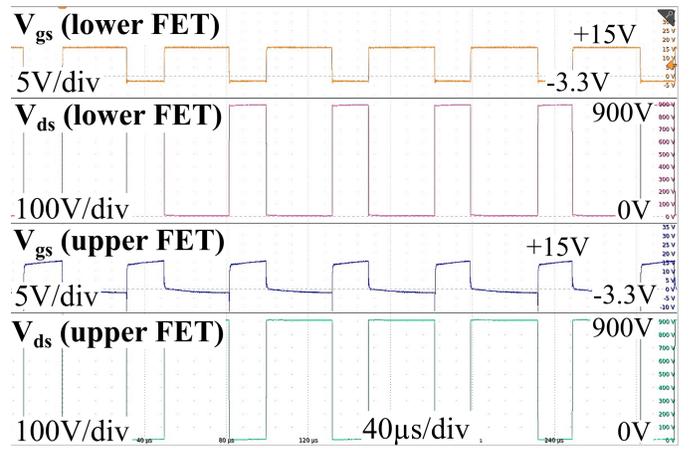


Fig. 9. V_{ds} and V_{gs} of one phase with a DC bus voltage of 900V.

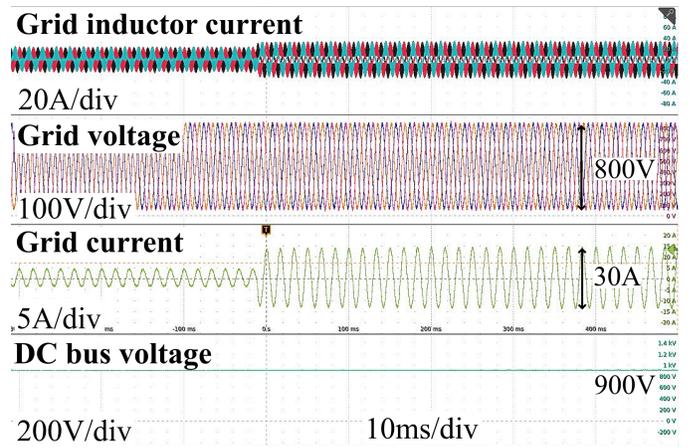


Fig. 10. 3kVA to 9kVA load step.

requirements. (4) can be used to calculate ripple current. Neglecting the effect of L_g , ripple voltage can be calculated as a function of ripple current using

$$V_{out,p-p} = \frac{I_{L,p-p}}{8f_{sw}C_f}. \quad (14)$$

Considering a value of 22A for $I_{L,p-p}$, a desired ripple voltage of 5V yields a minimum value of $27.5\mu F$ for C_f . This, in conjunction with (13), gives a required minimum L_g of $9.4\mu H$ for the prototype with $L_i = 450\mu H$. An identical process is repeated for the prototype version with $L_i = 45\mu H$.

TABLE V
HEATSINK DESIGN SPECIFICATIONS

Parameter	Value
P _{FET}	26W
T _{Ambient}	40°C
T _{Junction,max}	100°C
R _{θJC}	0.32°C/W
R _{θPad}	0.25°C/W
R _{θHeatsink}	0.13°C/W

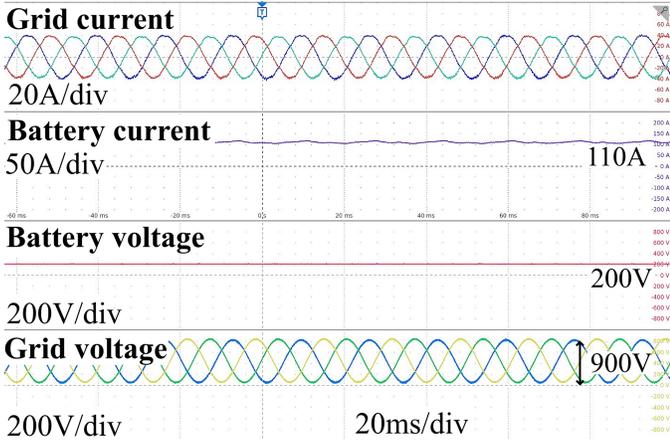


Fig. 11. Rated power charging with 200V battery.

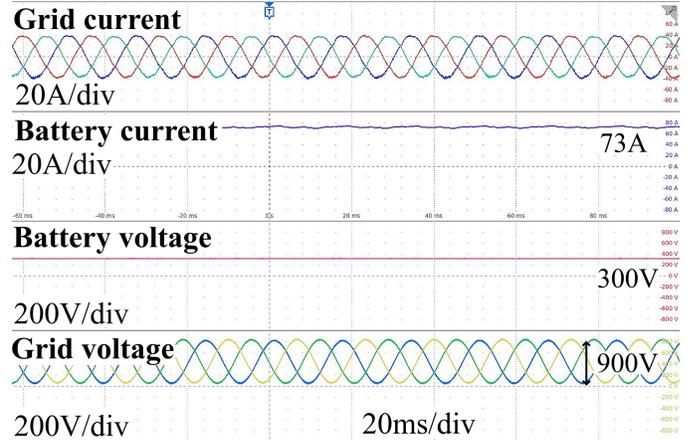


Fig. 13. Rated power charging with 300V battery.

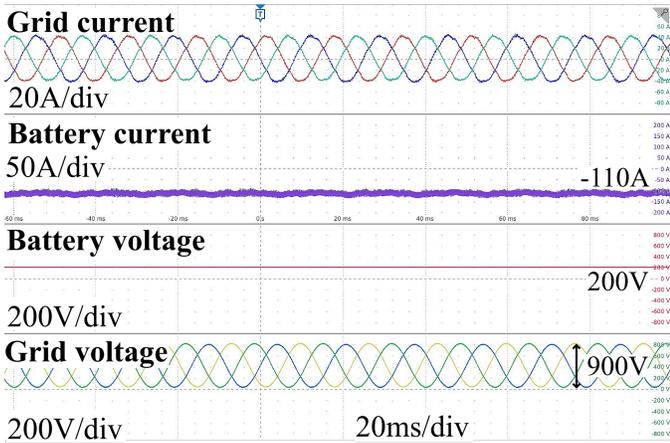


Fig. 12. Rated power discharging with 200V battery.

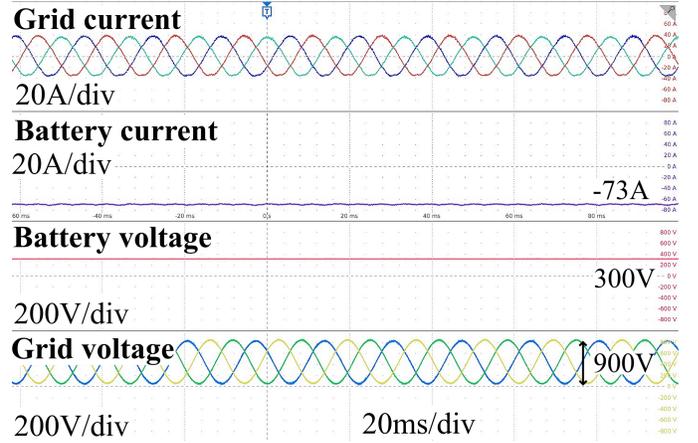


Fig. 14. Rated power discharging with 300V battery.

E. Heatsink Calculations

The physical layout of this charger is separated into six phases where each phase has its own heatsink. The loss per phase at the previously chosen operating point was determined to be 26W during the optimization process. Fujipoly SARCON XR-m thermal pads of 1mm thickness in conjunction with readily available server CPU heatsinks are used in this application. Conservative values were used for maximum allowable FET junction temperature $T_{junction}$ along with the ambient temperature $T_{ambient}$. The maximum FET power dissipation can be calculated with

$$P_{diss} = \frac{T_{junction} - T_{ambient}}{\frac{1}{2}(R_{\theta JC} + R_{\theta JC}) + R_{\theta Heatsink}}, \quad (15)$$

which represents the parallel combination of two FETs and thermal pads in series with the heatsink, where each FET and thermal pad are in series. Using (15) with the values in Table V yields a maximum heat dissipation in the range of 140W, sufficient for cooling the FETs under the previously determined operating conditions. Water cooling was considered for this application, however, the excess complexity associated with it as well as the insignificant thermal requirements of this charger makes it unnecessary.

IV. EXPERIMENTAL RESULTS

Both versions of the charger can be seen in Figs. 6 and 8 and their general operating parameters in Table IV. One of the six series segments used to create the battery can be seen in Fig. 7. Fig. 8 shows that the version 2 charger has an over 50% reduction in volume from the version 1 prototype, which is achieved through the increased switching frequency and reduced inductance at the cost of efficiency.

A. Switching Waveforms

The switching waveforms can be seen in Fig. 9. No overshoot is measured on the V_{ds} voltages of neither the upper FET nor lower FET. Minimal ringing is observed in the signals that drive the gates of the FETs. None of the phases are interleaved.

B. Transient Performance

Transient performance can be seen in Fig. 10 where the output power is stepped from 3kVA to 9kVA. During this load step the DC bus voltage remains constant and no noticeable fluctuations on the grid voltage can be seen. The grid current of a single phase shows an as expected increase, which is also

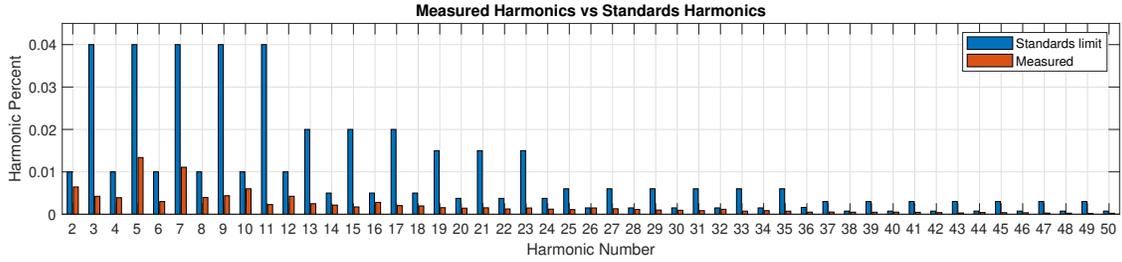


Fig. 15. Harmonic content of the charger relative to IEEE standards.

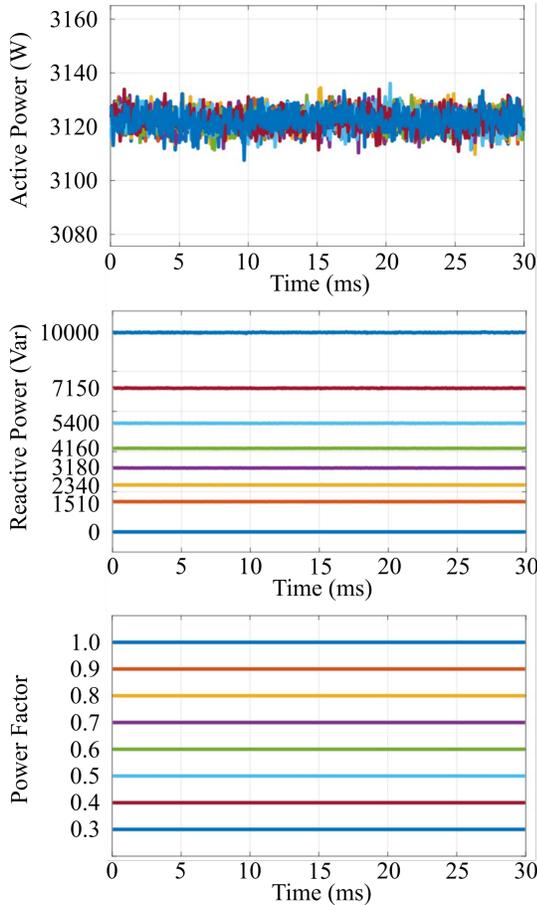


Fig. 16. Power factor control demonstration by varying the reactive power while active power is held constant.

Each color represents a different desired power factor test case.

reflected in the grid inductor current. No instabilities are noted during this transient.

C. Power Tests

This section shows experimental results of the charger operating at rated power in both charging mode and discharging mode for two different battery voltages. Three phase grid currents and voltages as well as battery current and voltage are provided. Figs. 11 and 13 show the charger operating at rated power to in charging mode. Figs. 12 and 14 show the charger operating at rated power in discharging mode.

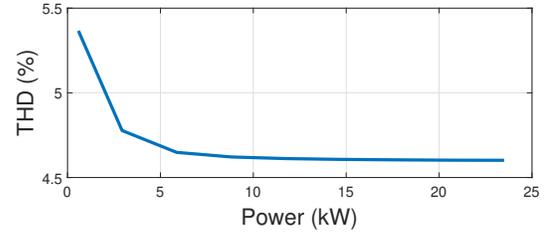


Fig. 17. THD performance as a function of power.

D. Power Factor

As the AC/DC side of this charger has an active rectifier, the power factor can be arbitrarily controlled. Fig. 16 shows varying the reactive power while the active power is held constant, resulting in control of the power factor over its entire range. Each color of Fig. 16 represents a single test case, where each test case is a unique combination of active power, reactive power, and the resulting power factor. Power factor for each test case is controlled by varying the reactive power. This shows how chargers of this design can be used to provide reactive power support to the grid.

E. Grid Quality

The grid quality results discussed in this section include both the THD as a function of output power and the lower frequency harmonic performance as it relates to UL2231 and IEEE1547 standards. The harmonic content of the grid current is measured at the point of common coupling between the charger and the grid connection. Fig. 17 shows that the THD is relatively constant with respect to power. Fig. 15 show that the charger is compliant with the harmonic content standards outlined in UL2231 and IEEE1547. This also has the implication of further proving that this transformerless topology is feasible for industrial applications.

F. Leakage Performance

Experimentally validating the leakage current is of increased importance with a charger of this topology as it is not galvanically isolated. Standards dictate that the voltage that drives the leakage current must be kept below $10V_{RMS}$ between the frequencies of 20Hz to 1MHz when measured through the circuit as seen in Fig. 18. The transfer function of the standards compliant measuring circuit is

$$\frac{V_{out}}{V_{in}} = \frac{s(C_1 R_1 R_2 + R_2)}{s^2(C_1 C_2 R_1 R_2 R_3) + s(C_2 R_2 R_3) + R_1 + R_2}. \quad (16)$$

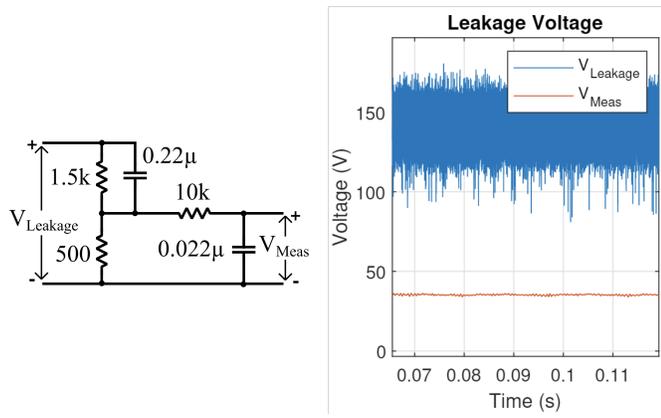


Fig. 18. UL standards compliant leakage voltage measuring circuit (left) and filtered and unfiltered leakage voltage (right).

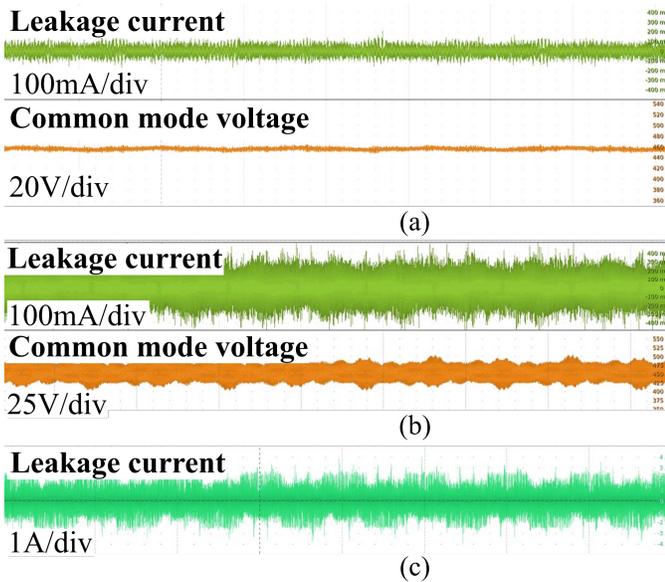


Fig. 19. Leakage current and leakage voltage of the charger under various control scenarios. a) Proposed charger with zero voltage control active. b) Proposed charger with zero voltage control disabled. c) Typical charger topology without zero voltage control.

The measured leakage voltage is first passed through the transfer function in (16) and then all frequencies outside of 20Hz to 1MHz are removed. The RMS of this signal is then calculated. This charger achieved a value of $4.22V_{RMS}$ during this test, under the standards defined limit of $10V_{RMS}$, proving this topology compliant with the relevant leakage standards, further implying the feasibility of this charger topology for industrial applications.

Fig. 19a shows the leakage current and voltage for the proposed charger with zero voltage control active. The leakage current is $15mA_{RMS}$, well below the $30mA_{RMS}$ standards limit. Fig. 19b shows the proposed charger with the zero voltage control disabled, resulting in a leakage current of $75mA_{RMS}$. Lastly, Fig. 19c shows a traditional topology with no zero voltage control which has a leakage current of $300mA_{RMS}$.

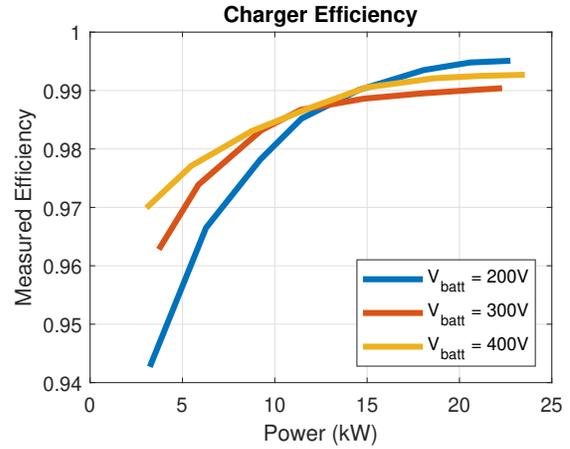


Fig. 20. Efficiency curves of charger for varying battery voltages while providing power to the grid.

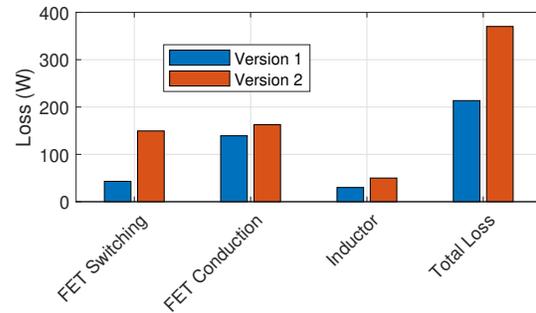


Fig. 21. Loss breakdown of Version 1 and Version 2 chargers.

G. Efficiency

The power conversion efficiency as a function of battery voltage can be seen in Fig. 20. The peak efficiency of 99.51% is reached at rated power (22kW) a battery voltage of 200V. Peak efficiency for a 400V battery is 99.04% and 99.27% for a 300V battery. Efficiency at one-half the rated power is above 98%. Fig. 21 shows the loss breakdown for both Version 1 and Version 2 of the charger when operating at rated power with a 400V battery. The total loss is experimentally measured, then the ratio of the individual loss mechanisms to the total loss is calculated using (1) - (12). This provides the individual loss mechanism values of Fig. 21.

From version 1 to version 2 the conduction and inductor losses increase slightly, but the switching losses increase significantly which can be attributed to the increased switching frequency. These values are in line with those calculated using the methods presented in Section III, however, it is worth noting that the measured efficiency is slightly higher than the calculated efficiency. Efficiency is measured using a Tektronix MSO58 oscilloscope IMDA power analyzer function.

V. CONCLUSION

This paper demonstrates the feasibility of transformerless charger architectures in non-academic environments and presents a formulaic approach to the design process. The benefits of the transformerless topology is evident in the high

efficiency of this charger. By conforming to relevant leakage current and current harmonics standards the industrial applications of this topology are proven. Potential improvements on this charger include increasing efficiency and power density. Neither the switches nor the passive components are operating near their current limits, so power density can be increased by simply increasing power output. Placing FETs in parallel can reduce the FET loss, improve efficiency and further increase the power output. Lastly, the layout of the physical charger can be optimized and compacted, resulting in decreased charger volume and increased power density.

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