Controllability Techniques for the Multilevel Power Converter Manhattan Topology

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***Abstract*—This paper explores the controllability of different configurations of the Manhattan Topology. The Manhattan Topology is a multilevel power converter topology that is defined by a set of series stacked capacitors where each capacitor establishes a voltage level. The functionality of the converter is built around the transfer of power between these capacitors. The methodology, quantity, and connectivity of the capacitive power transfer scheme is not specific to the Manhattan Topology. Different topology configurations will have different capacitive power transfer connectivities. A completely connected topology is not necessary for a fully controllable converter (where capacitor voltage balance of any arbitrary ratio can be maintained in steady state). For some practical implementations of the Manhattan Topology, it is also not feasible to connect all capacitive power transfer links together. Different link topologies will result in different levels of controllability. This paper shows three different link topologies: a fully controllable topology, a partially controllable topology, and a modification to the partially controllable topology that results in a fully controllable topology. Converter state-space models, controllability theory, and control diagrams are provided. Results are validated through high-fidelity simulation of example Manhattan Topology power converters that use the three different link topologies in DC/DC mode.**

I. Introduction

Multilevel power converters are inherently complex. They have an increased number of switching devices, passive components, and circuit states over their typical single-level counterparts. This is a necessary allowance as the bridging of higher voltage power conversion with lower voltage components comes at a cost. Distributing a higher voltage across multiple lower voltage components will inherently result in higher component quantities and more switching devices will result in more complex control. Multilevel power converters also allow for a reduction in required output filtering [1], [2] as the splitting of the output voltage into more discrete levels reduces the magnitude of undesired frequency harmonics [3].

A wide variety of multilevel topologies exist and advancing multilevel technologies is actively studied. Reducing the device count [4]–[6], improving THD [7]–[10], methods of maintaining voltage balance [11], and switch actuating techniques [12] are all current areas of research. Benchmarking different multilevel topologies is out of the scope of this paper but can be found in [13]–[17]. The Manhattan Topology is unique in that it provides inherent capacitor voltage balance in AC/DC and DC/DC operation, has simple a modular switch actuation control, and component quantities scale linearly with the number of levels [18]–[21].

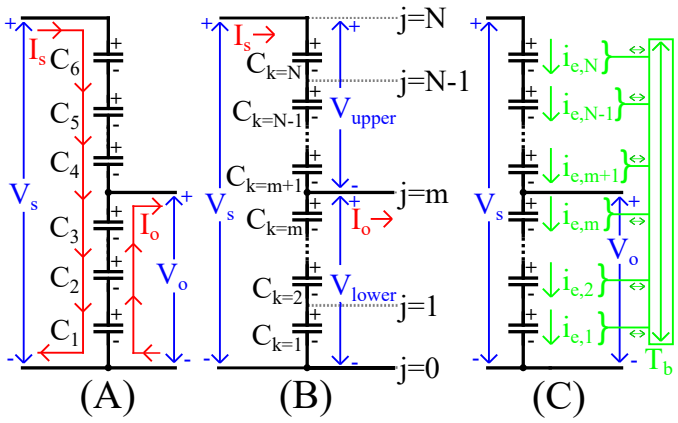

Fig. 1. Generalized Manhattan Configuration multilevel topological framework. (A): 6-level implementation. (B): N-level implementation. (C): capacitive power transfer scheme with connectivity of $\mathbf{T_b}$.

The Manhattan Topology is defined by a set of series stacked capacitors. Power is shared between capacitors through capacitive power transfer links. This allows for voltage balance, regardless of power level and voltage conversion ratio, to be maintained in steady state [19]. The basic Manhattan Topology power converter with obfuscated capacitive power transfer links can be seen in Fig. 1, which shows the case where all capacitors are linked together. This is not always practical or convenient, and as discussed in Section II, and shown in III and IV, is not explicitly necessary. As this topology can be a multi-input multi-output power converter with multiple control states that all scale with the number of levels, it is necessary to study the the types and quantities of links that are necessary for a given Manhattan Topology configuration to be fully functional, which is the intention of this paper.

II. Theory

The theory within the scope of this paper pertains to the state-space model for the generalized Manhattan Topology. More in depth circuit analysis can be found in [18]–[21]. The state-space model considers the capacitor voltages as states and begins with defining the relationship between capacitor voltage and current

$$dV_c = \frac{I_c}{C} dt, \tag{1}$$

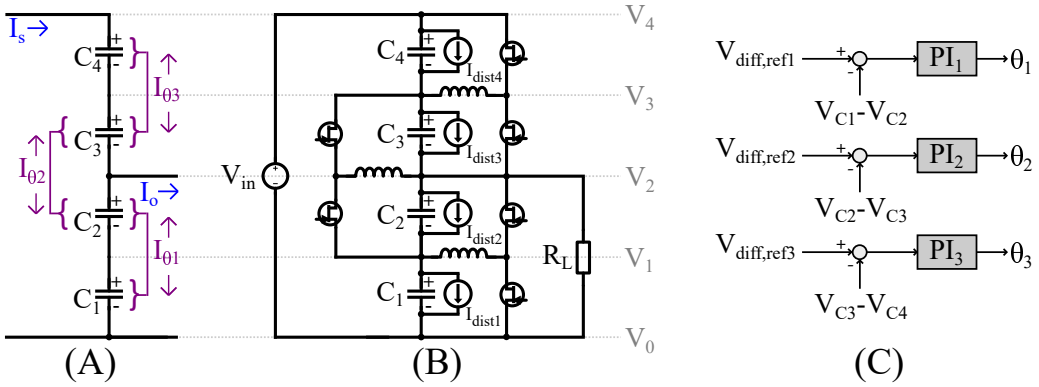

Fig. 2. Fully controllable example Manhattan Topology consisting of three half-bridge capacitive power transfer links. (A): internal power flow diagram. (B): converter schematic, drawn with disturbance current sources used for validation. (C): control topology.

where V_c is the capacitor voltage, C is the capacitance value, and I_c is the total capacitor current.

As can be seen in Fig. 1, there are multiple mechanisms that define the total capacitor current. (1) can be modified to reflect this and results in

$$dV_c = \frac{i_e + i_b}{C} dt, \tag{2}$$

where i_e is the current due to the externalities of input current I_s and output current I_o where $i_e = [I_s, I_o]'$. i_b is the current due to internal capacitive power transfer links. i_e and i_o will change for different configurations of the Manhattan topology. Topology matrices T_b and T_e are included to make allowances for these different configurations of capacitive power transfer links and input/output node configurations, respectively. T_b for different configurations is shown in Section III.

The complete state space formulation can then be written as

$$V_c^+ = V_c + \frac{T_s}{C}\mathbf{T_b} i_b + \frac{T_s}{C}\mathbf{T_e} i_e, \tag{3}$$

with a constraint of

$$V_c \mathbf{T_b} i_b = 0. \tag{4}$$

This constraint denotes that the power transferred internally within the capacitive power transfer links is conserved. T_s is the sample interval of the controller and is defined by the practical controller implementation (and not the circuit itself). The state-space model of (3) can be used to determine the controllability of the system it describes.

Gleaning controllability (and observability) from a state-space model is straightforward and well-known process. For a given state-space model of the form of

$$x^+ = \mathbf{A}x + \mathbf{B}u, \tag{5}$$

a controllability matrix C can be derived

$$\mathbf{C} = [\mathbf{B}|\mathbf{AB}|\mathbf{A}^2\mathbf{B}|\dots|\mathbf{A}^{n-1}\mathbf{B}], \tag{6}$$

where n is the rank of $\mathbf{A}$. If the system is fully controllable then all of the columns of C will be linearly independent and its rank will be full. In the context of the state-space model of (3), $\mathbf{C}$ can be rewritten as $\bar{\mathbf{C}}$ of

$$\bar{\mathbf{C}} = [\mathbf{I}|\mathbf{IT_b}|\mathbf{I}^2\mathbf{T_b}|\dots|\mathbf{I}^{n-1}\mathbf{T_b}], \tag{7}$$

where $\mathbf{I}$ is the identity matrix. This shows that the controllability of the topology depends wholly on $\mathbf{T_b}$ and not on any other element within the state-space equation of (3) or its constraint of (4). Lastly, in the context of this converter, the rank does not need to be full as the sum of the capacitor voltages is

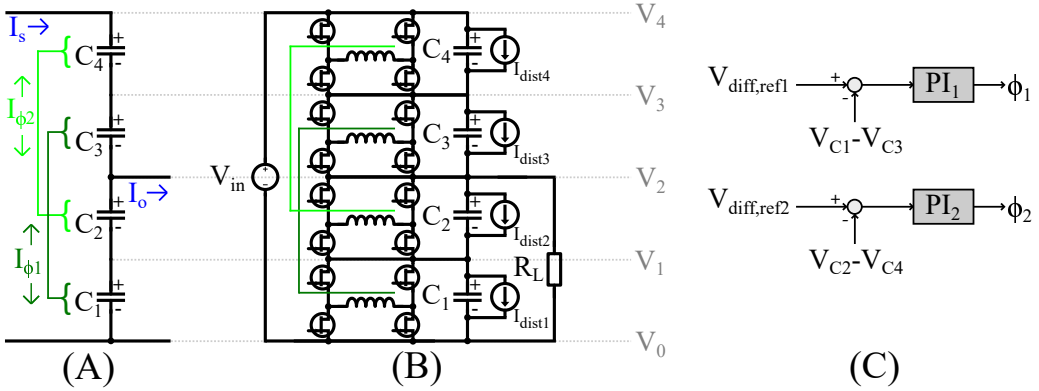

Fig. 3. Partially controllable example Manhattan Topology consisting of two dual-active-full-bridge (DAFB) capacitive power transfer links. (A): internal power flow diagram. (B): converter schematic, drawn with disturbance current sources used for validation. (C): control topology.

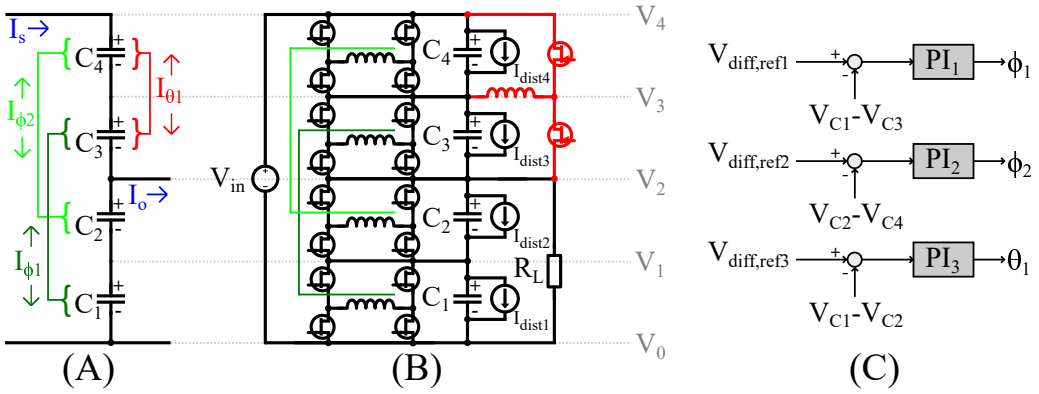

Fig. 4. Fully controllable example Manhattan Topology consisting of two dual-active-full-bridge (DAFB) and one half-bridge capacitive power transfer links. (A): internal power flow diagram. (B): converter schematic, drawn with disturbance current sources used for validation. (C): control topology.

controlled by the input voltage V_{in} and this is not reflected in the state-space model. Instead, for full controllability, the rank of $\bar{\mathbf{C}}$ must be one less than full. This is written explicitly as

$$rank(\bar{\mathbf{C}}) = n - 1, \tag{8}$$

where n is conveniently equal to the number of capacitors in the center capacitance stack of the converter.

The following section follows the derivation of $\mathbf{T_b}$ and the resulting controllability matrices $\bar{\mathbf{C}}$ for different configurations of the Manhattan Topology.

III. Controllability of Different Manhattan Topology Configurations

Three different configurations of the Manhattan Topology are shown in this section. These were chosen to demonstrate the fully controllable case, the partially controllable case, and a modification to the partially controllable case to make it fully controllable. A basic 4-capacitor 4-level center capacitor stack is used for all configurations to maintain simplicity and consistency.

The first of the three configurations can be seen in Fig. 2. This configuration represents the fully controllable case and consists of a three of half-bridge modules as the capacitive power transfer links. This configuration is discussed in detail in [18] and has topology matrix $\mathbf{T_{b1}}$ and link power transfer quantities i_{b1} of

$$i_{b1} = \begin{bmatrix} I_{\theta 1} \\ I_{\theta 2} \\ I_{\theta 3} \end{bmatrix} \quad \mathbf{T_{b1}} = \begin{bmatrix} 1 & 0 & 0 \\ -1 & 1 & 0 \\ 0 & -1 & 1 \\ 0 & 0 & -1 \end{bmatrix}. \tag{9}$$

The second configuration is of Fig. 3 which represents the partially controllable case and consists of dual-active-full-bridge (DAFB) capacitive power transfer links. One required capacitive power transfer link is missing which results in partial controllability. This configuration is discussed in [19] and has topology matrix $\mathbf{T_{b2}}$ and link power transfer quantities i_{b2} of

$$i_{b2} = \begin{bmatrix} I_{\phi 1} \\ I_{\phi 2} \end{bmatrix} \quad \mathbf{T_{b2}} = \begin{bmatrix} 1 & 0 \\ 0 & 1 \\ -1 & 0 \\ 0 & -1 \end{bmatrix}. \tag{10}$$

The third and last configuration is of Fig. 4 which includes a modification to the partially controllable case that allows for it to become fully controllable. This modification is an additional half-bridge, highlighted in red and connected in a strategic location that provides a necessary power transfer link between two adjacent capacitors. Configuration 3 has topology matrix $\mathbf{T_{b3}}$ and link power transfer quantities i_{b3} of

$$i_{b3} = \begin{bmatrix} I_{\phi 1} \\ I_{\phi 2} \\ I_{\theta 1} \end{bmatrix} \quad \mathbf{T_{b3}} = \begin{bmatrix} 1 & 0 & 1 \\ 0 & 1 & -1 \\ -1 & 0 & 0 \\ 0 & -1 & 0 \end{bmatrix}. \tag{11}$$

The controllability matrix $\bar{\mathbf{C}}_\mathbf{1}$ resulting from $\mathbf{T_{b1}}$ of configuration 1 has rank 3, implying full controllability. The controllability matrix $\bar{\mathbf{C}}_\mathbf{2}$ resulting from $\mathbf{T_{b2}}$ of configuration 2 has rank 2, implying partial controllability. Lastly, the controllability matrix $\bar{\mathbf{C}}_\mathbf{3}$ resulting from $\mathbf{T_{b3}}$ of configuration 3 has rank 3, implying full controllability. These claims are validated in section IV.

IV. Results

The controllability of the different configurations is validated through high fidelity simulation. The circuits and their control diagrams used for validation can be seen in Figs. 2, 3, and 4.

Validation is a two-step process. The first step is for the converter to reach a steady state operating point from a zero initial condition. During this time to reach a steady state operating point the disturbance current sources $I_{dist1-4}$ are set to 0. The second step in validation is for the disturbance current sources $I_{dist1-4}$ to activate and produce a disturbance on each capacitor voltage. This shows the converter's ability to compensate and maintain the reference steady state operating point.

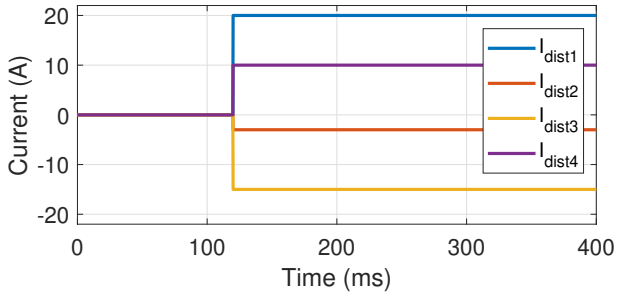

Fig. 5. Disturbance current sources used for controllability validation.

PI control is used exclusively. Each module has its own controller (a half-bridge is a single module and a DAFB is a single module) and all PI controllers are identical. The V_{diff} references are all set to 0, implying that the target state is an even split of the input voltage V_{in} across all four capacitors ($V_{C1} = V_{C2} = V_{C3} = V_{C4} = 0.25V_{in}$). It is worth noting that this is an unoptimized control scheme and is used to demonstrate controllability and not control performance.

The disturbance current sources $I_{dist1-4}$ have values of $I_{dist1} = 20A$, $I_{dist1} = -3A$, $I_{dist1} = -15A$, and $I_{dist1} = 10A$. These are arbitrary values and all disturbance current sources activate at $t = 0.12$s and are the same for each of the three configurations. These disturbances can be seen in Fig. 5.

Lastly, all configurations have the circuit parameters of $C = 30\mu$F, $L = 20\mu$H, and switching frequency $F_{sw} = 100$kHz. All transformers have a 1:1 turns ratio, leakage inductance equal to L, and coupling coefficient of 1. The input voltage is

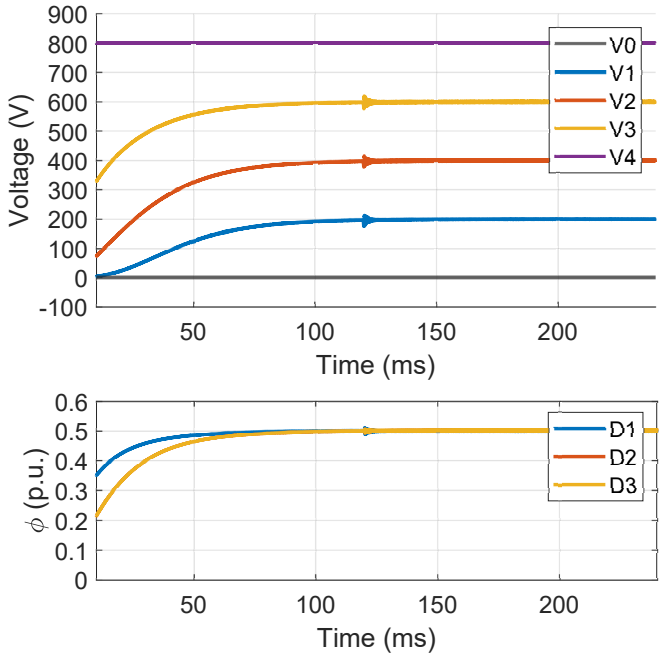

Fig. 6. Configuration 1 results. Upper: Level voltages. Lower: Duty cycles of the three half-bridge modules.

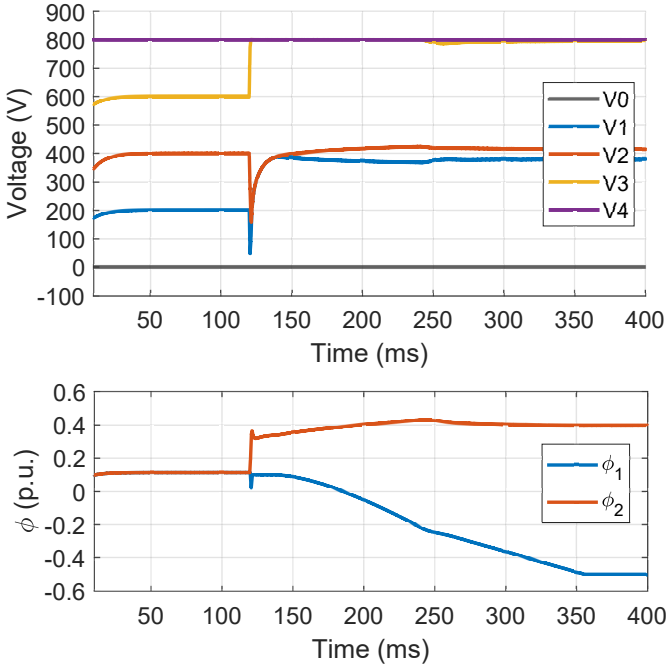

Fig. 7. Configuration 2 results. Upper: Level voltages. Lower: normalized phase difference ϕ of the two DAFB modules.

$V_{in} = 800$V and the load resistance is $R_L = 40\Omega$.

Fig. 6 shows the level voltages and module duty cycles of Configuration 1 (Fig. 2) during the initial settling and the introduction of the disturbances. It can be seen that the the steady state operating point is successfully achieved and the duty cycles settle on an expected value of 0.5. The introduction of the disturbances cause some fluctuations but the steady state operating point is maintained. Full controllability is achieved.

Fig. 7 shows the level voltages and normalized phase differences ϕ, respectively, of Configuration 2 (Fig. 3) during both the initial settling period and the introduction of the disturbances. This configuration achieves the steady state operating point. This can be attributed to the identical PI controllers, as during the initial settling period both DAFBs are effectively doing the same thing. However, this configuration fails when the disturbances are introduced. This is because this configuration is not fully controllable and it lacks the ability to transfer power between the DAFBs. The result of this is that one DAFB supports the whole input voltage and the voltage of the other DAFB is driven to zero.

The fix for Configuration 2 is to add a method for power transfer between the two DAFBs. One way is to include an additional half-bridge module that connects the two DAFBs, which results in Configuration 3 (Fig. 4). Fig. 8 shows the level voltages, normalized phase differences ϕ, and duty cycle D, of this configuration. It can be seen that the the steady state operating point is achieved and that the disturbances do cause fluctuations but ultimately the operating point is maintained. The addition of this strategically placed half-bridge allows for full controllability.

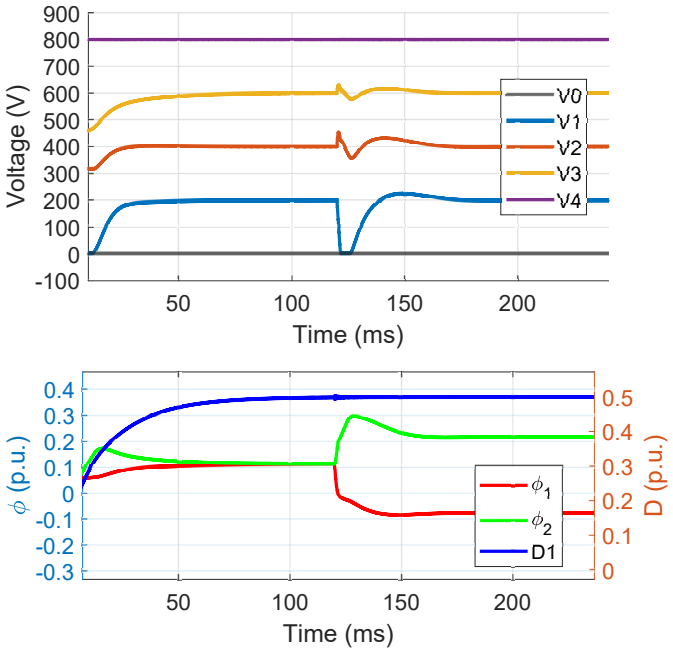

Fig. 8. Configuration 3 results. Upper: Level voltages. Lower: normalized phase difference ϕ of the two DAFB modules and duty cycle D of the half-bridge module.

V. Conclusion

This paper is the first introduction in control limitations and considerations of the Manhattan Topology. Controllability theory and necessary conditions as they relate to the Manhattan Topology are shown. Example circuits with varying levels of controllability are discussed and their stability results postulated. Lastly, the postulated stability results are confirmed through simulation. Further work on this topic involves building an experimental prototype to validate the simulated results.

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