A Fully Balanced Vertically Stacked Multilevel Power Converter Topology with Linear Scaling using Dual Active Half Bridge Converters

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Abstract—This paper proposes a novel multilevel power converter topology that can be expanded to an arbitrary N number of levels. The topology is modular in nature, consisting of groupings of three degrees-of-freedom dual active half bridge (3D-DAHB) switching cells that can be stacked and reconfigured to achieve any desired number of levels. Each DAHB can move power between any of its four associated capacitors, allowing for stacked DAHBs to distribute voltages arbitrarily around all capacitors in the stacked configuration, resulting in a multilevel topology of arbitrary level voltages. Component quantities and component stresses scale linearly with the number of levels. Internal power flows are exclusively a product of input/output parameters and not the number of levels. Dynamic equations for the topology that can be used to determine the capacitor voltages and required capacitor power transfers are provided. A simplified circuit model is derived alongside methods of expanding this topology to N-levels. Functionality of the proposed converter is demonstrated through high-fidelity simulation of a 9-level converter.

I. Introduction

Improvements in switching device technology and/or the application of multilevel topologies becomes increasingly necessary as society trends towards higher voltages. High Voltage DC (HVDC) power transmission is increasing in popularity and is presently beyond the MV range [1], [2]. Electric Vehicle (EV) batteries have steadily increased in voltage since their most modern introduction [3]. These applications require their associated power electronics to be able to also withstand these higher voltages.

Progressions in switching technology have enabled typical 2-level converter topologies to be able to withstand higher voltages. Modern Silicon Carbide (SiC) devices can withstand >1200V [4], [5], allowing for the safe control and conversion of 2-level topologies for voltages in the range of 900V. However, the control and conversion of voltages higher than the intrinsic blocking voltage of the chosen switching device will require some variation of a multilevel topology.

Multilevel power converters can also be applied in scenarios where they are not required, i.e. lower voltage applications. They can offer better quality input/output voltages in conjunction with smaller filters [6]. They have proven benefits in EVs [7], HVDC applications, [8], and medical devices [9].

Adapting a design for a multilevel topology does incur a cost, most notably associated with the increased circuit and control complexity of multilevel converters. Multilevel topologies are already a highly studied area of research and many topologies already exist, each with their own respective qualities. It is not straightforward to quantify control complexity, however, component quantities can be easily measured and a comparison between different component quantities can be seen in Table I.

Diode-clamped, capacitor-clamped, and the generalized D-shaped converters have exponentially increasing component counts as a function of number of levels [10], [11]. Modular Multilevel converters (MMC) have unbalanced voltages in steady state, making DC/DC implementations of these topologies challenging [13]. The full-bridge MMC improves over the half-bridge MMC with respect to flexibility in capacitor voltages and balancing but comes at the cost of increased switching devices and control complexity [14]. Likewise, the diode-clamped, capacitor clamped, and generalized D-shaped topologies also require extra attention to keep capacitor voltages balanced, more so as the number of levels increases [15]–[17].

The proposed topology is a derivation of the multilevel topology used in [12], which is an adaption of the high conversion ratio converters found in [18], [19]. These high conversion ratio converters are intended to be used in applications where the output voltage is a small fraction of the input voltage. Similar high conversion ratio topologies can be found in [20]–[22], with AC/DC implementation in [23].

In contrast, the half-bridge (HB) Manhattan topology of [12] are not intended for high conversion ratios but as a multilevel topology with an output voltage that can swing across the full input voltage. It can maintain capacitor voltage balance

TABLE I
NUMBER OF COMPONENTS IN N-LEVEL CONVERTER TOPOLOGIES

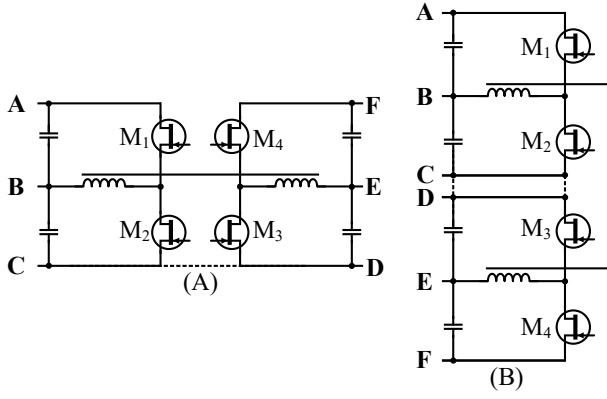| Topology	Semiconductors	Inductors	Capacitors
Diode-Clamped [10]	$N^2 - N$	1	$N - 1$
Capacitor-Clamped [10]	$2(N - 1)$	1	$(N - 1) + \frac{N^2 - 3N + 2}{2}$
Generalized D-shaped [11]	$N(N - 1)$	1	$\frac{N^2 + N}{2} - N$
Half-Bridge MMC [8]	$4(N - 1)$	2 or $4(N - 1)$	$2(N - 1)$
Full-Bridge MMC [8]	$8(N - 1)$	2 or $4(N - 1)$	$2(N - 1)$
Manhattan (HB) [12]	$2(N - 2)$	$N - 2$	$N - 1$
Manhattan (DAHB)	$N - 1$	$\frac{N - 1}{2}$	$N - 1$

Fig. 1. DAHB unit cell of proposed multilevel topology. a) Isolated DAHB. b) DAHB reconfigured and stacked to create non-isolated multilevel converter.

while bidirectionally converting AC/DC or DC/DC through its independently operable unit switching cells. Component quantities scale linearly with the number of levels. However, the HB Manhattan topology of [12] requires circulating currents to maintain capacitor voltage balancing, and as a result, component stresses do not scale linearly.

The proposed DAHB Manhattan topology exchanges the HB switching cells of [12] with DAHB switching cells. The resulting topology requires half the number of switches and inductive components. In addition, the DAHB Manhattan converter mitigates the circulating loop currents present in the HB Manhattan topology [12], resulting in linear scaling of both component quantities and component stresses. To the authors knowledge, it is therefore the first fully balanced power electronic topology that scales linearly in all respects to N levels. Hence, the Manhattan topology can be interpreted as an alternative to the MMC.

II. TOPOLOGY DESCRIPTION

The topology of the unit cell upon which this converter is constructed can be seen in Fig. 1. The unit cell is identical to the dual active half-bridge (DAHB), where there are two half-bridges that share an inductive coupling. Important to note is the isolation between both half-bridges, the characteristics of which are leveraged in the stacking of unit cells to create a multilevel topology, which can be seen in Fig. 1-(b). Configuring the single unit cell into a multilevel topology involves connecting nodes C and D together across the isolation barrier and "folding" the inductive coupling to create a set of series stacked capacitors. The set of series stacked capacitors is the basis upon which this multilevel topology is constructed.

Characteristics of the DAHB allow for the voltages of each capacitor within the DAHB to be controlled to any arbitrary ratio with the caveat that the total stored power within these capacitors does not change. This functionality persists when the DAHB is reconfigured from Fig. 1-(a) into the stacked topology of Fig. 1-(b). For the circuit of Fig. 1-(b), input can be applied across nodes A and F and the output can be taken across nodes C/D and F. In this manner the input voltage
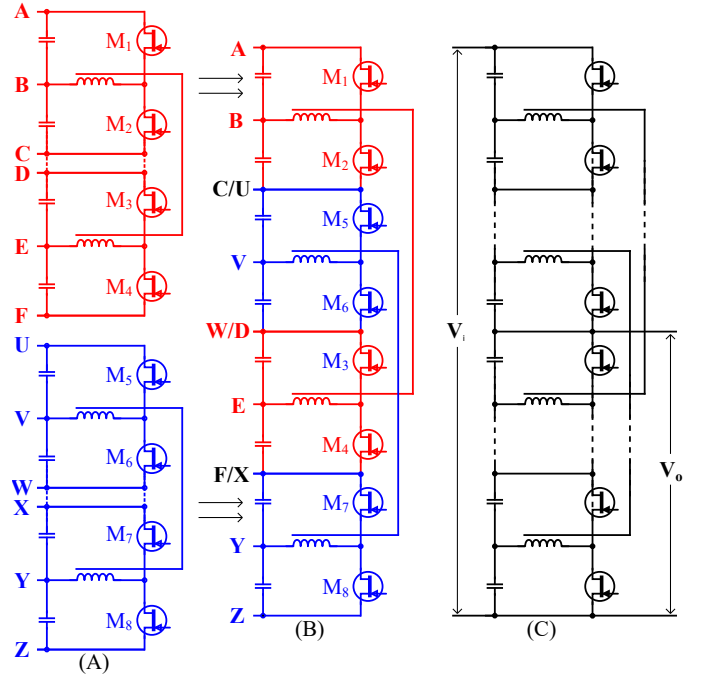

Fig. 2. Stacking of unit cells to create a multilevel topology. a) Two DAHB unit cells. b) Placement and connectivity of the two DAHB unit cells of (a) to create a 9-level converter. c) (these need output nodes) (and color code them).

stresses can be split across the series combination of the four capacitors that compose the center capacitance stack. The output voltage is likewise split along the two capacitors across which the output voltage is taken. Furthermore, the voltage seen by each switching device is split in an identical manner as the voltage split along the center capacitance stack. This allows for the single DAHB to effectively be used as a multilevel
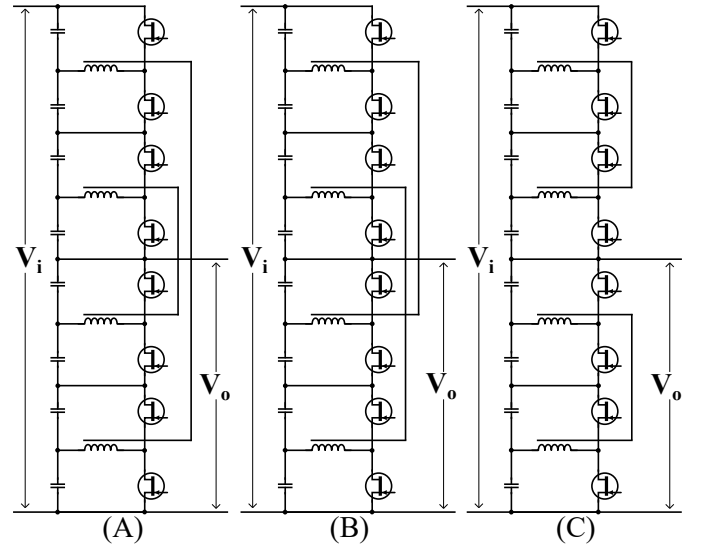

Fig. 3. Allowable couplings for stacked unit cells. a) Allowed symmetric coupling scheme. b) Allowed asymmetric coupling scheme. c) Disallowed coupling scheme.
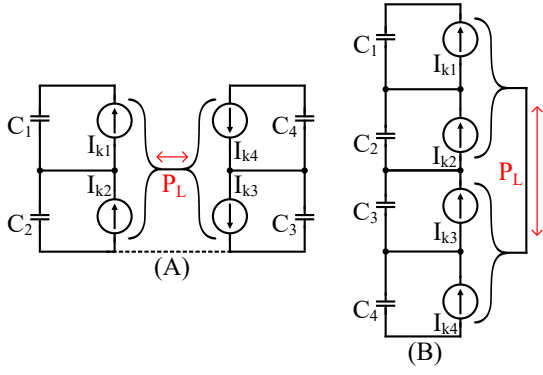
Fig. 4. DAHB unit cell current source model. a) DAHB unit cell isolated current source model. b) non-isolated stacked DAHB current source model.
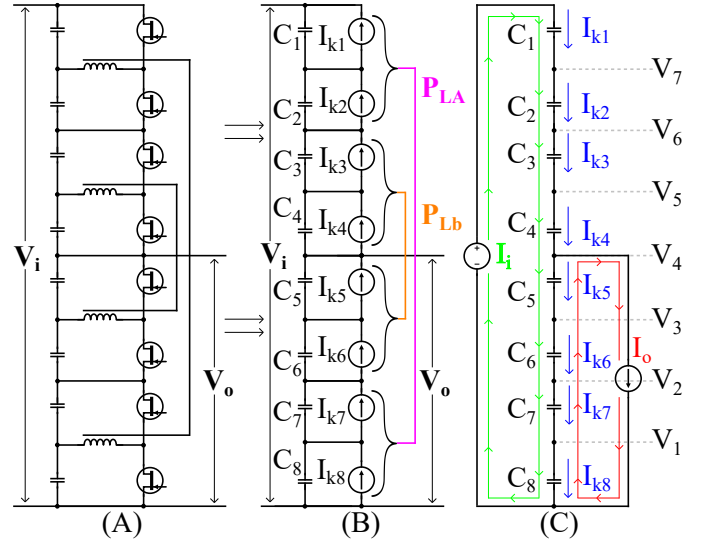

Fig. 5. Unit switching cell current source model derivation. a) 9-level complete converter. b) 9-level simplified current source model. c) Capacitor currents within the simplified model.

topology as the converter's input and output voltages can be higher than the voltage ratings of any individual switching device or capacitor.

The stacking of multiple unit cells into a multilevel topology with increased number of levels (and therefore an increased number of series capacitors in the center capacitance stack) follows a similar process and can be seen in Fig. 2. Multiple half bridges (HB) are connected in series to increase the number of levels in the center capacitance stack. The inductors of each HB are then coupled in pairs, creating a set of stacked DAHB unit cells. It is important to note, however, that the inductive coupling of each DAHB unit cell must cross the output node. There are multiple allowable coupling schemes, the quantity of which increases as the number of DAHB unit cells increases. The two allowable coupling schemes for a 9-level (8-capacitor) converter of the proposed topology can be seen in Fig. 3. This is a necessary condition to meet as internal power flows require that power from the HB cells above the output node be transferred to the HB cells below the output node to maintain power balance in steady-state. The reasoning for this is discussed in the following analysis section.

The inductive coupling scheme allows for the circulating currents present in the Manhattan HB topology to be eliminated entirely. Although component quantities scale linearly in the Manhattan HB topology [12], due to the circulating currents the component stresses do not, and as a result scaling to N-levels is technically feasible but practically impossible in [12]. The circulating currents in the Manhattan HB toplogy are required to maintain capacitor voltage balance in steady-state. The inductive couplings of the proposed Manhattan DAHB topology allow for the necessary power flows to maintain capacitor voltage balance in steady state without circulating currents, resulting in complete linear scaling to N-levels in both component quantity and component stresses.

III. ANALYSIS OF 9-LEVEL CONVERTER

Analysis of the proposed topology first begins with analysis of the DAHB unit cell. DAHB analyses are not novel in the scope of this paper and have been previously studied [24], [25]. As it is possible to transfer power in and out of any capacitor

within a DAHB, the inductive coupling and switches can be removed and replaced with current sources in parallel with each capacitor. This model can be seen in Fig. 4. This type of DAHB model operates under the constraint of

$$V_{C1}I_1 + V_{C2}I_2 + V_{C3}I_3 + V_{C4}I_4 = 0 \qquad (1)$$

where power is conserved and the sum of all the powers from each current source is zero. This model does not consider any external current inputs or outputs as these are treated as separate mechanisms. Like the DAHB unit cell, this model can be stacked to become representative of a stacked capacitor multilevel converter.

Although this topology can be expanded to an arbitrary N number of levels, for the sake of brevity, this analysis will follow a converter with $N = 9$ number of levels consisting of 8 series capacitors in the center stack. The 9-level converter of the proposed Manhattan DAHB topology can be seen in Fig. 5-(a), which uses the inductive coupling topology of Fig. 3-(a). The simplified current source model can be seen in Fig. 5-(b).

Derivation starts with defining the capacitor voltages. The change in voltage within a capacitor as a function of its current can be calculated with

$$\frac{dV_c(t)}{dt} = \frac{1}{C}i_c(t), \qquad (2)$$

where $i_c(t)$ is the capacitor current, $V_c(t)$ is the capacitor voltage, and C is the capacitor capacitance. The current into each capacitor can be seen in Fig. 5-(c). Analytically, these currents can be used in conjunction with (2) to calculate $\frac{dV_c(t)}{dt}$:

$$\dot{V_c} = \mathbf{C}^{-1}(I_k + \mathbf{T_k}I_u) \qquad (3)$$

where $\dot{V_c}$ is a vector of capacitor voltage deltas $\dot{V_c} = [\frac{dV_{C1}(t)}{dt}, \frac{dV_{C2}(t)}{dt}, \dots \frac{dV_{C8}(t)}{dt}]'$, C is a matrix of capacitances
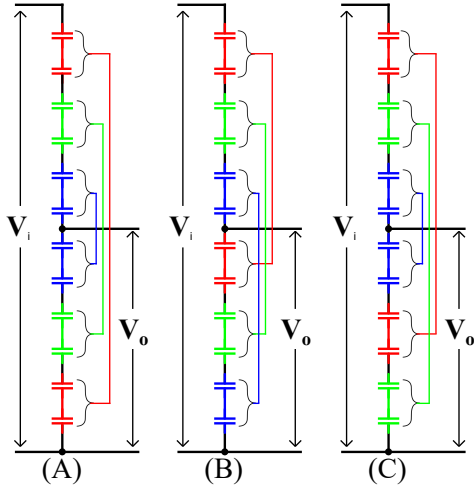
Fig. 6. Example inductive coupling schemes.

$\mathbf{C} = \text{diag}[C_1, C_2, \ldots C_8]'$, I_k is a vector of currents transferred over the inductive coupling of the DAHB $I_K = [I_{k1}, I_{k2}, \ldots I_{k8}]'$, I_u represents the external current flows $I_u = [I_i, I_o]'$, and $\mathbf{T_k}$ is a topology matrix that represents the connectivity of the input and output nodes. For the 8-capacitor converter considered in this analysis,

$$\mathbf{T_k} = \begin{bmatrix} 1 & 0 \\ 1 & 0 \\ 1 & 0 \\ 1 & 0 \\ 1 & -1 \\ 1 & -1 \\ 1 & -1 \\ 1 & -1 \end{bmatrix}. \tag{4}$$

$\mathbf{T_k}$ also represents the direction of current flow of the external input and output currents. This shows how it is necessary to transfer power from cells above the output node to cells below the output node to maintain capacitor voltage balance in steady state. The output current exclusively draws power from the capacitors below the output node as seen in Fig. 5-(c), necessitating inductive couplings that span the output node and transfer power from the upper capacitors to the lower capacitors to compensate for the output current and maintain capacitor voltage balance.

The DAHB unit cells transfer internal power over the inductive coupling, and as stated previously, all powers contained in I_k must sum to zero. However, this is not wholly the case, as the power transferred in each unit cell DAHB must also be conserved and sum to zero. A constraint on the internal currents I_k is developed that maintains the internal power flow:

$$I_k \mathbf{V}^{-1} \mathbf{T_u}' = 0, \tag{5}$$

where $\mathbf{V}$ is a matrix of capacitor voltages $\mathbf{V} = \text{diag}[V_{C1}, V_{C2}, \ldots V_{C8}]'$, and $\mathbf{T_u}$ is a topology matrix that represents how the inductive couplings are paired. For the 8-

capacitor converter considered in this analysis,

$$\mathbf{T_u} = \begin{bmatrix} 1 & 0 \\ 1 & 0 \\ 0 & 1 \\ 0 & 1 \\ 0 & 1 \\ 0 & 1 \\ 1 & 0 \\ 1 & 0 \end{bmatrix}, \tag{6}$$

where the values in the first column of $\mathbf{T_u}$ represent the capacitors that inductive coupling P_{LA} can share power with and the values in the second column represent the capacitors the second inductive coupling P_{LB} can share power with. The constraint of (5) and (6) serves two purposes, not only does it ensure that the internal power flows as a whole follow the law of conservation of energy, but also ensures that that the individual DAHB unit cells do not also violate this law.

For steady state operation, vector $\dot{V}_c$ can be set to zero as the capacitor voltages do not change in steady state. In conjunction with (3), for vector $\dot{V}_c$ to equal zero, then the term $\mathbf{C}^{-1}(I_k + \mathbf{T_u}I_u)$ must equal zero and

$$I_k = -\mathbf{T_u}I_u, \tag{7}$$

as $\mathbf{C}^{-1}$ term can be removed. This term is also not present in any constraint, suggesting that the capacitance value does not impact the steady state operation. It can be seen that

$$I_{k1-4} = -I_i \tag{8}$$
$$I_{k5-8} = -I_i + I_o, \tag{9}$$

is the only solution to (7). Therefore the constraint of (5) dictates the allowable capacitor voltages and not the allowable internal current flows, which are dictated by the input and output currents of the converter.

Characteristics of the DAHB unit cell allow for the voltage across the center capacitor stack of the converter to be set to any arbitrary ratio of the input voltage V_i. There are multiple allowable values for these sets of voltages that satisfy the constraint of (5). One allowable set of note is the one that represents ideal voltage splitting across the capacitors. To maintain the minimum voltage stress of each capacitor (and therefore also each capacitor's associated switch) across the entire output voltage range $0 < V_o < V_i$, the capacitors below the output node must evenly split the output voltage V_o and the capacitors above the output node must evenly split the voltage $V_i - V_o$. Analytically, this is

$$V_{C1-4} = \tfrac{1}{4}(V_i - V_o) \tag{10}$$
$$V_{C5-8} = \tfrac{1}{4}V_o \tag{11}$$

The voltages of (10)-(11) in conjunction with the currents of (8)-(9) satisfy the constraint of (5) as well as the steady state requirement of (3) with $\dot{V}_c$ set to zero. In this manner the capacitor voltages maintain balance during steady state operation through the power shared over the inductive couplings which are injected into each capacitor as I_k. This same 8-capacitor converter is used in the results section.

IV. METHODS OF EXPANSION TO N-LEVELS

As discussed previously, this topology can be expanded to an arbitrary N-levels. Switching cells can be stacked ad infinitum given all inductive couplings cross the output node. (3) - (11) are applicable to expansion of this topology to N-levels, however, the topological matrices of $\mathbf{T_k}$ and $\mathbf{T_u}$ need to be adjusted.

The topological matrix $\mathbf{T_u}$ represents the current that flows into each capacitor due to external currents I_i and I_o with positive notation denoting positive current into the capacitor. The number of rows is equal to the number of series capacitors in the center capacitor stack and the number of columns is equal to two. The first column represents the input current I_i into each capacitor. As the current I_i will flow into all capacitors with the same direction, this column is simply all ones. The second column represents the current I_o into each capacitor, which flows out of capacitors exclusively below the output node and corresponds to a value of -1 for these capacitors. This paper considers the output to always be taken at the center node and the generalized form of $\mathbf{T_u}$ reflects this:

$$\mathbf{T_u} = \begin{bmatrix} 1 & 0 \\ 1 & 0 \\ \vdots & \vdots \\ 1 & 0 \\ 1 & -1 \\ \vdots & \vdots \\ 1 & -1 \\ 1 & -1 \end{bmatrix}. \tag{12}$$

The topological matrix $\mathbf{T_k}$ represents the connectivity of the inductive couplings. The number of columns is equal to the number of inductive couplings and the number of rows is equal to the number of capacitors. From top to bottom, the first column represents the inductive coupling of the of the first half-bridge, the second of the second half-bridge, and the nth of the nth half-bridge above the output node. The values in each column represent the capacitors that can share power across the column's respective inductive coupling, with a 1 denoting that power can be shared across this inductive coupling and a 0 denoting that power is not shared across this inductive coupling. For the example converters in Fig. 6 the $\mathbf{T_k}$ connectivity matrix is

$$\mathbf{T_k^A} = \begin{bmatrix} 1 & 0 & 0 \\ 1 & 0 & 0 \\ 0 & 1 & 0 \\ 0 & 1 & 0 \\ 0 & 0 & 1 \\ 0 & 0 & 1 \\ 0 & 0 & 1 \\ 0 & 0 & 1 \\ 0 & 1 & 0 \\ 0 & 1 & 0 \\ 1 & 0 & 0 \\ 1 & 0 & 0 \end{bmatrix} \mathbf{T_k^B} = \begin{bmatrix} 1 & 0 & 0 \\ 1 & 0 & 0 \\ 0 & 1 & 0 \\ 0 & 1 & 0 \\ 0 & 0 & 1 \\ 0 & 0 & 1 \\ 1 & 0 & 0 \\ 1 & 0 & 0 \\ 0 & 1 & 0 \\ 0 & 1 & 0 \\ 0 & 0 & 1 \\ 0 & 0 & 1 \end{bmatrix} \mathbf{T_k^C} = \begin{bmatrix} 1 & 0 & 0 \\ 1 & 0 & 0 \\ 0 & 1 & 0 \\ 0 & 1 & 0 \\ 0 & 0 & 1 \\ 0 & 0 & 1 \\ 0 & 0 & 1 \\ 0 & 0 & 1 \\ 1 & 0 & 0 \\ 1 & 0 & 0 \\ 0 & 1 & 0 \\ 0 & 1 & 0 \end{bmatrix}. \tag{13}$$

where $\mathbf{T_k^A}$ corresponds to Fig. 6-(a), $\mathbf{T_k^B}$ to Fig. 6-(b), and $\mathbf{T_k^C}$ to Fig. 6-(c). The general form of $\mathbf{T_k}$ is

$$\mathbf{T_k} = \begin{bmatrix} 1 & 0 & \dots & 0 \\ 1 & 0 & \dots & 0 \\ 0 & 1 & \dots & 0 \\ 0 & 1 & \dots & 0 \\ \vdots & \vdots & \dots & \vdots \\ 0 & 0 & \dots & 1 \\ 0 & 0 & \dots & 1 \\ 0 & 0 & \dots & 1 \\ 0 & 0 & \dots & 1 \\ \vdots & \vdots & \dots & \vdots \\ 0 & 1 & \dots & 0 \\ 0 & 1 & \dots & 0 \\ 1 & 0 & \dots & 0 \\ 1 & 0 & \dots & 0 \end{bmatrix} \tag{14}$$

as it relates to the connectivity scheme used in Fig. 6-(a). Other connectivity schemes will have different generalized forms of $\mathbf{T_k}$, however, the methodology remains constant.

Finally, the equation for for $\dot{V}_c$ in (3) can be applied to the general N-level converter with $\dot{V}_c = [\frac{dV_{C1}(t)}{dt}, \frac{dV_{C2}(t)}{dt}, \dots \frac{dV_{CN}(t)}{dt}]'$, $\mathbf{C} = \text{diag}[C_1, C_2, \dots C_N]'$, and $I_k = [I_{k1}, I_{k2}, \dots I_{kn}]'$. The constraint of (5) also persists with $\mathbf{V} = \text{diag}[V_{C1}, V_{C2}, \dots V_{CN}]'$.

Given these methods of expansion, and using a similar analysis setup as the previous section with ideal voltage splitting across the capacitors, it can be seen that the power that needs to be transferred across the inductive couplings and into each capacitor scales linearly with voltage. For a given input/output voltage, the total power transferred over all inductive couplings is constant regardless of number of levels. Furthermore, sum of voltage and current stresses of all switching devices is constant for a given input/output voltage and does not change with the number of levels. In this way, linear component stress scaling with N is achieved.

V. RESULTS

The circuits of Fig. 5-(a) and Fig. 5-(b) are used in simulation to validate both the topology (Fig. 5-(a)) and the simplified current source model (Fig. 5-(b)).

An input voltage V_i of 800V is used for all simulations involving the simplified current source model. Figs. 7, 8, and 9 show the simplified model of Fig. 5-(b) operating in steady state with a constant output current $I_o = 5$A while the output voltage is swept from 0V $< V_o < V_i = 800$V. Ideal voltage splitting is implemented and can be seen in Fig. 7.

The I_k currents can be seen in Fig. 9. As discussed in the analysis section, all of the inductive coupling current sources I_k above the output node are equal and all the I_k sources below the output node are equal. The power transferred through each inductive coupling ($P_{LA,B}$) as well as the power of each inductive coupling source ($Pk1 - 8$) can be seen in Fig. 8. The internal power flows associated with I_{k1-8} sum to zero over the entirety of the voltage sweep, satisfying the constraint of (5). The power transferred over both inductive couplings
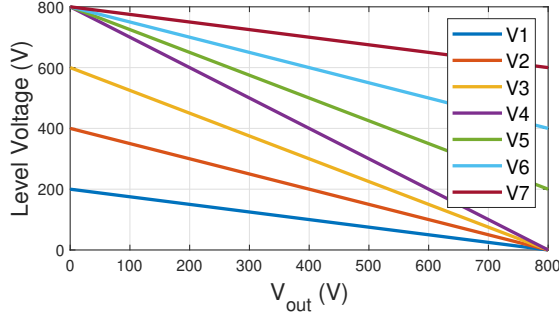
Fig. 7. Level voltages achieved during the sweep of output voltage.
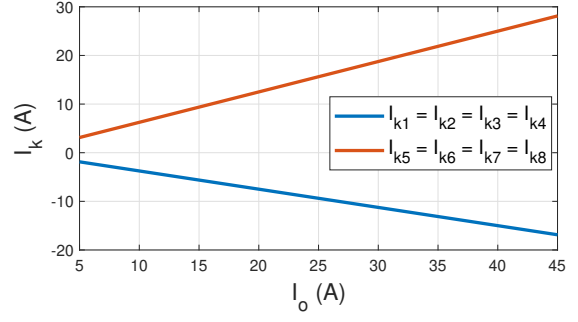

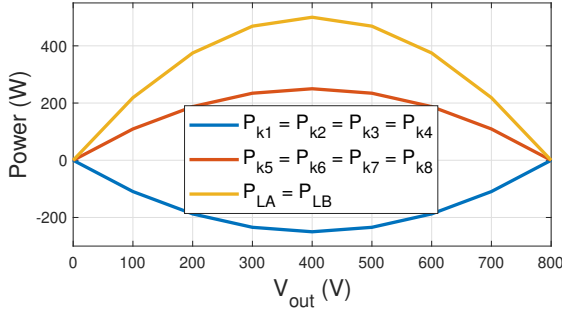Fig. 10. Coupling currents during the sweep of output current.

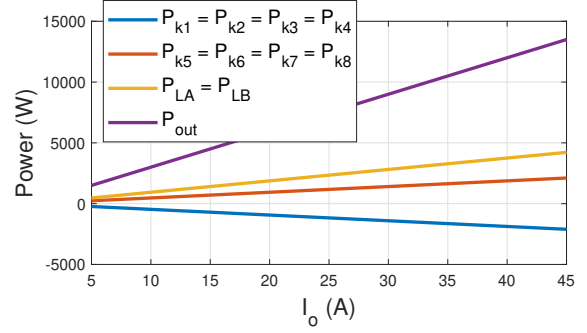Fig. 8. Power flows within the converting during the sweep of output voltage.

Fig. 11. Power flows within the converting during the sweep of output current.
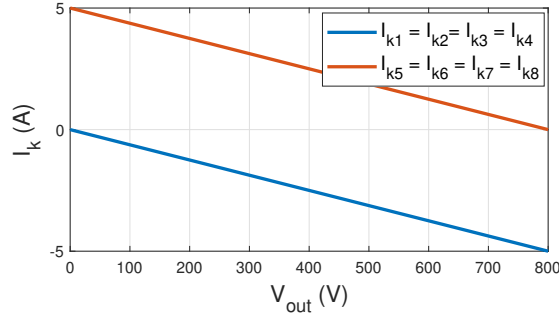

Fig. 9. Coupling currents during the sweep of output voltage.

P_{LA} and P_{LB} are equal and peak at 500W each for a 2kW output power at $V_o = 400$V (a conversion ratio of $\frac{1}{2}$).

Figs. 10 and 11 show the simplified model of Fig. 5-(b) operating in steady state with a constant output voltage $V_o = 300$V while the output current I_o is swept from $5A < I_o < 45A$. It can be seen that the the current and powers of the I_k sources remain proportional to the output power of the converter over the entirety of the output current I_o sweep.

Lastly, a high-fidelity transient simulation of the full circuit in Fig. 5-(a) was performed with capacitance values of $C_{1-8} = 24\mu$F, $L = 2.5\mu$H, a coupled inductor turns ratio of $n = 1$, switching frequency $f_{sw} = 200$kHz, and input voltage $V_i = 400$V. The duty cycle of each half bridge is held constant at 0.5. A resistive load of 100Ω is placed at the output. A rudimentary PI controller is implemented to set the

phase difference ϕ between the half-bridges of each DAHB unit cell to achieve a reference output voltage. As the phase difference ϕ controls the amount of power transferred over the inductive coupling, the PI controller can be considered as controlling P_{LA} and P_{LB} and therefore I_{k-8}.

Fig. 12 shows the voltages of each level for a range of output voltages. Fig. 13 shows the value of ϕ for each of the cells needed to achieve the desired output voltage. From a steady state perspective the level voltages are constant. Ideal voltage splitting is achieved. As ϕ is linearly related to the power transferred across the inductive coupling, the trend in ϕ as the output voltage increases (and therefore the output power increases as well) matches the predicted analytical results derived from the simplified current source model.

VI. CONCLUSION

The topology presented in this paper shows the that the reconfiguration and stacking of DAHB switching cells can be used to create a multilevel topology. A single cell can be stacked vertically, without any extra topological connections to create a multilevel converter. Multiple DAHB switching cells can be stacked to create a multilevel converter of N-levels. Voltage balance can be maintained during steady state, lending this topology to both DC/DC and AC/DC operation. Component quantities, component stresses, and circuit complexity scale linearly, which lends this topology to an easily expandable and adaptable dynamic multilevel environment. Further work regarding this topology involves construction of
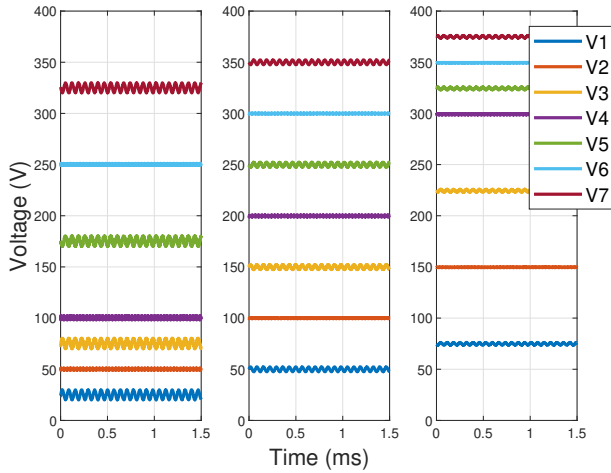
Fig. 12. Transient simulation of level voltages for 9-level converter. Left: $V_{out} = 0.25V_{in}$. Middle: $V_{out} = 0.5V_{in}$. Right: $V_{out} = 0.75V_{in}$.
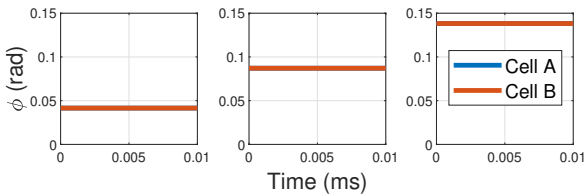

Fig. 13. DAHB phase difference ϕ during transient simulation of 9-level converter. Left: $V_{out} = 0.25V_{in}$. Middle: $V_{out} = 0.5V_{in}$. Right: $V_{out} = 0.75V_{in}$.

a physical experimental setup of the proposed circuits, evaluating the performance when the output is taken at a non-centered node or multiple nodes simultaneously, and examining the feasibility of coupling multiple inductors together.

REFERENCES

[1] L. Michi, G. Donnini, P. Capurso, A. Caldarulo Bugliari, F. Falorni, M. Quadrio, D. Canever, and L. Giorgi. An overview of the hvdc transmission system models in planning tools: the italian experience. In *2019 AEIT HVDC International Conference (AEIT HVDC)*, pages 1–6, 2019.

[2] L. Michi, G. Donnini, C. Giordano, F. Scavo, E.G. Luciano, B. Aluisio, Ch. Vergine, M. Pompili, S. Lauria, L. Calcara, and A. L'Abbate. New hvdc technology in pan-european power system planning. In *2019 AEIT HVDC International Conference (AEIT HVDC)*, pages 1–6, 2019.

[3] Iqbal Husain, Burak Ozpineci, Md Sariful Islam, Emre Gurpinar, Gui-Jia Su, Wensong Yu, Shajjad Chowdhury, Lincoln Xue, Dhrubo Rahman, and Raj Sahu. Electric drive technology trends, challenges, and opportunities for future electric vehicles. *Proceedings of the IEEE*, 109(6):1039–1059, 2021.

[4] B. Powell, K. Matocha, S. Chowdhury, K. Rangaswamy, C. Hundley, and L. Gant. Performance and reliability of 1200v sic planar mosfets fabricated on 150mm sic substrates. In *2016 IEEE 4th Workshop on Wide Bandgap Power Devices and Applications (WiPDA)*, pages 158–161, 2016.

[5] Eugen Wiesner, Koichi Masuda, and Motonobu Joko. New 1200v full sic module with 800a rated current. In *2015 17th European Conference on Power Electronics and Applications (EPE'15 ECCE-Europe)*, pages 1–9, 2015.

[6] Oskar Josefsson, Torbjörn Thiringer, Sonja Lundmark, and Hector Zelaya. Evaluation and comparison of a two-level and a multilevel inverter for an ev using a modulized battery topology. In *IECON 2012 -*

[7] L.M. Tolbert, Fang Zheng Peng, and T.G. Habetler. Multilevel converters for large electric drives. *IEEE Transactions on Industry Applications*, 35(1):36–44, 1999.

[8] Alireza Nami, Jiaqi Liang, Frans Dijkhuizen, and Georgios D. Demetriades. Modular multilevel converters for hvdc applications: Review on converter cells and functionalities. *IEEE Transactions on Power Electronics*, 30(1):18–36, 2015.

[9] M.R. Pavan Kumar and J.M.S. Kim. A hybrid multi-level switching converter for ring-magnet power supplies. *IEEE Transactions on Nuclear Science*, 43(3):1876–1883, 1996.

[10] Jih-Sheng Lai and Fang Zheng Peng. Multilevel converters-a new breed of power converters. *IEEE Transactions on Industry Applications*, 32(3):509–517, 1996.

[11] Fang Zheng Peng. A generalized multilevel inverter topology with self voltage balancing. *IEEE Transactions on Industry Applications*, 37(2):611–618, 2001.

[12] Matthew Jahnes, Bernard Steyaert, and Matthias Preindl. A balanced and vertically stacked multilevel power converter topology with linear component scaling. In *IECON 2021 – 47th Annual Conference of the IEEE Industrial Electronics Society*, pages 1–6, 2021.

[13] Heng Yang, Maryam Saeedifard, and Amirnaser Yazdani. An enhanced closed-loop control strategy with capacitor voltage elevation for the dc–dc modular multilevel converter. *IEEE Transactions on Industrial Electronics*, 66(3):2366–2375, 2019.

[14] Jianpo Zhang, Chuan Jiang, and Chongchong Chen. Research of control strategies of mmc based on full bridge sub-modules. *The Journal of Engineering*, 2019, 10 2018.

[15] A. Narendrababu and Pramod Agarwal. A five level diode clamped rectifier with novel capacitor voltage balancing scheme. In *2014 IEEE International Conference on Power Electronics, Drives and Energy Systems (PEDES)*, pages 1–6, 2014.

[16] Neha Beniwal, Josep Pou, Christopher D. Townsend, and Salvador Ceballos. Enhancing the natural voltage balancing capability of neutral-point-clamped converters under carrier-based pulsewidth modulation. In *2018 IEEE 4th Southern Power Electronics Conference (SPEC)*, pages 1–6, 2018.

[17] Xiaoming Yuan, H. Stemmler, and I. Barbi. Self-balancing of the clamping-capacitor-voltages in the multilevel capacitor-clamping-inverter under sub-harmonic pwm modulation. *IEEE Transactions on Power Electronics*, 16(2):256–263, 2001.

[18] Kia Filsoof and Peter W. Lehn. A bidirectional modular multilevel dc–dc converter of triangular structure. *IEEE Transactions on Power Electronics*, 30(1):54–64, 2015.

[19] Matthias Kasper, Dominik Bortis, and Johann W. Kolar. Novel high voltage conversion ratio "rainstick" dc/dc converters. In *2013 IEEE Energy Conversion Congress and Exposition*, pages 789–796, 2013.

[20] G. Tibola, J. L. Duarte, and A. Blinov. Floating high step-down stacked dc-dc converter based on buck-boost cells. In *2015 17th European Conference on Power Electronics and Applications (EPE'15 ECCE-Europe)*, pages 1–10, 2015.

[21] Fahad Alhuwaishel, Ahmad Allehyani, Sinan Al-Obaidi, and Prasad Enjeti. A new medium voltage dc collection grid for large scale pv power plants with sic devices. In *2018 IEEE 19th Workshop on Control and Modeling for Power Electronics (COMPEL)*, pages 1–8, 2018.

[22] Ahmed Morsy, Yong Zhou, and Prasad Enjeti. A new high power density modular multilevel dc-dc converter with localized voltage balancing control for arbitrary number of levels. In *2016 IEEE Applied Power Electronics Conference and Exposition (APEC)*, pages 2567–2572, 2016.

[23] Ahmed Allehyani and Prasad Enjeti. A new modular micro-inverter with sinusoidal output voltage using gan switches for pv modules. In *2018 9th IEEE International Symposium on Power Electronics for Distributed Generation Systems (PEDG)*, pages 1–6, 2018.

[24] Haixu Shi, Kai Sun, Hongfei Wu, and Yunwei Li. A unified state-space modeling method for a phase-shift controlled bidirectional dual-active half-bridge converter. *IEEE Transactions on Power Electronics*, 35(3):3254–3265, 2020.

[25] Fei Gao, Ngoni Mugwisi, and Daniel J. Rogers. Average modeling of a dual-half-bridge converter modulated with three degrees of freedom. *IEEE Transactions on Transportation Electrification*, 7(3):1016–1030, 2021.