A Software-Defined Stacked Multilevel Motor Drive Inverter with Linear Component Scaling

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***Abstract*—This research proposes a software-defined multilevel inverter topology for use in motor drives. Each cell consists of elementary power conversion modules that consist of power FETs, filtering, and local control. They are aggregated by software to form a multilevel topology demonstrating a simplified construction of a larger converter from component cells. A 5-Cell converter is simulated to validate the design, and the resulting voltage and current waveforms are shown. Dynamic modelling of the converter is also discussed. [1] demonstrated that high-performance module-level controls enable stacked converters and mitigate resonances. The simulated 2.5 kW, 5-level motor drive has 300 Hz torque control bandwidth. The modular stacked design provides dynamic voltage sharing. This allows commonly available fast, low on resistance switches to be used.**

I. Introduction

There are many applications for inverters at higher voltage levels. Traction motor drives for electric vehicles are a common example. Increasing the operating voltage reduces the driving current and the associated copper volume and weight of interconnects. This issues is even more pronounced for electric airplanes, which are highly weight-sensitive. This paper proposes an inverter topology consisting of a series stack of modular cells. The cells can use fast, efficient lower voltage switches, and the cells can be stacked to support larger voltages. This improves overall efficiency while reducing cost [2], [3], [4]. This topology is shown to be effective as a three-phase motor inverter. It differs from other uses of stacked converters [5]–[11] in that there is local feedback around each stage, avoiding unwanted resonances and simplifying the design process.

Modern traction motor drives tend to increase the voltage levels achieve high powers, high efficiency, and power density with reduced cabling requirements. However, high-voltage switching devices tend to have increased on-resistance and high switching losses. Additionally, directly switching high voltage can generate significant conducted and radiated EMI. Multilevel typologies are often used to distribute voltage stress over many low voltage components. This allows the use devices with better properties, and avoids many of the EMI issues associated with direct switching.

The primary trade-offs in multilevel architectures are a higher component count, and increased control complexity. Different multilevel architectures have different characteristics, particularly relating to scaling the number of stages. The topology presented here has linear component count scaling

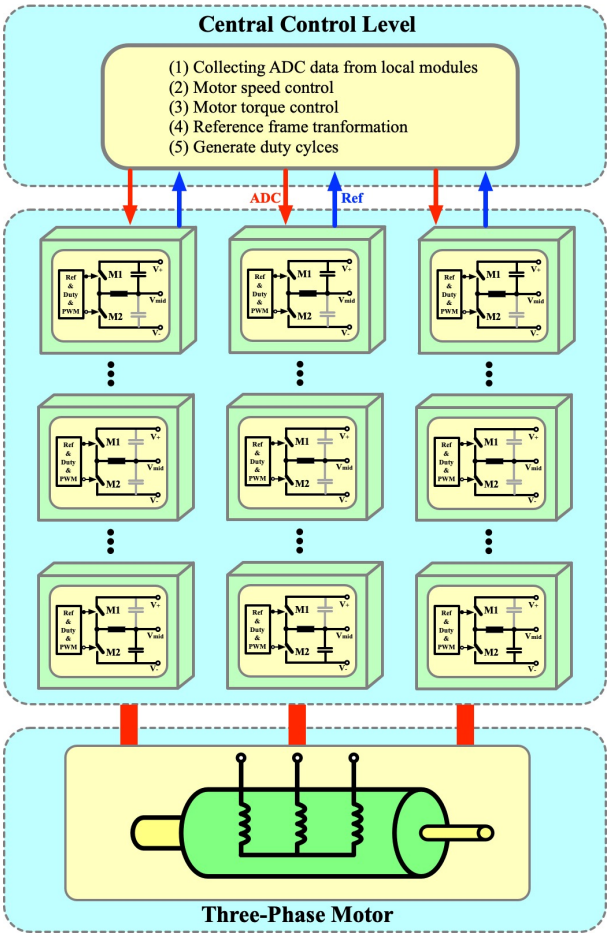


Fig. 1: Software-defined stacked control architecture for motor application

and full control over all voltages down to DC. The main disadvantage is large inductor currents close to the center of the stack.

In this paper, we present a methodology for constructing a stacked, high voltage inverter from a series of sub-converters called cells. Each cell has local feedback to define its input/output behavior and damp internal resonances. The full converter is then simple to constructed and modeled at the cell level.

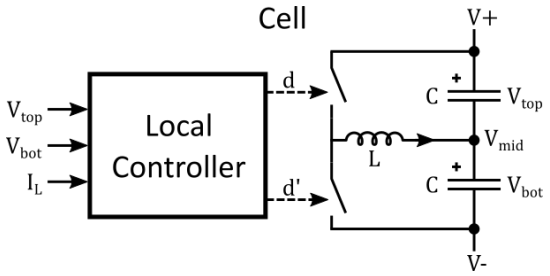


Fig. 2: Single cell with local feedback

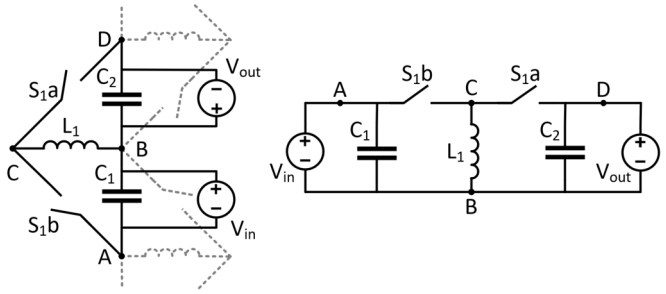


Fig. 3: Stackable unit cell as it relates to the inverting buck-boost converter (dashed lines show connections of adjacent cells).

II. Topology Description

The generalized topology of the converter used in this paper can be seen in Fig. 4, where where N and K represent the number of levels and number of stackable unit cells, respectively, and $N = K + 2$. The output is taken exclusively at the center node, which is defined as having the same number of series capacitors above it as below it. This topology is unique in that it can be expanded to an arbitrary N levels with component quantities scaling linearly. This is achieved through individually stackable and controllable unit cells, which can be seen in figures 2 and 3.

The stacked cell nature of this topology eliminates the need for a bulk capacitance between the input and reference or between the output and reference. The series combination of the cell capacitances serves to support both the input and output nodes as well as the voltages within each cell. The individual capacitor voltages can be controlled as a function of the duty cycles of each unit cell, allowing for the voltage across the entire stack to be balanced across the cells arbitrarily. This enables the control and conversion of voltages higher than the voltage rating of any individual semiconductor or passive component. The output voltage is the sum of the capacitor voltages between the output node and reference. The ability to balance the capacitor voltages to any ratio allows rail-to-rail output.

Governing equations, DC analysis, detailed topology description, and performance results of this topology can be found in [12].

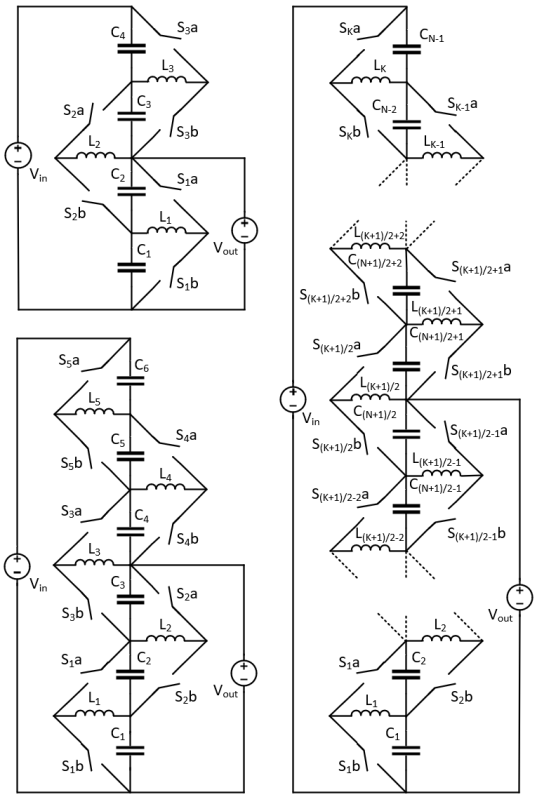


Fig. 4: Manhattan Topology. Upper left: 3 Cells, 5 Levels. Bottom left: 5 Cells, 7 Levels. Right: Generalized topology for K cells and N levels.

A. Stackable Concept

For the inverter application, a stackable concept is used for the motor controller as is shown in Fig. 1. The central controller is configured with several functions to manage the power modules. First, the ADC samples voltages and currents from the local modules. Second, the motor speed and torque are controlled in the dq reference frame by Park/Clarke transformations. Third, the generated references are distributed to the local power modules for duty cycle controlled PWM. This causes each stack to act as a single, unified inverter leg.

III. Stacked Topology as an Inverter

The proposed system uses the stacked topology (Fig. 4) as an inverter. The centered output can swing from rail to rail while maintaining evenly distributed voltage stresses above and below. This voltage sharing allows the use of switches with lower voltage rating, as each must support only a fraction of the input voltage. MOSFET conduction loss grows faster than linearly with blocking voltage [13] (and switching speed reduces), so overall conduction loss can be reduced by sharing voltage between several low-voltage switches rather than using a single high-voltage switch. For high-current applications, the lower device rating can allow the use of Silicon or Silicon Carbide MOSFETs, rather than IGBTs. IGBTs can have very low conduction loss at higher blocking voltage, but suffer

from large turn-off "tail current" loss due to slow carrier recombination.

A. Generating Sinusoidal Output

In an inverter application, the stack output must be controlled to follow a sinusoidal voltage or current reference. This reference comes from a top-level stack controller (Fig. 8). The stack controller measures the inverter output and any other desired variables (such as angle and speed for a motor drive), and computes a reference input for the stack.

The reference directly controls only the center (output) cell. The other cells are set to maintain a 1:1 voltage ratio between their top and bottom capacitors. Modulating the center stage reference trades voltage between the middle two capacitors. These voltage changes then propagate up and down the stack as the other cells enforce the 1:1 ratio. The cells adjacent to the middle cell mirror its voltages, and then the next cells, until all cells mirror the center cell. This ensures that all the capacitors above the output share the same voltage, as do all those below the output. The overall conversion ratio of the stack therefore matches the conversion ratio of the center cell. The fast local feedback loops and capacitive energy storage on each cell ensure that voltage balancing is maintained through transients. This allows the stacked low voltage devices to safely share the bus voltage.

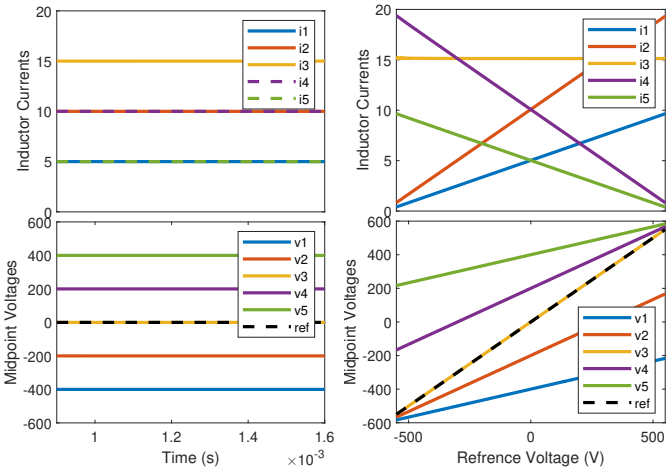
B. Cell Waveforms

The converter was simulated under various conditions in order to validate the topology. The parameters used for simulation are $V_{DC} = 1200V, L = 7.1\mu H$, and $C = 2.5\mu F$. As the exact inductor current waveforms intentionally contain large ripple, a switching-cycle averaged model was used to show the underlying behavior. As shown in [12], cell inductor currents are not equal in steady state, with those closer to the center carrying more current. Additionally, all inductors carry more than the output current. For example, in a 5-cell converter in steady state with centered output, the middle cell inductor current is 3x the output current. Here, the dynamic behavior of the inductor currents is investigated. Figure 5a shows the steady-state behavior of a 5-cell stack with the output centered and a 5 A load. The cell voltages evenly divide the 1,200 V bus voltage. The inductor currents are all greater than 5 A, with the current decreasing away from the center cell. Cells above or below the center by the same distance carry the same current.

Figure 5b shows the steady-state inductor currents and cell midpoint voltages of the 5-Cell stack as the output is swept from the negative to the positive rail with a 5 A load current. The voltages behave as expected. In the center of the figure, they are evenly distributed around zero, matching figure 5a. At the extremes, the voltage is evenly across each half of the stack, though the halves support different voltages. At all points, cells on the same side of the midpoint share the same voltage stress.

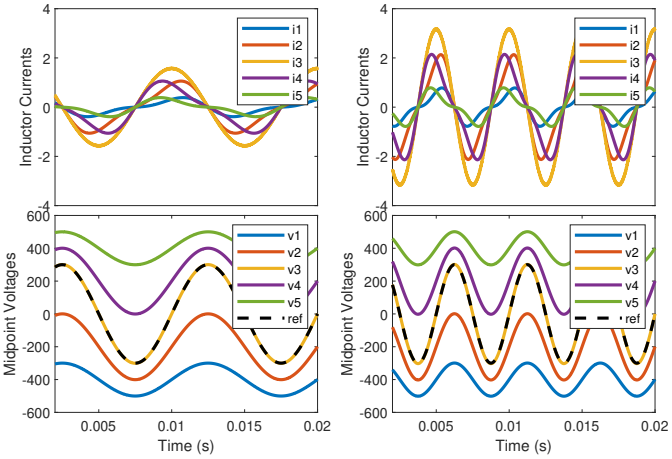
Figure 7a shows the cell voltages and inductor currents driving an inductive load with a 100 Hz sinusoid. The inductor currents are now the sum of two components. The first is the currents supporting the load, which match the DC case. Second, the inductors must move charge between the capacitors in the stack in order to change the capacitor voltages. This requires an additional current component, which is superimposed on the DC component when the output voltage is changing. These capacitor charge transfer currents can be seen in isolation in figure 6, where there is no load on the converter and thus no DC component, only the charge transfer required to generate the sinusoid at 100 or 200 Hz. As the capacitor voltages change is defined by $I_c = C\frac{dV_c}{dt}$, these currents are proportional to output frequency (as seen in figure 6), and disappear at DC.

Figure 7b shows the step response of the inductor currents and cell voltages in an averaged switch model. The step in output voltage is from -200 to +200 V. The center stage (which is directly controlled) responds immediately, while the



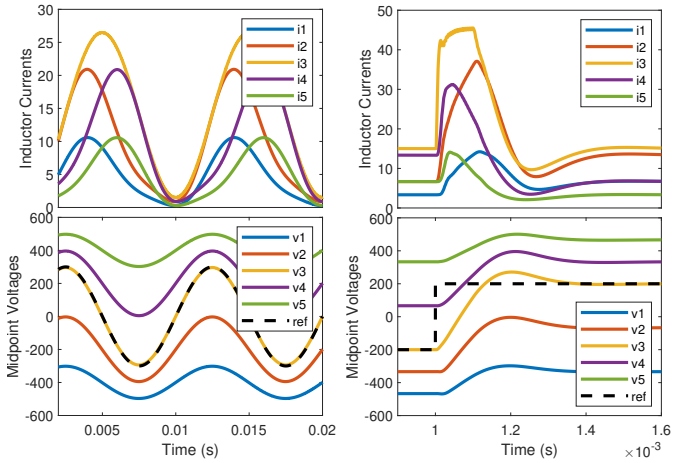
(a) Steady-state centered output (b) DC sweep of output voltage

Fig. 5: Averaged DC behavior of cell currents and voltages with 5 A load.



(a) 100 Hz (b) 200 Hz

Fig. 6: Circulating currents increase with frequency.



(a) 100 mH load (b) 400 V step input, 5 A load

Fig. 7: Loaded dynamic behavior.

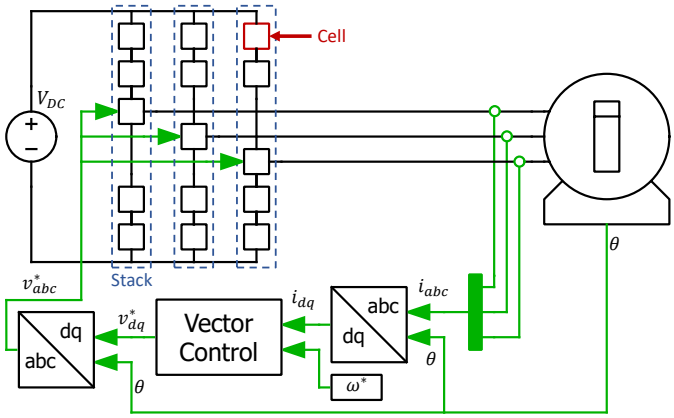


Fig. 8: Motor controller configuration

responses are increasingly delayed in cells moving away from the center. Currents and voltages are well damped and exhibit minimal ringing. This demonstrates that the converter is stable even with aggressive setpoint variation.

C. Alternate Control to Reduce Circulating Currents

The voltage sharing scheme above is simple to implement, but is not the only option. When the output voltage is not at either extreme, the cell voltages can be unbalanced while still remaining within their voltage rating. As is shown in [12], this extra flexibility can be leveraged to reduce inductor currents and the associated loss and component size.

Taking advantage of this optimization would require a more complex control scheme. Rather than only controlling a single reference (going to the center cell), the controller would need to provide a reference to each cell. To save computation time on the controller, optimum reference values can be pre-computed offline. The controller would then store a lookup table mapping the desired conversion ratio to the set of optimized cell voltage ratios.

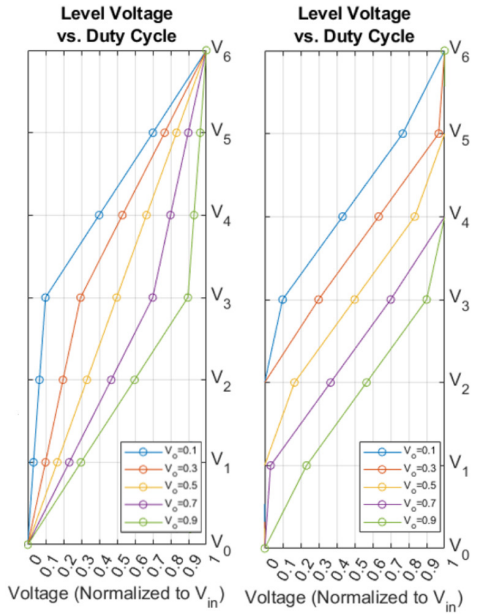


Fig. 9: Simple (left) and total current optimized (right) stack voltage distributions.

IV. Dynamic Converter Modelling

A. Controlling the Cells

Each cell has a local feedback loop. This provides high-bandwidth control of each capacitor voltage, as shown in Fig. 2. The cell-level controller is given a reference, which sets the desired ratio between the top and bottom port voltages. Each cell has a second-order response, and can be controlled with an inner inductor current loop and outer voltage loop, or with more advanced control techniques such as Model Predictive Control (MPC).

While the system could in theory be operated without local controllers by setting all off-center cell duty cycles to 50%, this would result in undesirable behavior. The balancing of the cell voltages would hold in steady state, but the dynamic response would be poor, significantly limiting overall bandwidth. As each unit cell contains an inductor and capacitor, if the cells were operated open loop, these components would be prone to resonating, leading to instability. Passively damping this resonance would result in unacceptable restive loss and low bandwidth. These issues are avoided by the cell controllers, which actively damp the resonance while improving dynamic response time. This requires fast switching, so the control bandwidth can be sufficiently above the resonant frequency of the cell.

The local feedback decouples the cells from each other. This significantly simplifies control of the stack. The number of cells in the stack can be scaled without significant changes to the design of the cell-level or top-level controllers. This allows design reuse between inverters of different voltage requirements and economies of scale for making the unit cells.

B. Dynamic Modelling

To design a high-performance compensator to control the output of the inverter, it is useful to first construct a dynamic model of the stack. This is done by first describing the cell input/output behavior, then building the stack model from the cell models. As the cells each have their own local feedback control, it is the closed-loop cell transfer functions that are of interest. The local feedback loops make the individual cells well behaved, allowing the closed-loop behavior to be approximately described by simplified models. This simplifies the modeling of the stack dynamics significantly. This also allows abstraction of the details of the cell controller. Substitution of one cell control scheme for another should only affect parameter values of the simplified cell model, but not change its structure.

The construction of the dynamic model starts with the center cell, as it is the only stage which is directly controlled by the top-level controller. The center cell has its input and output port loaded by the impedance of the rest of the stack. It will therefore be necessary to find this impedance. Once it is known, a transfer function can be constructed to model the reference-to-V_{bot} behavior of the center stage (and the complementary reference-to-V_{top} as well).

C. Stack Transfer Functions

A transfer function for the stack can be constructed from two cell transfer functions. The first is $G_r(s)$, the reference-to-bottom voltage of the center cell. The 2^{nd} is $G_v(s)$, the top to bottom voltage transfer function of an off-center cell.

$$G_r(s) = \frac{v_{bot}}{v_{top}}, G_v(s) = \frac{v_{bot}}{v_{ref}} \tag{1}$$

The exact expressions for these transfer functions depend both on the specific implementation of the local cell feedback, and on the impedance loading each port. However, as each cell is a 2^{nd} order converter, if it is assumed that the local controller is well designed (high bandwidth with damped resonances), both transfer functions can be approximated in the following form. Q is the quality factor, which will be small for a well designed cell. ω_{BW} is the closed-loop bandwidth of the cell in rad/s.

$$G(s) = \frac{1}{\left(1 + \frac{s}{Q\omega_{BW}} + \frac{s^2}{\omega_{BW}^2}\right)} \tag{2}$$

The overall converter transfer function is then built from the cell transfer functions. $G_r(s)$ defines the lower port voltage of the middle cell, $v_3(s)$ in figure 10. This is then the input the the next cell down, which has its bottom voltage defined by $G_v(s)$. Therefore, in figure 10, $v_2(s) = G_v(v_3)$. This process continues until the bottom of the stack is reached. After simplifying, for a cell n cells below the center, the bottom voltage $v_n(s)$ is:

$$v_n(s) = G_v^n G_r v_{ref} \tag{3}$$

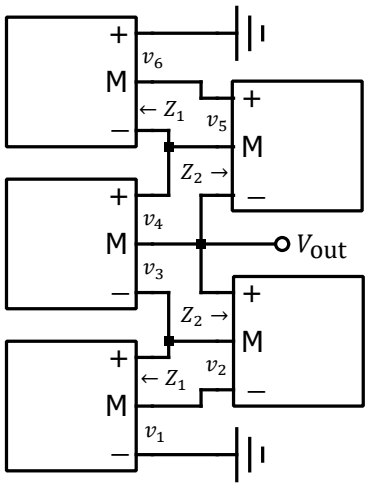


Fig. 10: 5-Cell stack with port impedances and voltages labeled.

Finally, the output voltage is found by summing the port voltages from ground:

$$v_{out} = v_1 + v_2 + ... + v_{n/2} \tag{4}$$

Plugging equation 3 into equation 4 and simplifying gives:

$$\frac{v_{out}}{v_{ref}} = G_r \left(G_v^n + G_v^{(n-1)} + ... + G_v + 1\right) \tag{5}$$

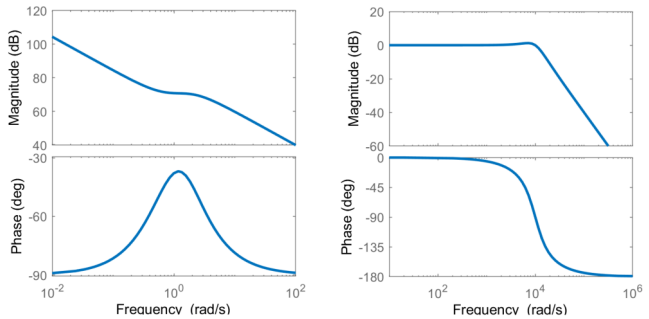
D. Stack Impedances

The impedances in the stack can also be approximated with a simple model by assuming that the local cell controllers are well designed, with high bandwidth and damped resonance. Consider a cell with no loading impedance other than the two internal capacitors. At low frequency, the cell feedback forces the two port voltages to match. Looking into the top port, the two capacitors appear in parallel as any change to the top capacitor voltage is mirrored on the bottom capacitor. Thus, the low-frequency asymptote of the impedance is a capacitor of value $2C$. This models the cells at the top and bottom of the stack. As the cell is well regulated, the transition between these asymptotic is smooth and occurs at the cell closed-loop bandwidth, where it appears approximately as a zero-pole pair. This gives a model of the input impedance of the top and bottom cells:

$$Z_{in,end} = \frac{1}{s2C} \parallel \left(1 + \frac{s}{\omega_{BW}}\right) \tag{6}$$

The same argument extends to include any loading impedance Z_{load} connected to the bottom port, in which case the input impedance is $2C$ in parallel with Z_{load}. This leads to the approximate impedance:

$$Z_{in} = \left[\left(\frac{1}{sC} \parallel Z_{load}\right)\left(1 + \frac{s}{\omega_{BW}}\right)\right] \parallel \left(1 + \frac{s}{\omega_{BW}}\right) \tag{7}$$



(a) Impedance (b) Voltage Transfer Function

Fig. 11: Cell approximate impedance and transfer function.

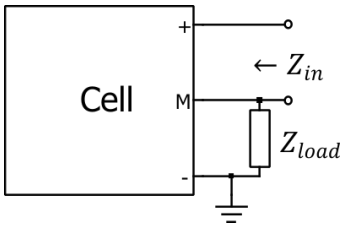


Fig. 12: Input and loading impedance of a below-center cell.

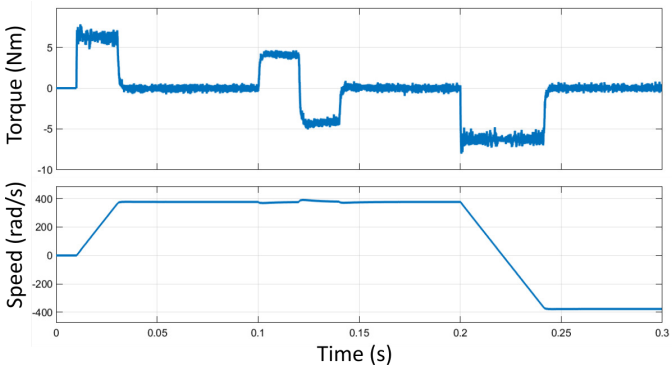


Fig. 13: Motor torque and speed while following a test profile

The next step is to solve for the input impedance of the half-stacks (which load the center cell). The bottom cell has impedance Z_1, calculated in equation 6. The next cell up has impedance Z_2, calculated using equation 7, where $Z_{load} = Z_1$. This pattern is repeated until the center cell is reached. By symmetry, cells of equal distance from the center have the same input impedance, so there is no need to separately calculate the impedances in the top half of the stack.

V. Behavior as Motor Drive

A simulation has been constructed to demonstrate the topology's use as a motor drive. Three copies of the 3-cell topology and a top-level controller are modelled. The setup is shown in Fig. 8. The system tracks a speed profile ω_{ref} and responds to bidirectional torque disturbances, as shown in Fig. 13. The topology successfully produces the required waveforms, and the motor tracks the speed profile while rejecting the torque disturbances.

VI. Conclusion

In this research we show a buck-boost derived stacked cell topology that can be controlled to produce a time-varying output voltage that tracks a reference. The output variation can be as large as the input voltage. The stack height can be scaled to support high operating voltage, though circulating currents limit stack size to roughly seven cells. These properties make this topology of interest for applications such as grid-connected inverters and high-voltage motor drives. Operation of the topology as a three-phase motor drive is shown.

References

[1] L. Zhou, M. Jahnes, M. Eull, W. Wang, and M. Preindl, "Control Design of a 99% Efficiency Transformerless EV Charger Providing Standardized Grid Services," *IEEE Transactions on Power Electronics*, vol. 37, no. 4, pp. 4022–4038, Apr. 2022, conference Name: IEEE Transactions on Power Electronics.

[2] F. Chang, O. Ilina, M. Lienkamp, and L. Voss, "Improving the Overall Efficiency of Automotive Inverters Using a Multilevel Converter Composed of Low Voltage Si mosfets," *IEEE Transactions on Power Electronics*, vol. 34, no. 4, pp. 3586–3602, Apr. 2019, conference Name: IEEE Transactions on Power Electronics.

[3] O. Josefsson, T. Thiringer, S. Lundmark, and H. Zelaya, "Evaluation and comparison of a two-level and a multilevel inverter for an EV using a modulized battery topology," in *IECON 2012 - 38th Annual Conference on IEEE Industrial Electronics Society*, Oct. 2012, pp. 2949–2956, iSSN: 1553-572X.

[4] L. Tolbert, F. Z. Peng, and T. Habetler, "Multilevel converters for large electric drives," *IEEE Transactions on Industry Applications*, vol. 35, no. 1, pp. 36–44, Jan. 1999, conference Name: IEEE Transactions on Industry Applications.

[5] K. Filsoof and P. W. Lehn, "Design and control of a bidirectional triangular modular multilevel DC-DC converter," in *2013 IEEE 14th Workshop on Control and Modeling for Power Electronics (COMPEL)*, Jun. 2013, pp. 1–7, iSSN: 1093-5142.

[6] M. Kasper, D. Bortis, and J. W. Kolar, "Novel high voltage conversion ratio "Rainstick" DC/DC converters," in *2013 IEEE Energy Conversion Congress and Exposition*, Sep. 2013, pp. 789–796, iSSN: 2329-3748.

[7] G. Tibola, J. L. Duarte, and A. Blinov, "Floating high step-down stacked dc-dc converter based on buck-boost cells," in *2015 17th European Conference on Power Electronics and Applications (EPE'15 ECCE-Europe)*, Sep. 2015, pp. 1–10.

[8] A. Allehyani, A. Morsy, and P. Enjeti, "A new Interconnected Modular Multilevel Converter (IMMC) with sinusoidal voltage output suitable for high performance AC drives," in *2017 IEEE 18th Workshop on Control and Modeling for Power Electronics (COMPEL)*, Jul. 2017, pp. 1–8.

[9] F. Alhuwaishel, A. Allehyani, S. Al-Obaidi, and P. Enjeti, "A New Medium Voltage DC Collection Grid for Large Scale PV Power Plants with SiC Devices," in *2018 IEEE 19th Workshop on Control and Modeling for Power Electronics (COMPEL)*, Jun. 2018, pp. 1–8.

[10] A. Morsy, Y. Zhou, and P. Enjeti, "A new high power density modular multilevel DC-DC converter with localized voltage balancing control for arbitrary number of levels," in *2016 IEEE Applied Power Electronics Conference and Exposition (APEC)*, Mar. 2016, pp. 2567–2572.

[11] A. Allehyani and P. Enjeti, "A New Modular Micro-inverter with Sinusoidal Output Voltage Using GaN Switches for PV Modules," in *2018 9th IEEE International Symposium on Power Electronics for Distributed Generation Systems (PEDG)*, Jun. 2018, pp. 1–6, iSSN: 2329-5767.

[12] M. Jahnes, B. Steyaert, and M. Preindl, "A Balanced and Vertically Stacked Multilevel Power Converter Topology with Linear Component Scaling," in *IECON 2021 – 47th Annual Conference of the IEEE Industrial Electronics Society*, Oct. 2021, pp. 1–6, iSSN: 2577-1647.

[13] L. F. S. Alves, P. Lefranc, P.-O. Jeannin, and B. Sarrazin, "Review on SiC-MOSFET devices and associated gate drivers," in *2018 IEEE International Conference on Industrial Technology (ICIT)*, Feb. 2018, pp. 824–829.