A Single-or-Three-Phase Adaptable Inverter Enabled by Second Harmonic Injection

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***Abstract*—This paper provides an adaptable topology that can be used in grid-tied inverter adaptions for three-phase, single-phase, and split single-phase grids. The value of the DC-link capacitance is of high importance when using a three-phase converter in a single-phase application. If sized for the single-phase application the DC-link capacitance will be oversized for the three-phase application. Likewise, if sized for the three-phase application, the DC-link capacitance will be undersized for the single-phase application. This is because the DC-link needs to support a pulsating power flow in single-phase operation that is not present in three-phase interfaces. This paper proposes the use of Second Harmonic Injection (SHI) when operating with a single-phase grid to mitigate the pulsating power flow. SHI is enabled by the proposed topology, which allows for the required capacitance of single-phase operation to be reduced and become closer in value to the required DC-link capacitance of three-phase operation. This lessens the trade-off that must be made between single-phase operation, three-phase operation, and required DC-link capacitance, ultimately resulting in a more balanced design. Design equations are provided alongside comments on component sizing to maximally leverage SHI. Experimental three-phase, single-phase without SHI, and single-phase with SHI results are shown.**

I. Introduction

As EV penetration increases in today's market so do the need for their associated chargers. Chargers of different power and voltage levels are already well defined [1], [2] and a multitude of standards are currently in place that govern their operation [3], [4]. However, these different charger levels and types will often require a bespoke power electronics hardware design. Furthermore, different grid standards and types throughout the world will also require a bespoke design. Vehicle-to-grid (V2G), islanding, and grid forming/following inverter variations will also add to the design burden as their additions can also require topological updates.

This is a disadvantage for the both the power electronics engineer and the associated Research and Development (R&D) budgets. More effort and money than necessary will get spent designing and validating what is essentially the same product for different market segments. A better alternative would be to have a single power electronics hardware design that can be adapted for the different grid connections and market segments. This would greatly ease the R&D efforts required for introducing a new product to the worldwide market.

There are existing adaptable power converters in academia. Both [5], [6] describe isolated power converters where the secondary side can be reconfigured to maintain efficiency over varying load conditions. [7] describes a partial-power converter that can be reconfigured for more optimal step-up and step-down performance. These designs are intended for dynamic circuit reconfiguration, where the adaptability status is based off the current operating conditions.

More relevant to the proposed technology is [8], [9] where a single power converter, through a static adjustment, can be used in both single and three-phase applications. This type of adjustment is not dynamic, and is intended to be used in applications where the reconfigurable state of the converter is fixed i.e. three-phase is configured for European markets and single-phase is configured for US markets.

There are technical challenges associated with single-phase and three-phase converters sharing a single hardware design. The most prominent issue is the sizing of the DC-link capacitance, which, for comparable power levels, needs to be much larger for the single-phase design than the three-phase design. Should a typical approach be used, the sizing of the dc-link capacitance in 3-phase mode would be excessive as the DC-link capacitance would have to be sized for single-phase operation.

The proposed adaptable grid interface allows for the required sizing of this DC-link capacitance in single-phase to more closely match the required DC-link capacitance in three-phase. This is achieved through Second Harmonic Injection (SHI) [10], enabled by a connection of the star point of the grid-side filter capacitances to the negative DC link. This concept is discussed in detail in the following sections.

Through SHI, the proposed adaptable grid-tied inverter can be statically adapted to interface with any of the grid topologies (split phase, single-phase, and three-phase) with-

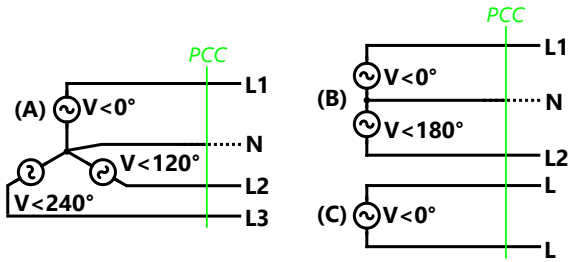

Fig. 1. Different grid topologies. (A): 3-phase, either with or without the neutral connection. (B) Split single-phase. (C): Single-phase.

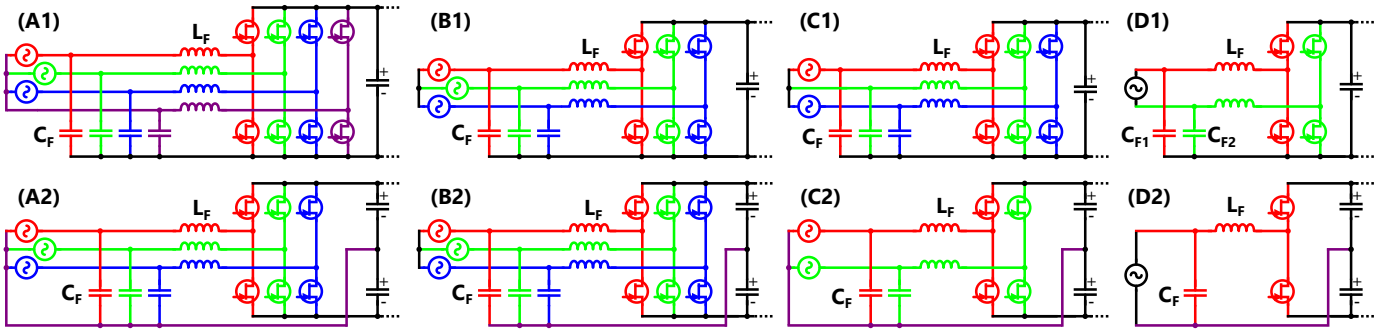

Fig. 2. Inverter types that can interface with various grid connections. (A1, B1 C1, D1): Full-bridge (Type 1) inverter topologies. (A2, B2, C2, D2): Half-bridge (Type 2) inverter topologies. (A1, A2): 3-phase 4-wire grid connection. (B1, B2): 3-phase 3-wire grid connection. (C1, C2): split single-phase grid connection. (D1, D2): single-phase grid connection.

out sacrificing performance for any of the individual grid topologies. Moreover, it is possible to create an islanding (grid-forming) connection with all grid topologies (although islanding is not specifically discussed in this paper). This allows for the proposed adaptable inverter to span all potential grid-tied inverter markets with a single design.

The proposed adaptable inverter is built around a set of power electronics hardware that can be rearranged for a variety of applications, in the scope of this paper, these applications are limited to different grid interfaces and the set of power electronics hardware is a grouping of modular phase legs.

Included in this paper is the proposed topology of the adaptable grid-tied inverter with two different types of phase legs. High-level design equations and sizing considerations are shown. Lastly, experimental results in single-phase (both with and without SHI) and three-phase configurations are provided to show the efficacy of the proposed system. Control systems design are out of the scope of this paper, but the hierarchical software defined control design can be found in [11], MPC control of the individual modules in [12], and motor drive applications in [13].

II. Background

Grid standards vary throughout the world. Frequency, voltage, and topology will change from country to country and sometimes even within the country. A table showing a comparison of different grid voltages and types can be seen in Table I. Fig. 1 shows different grid topologies.

TABLE I
Low Voltage Grids of the US and EU

Grid Voltage and type	V_{L-L}	V_{L-N}	Frequency	Region
3-phase 480V	480V	277V	60Hz	US
3-phase 400V	400V	230V	50Hz	EU
3-phase 208V	208V	120V	60Hz	US
Split 1-phase 240V	240V	120V	60Hz	US
1-phase 240V	240V	N/A	60Hz	US
1-phase 230V	230V	N/A	50Hz	EU
1-phase 120V	120V	N/A	60Hz	US

It is straightforward to adapt to voltages less than $480V_{l-l}$ as all of these voltages can be accommodated with 1200V FETs and a simple 2-level topology [14], [15]. Likewise, accommodating both 50Hz and 60Hz does not require excessive attention.

It is not straightforward, however, to accommodate multiple different grid topologies simultaneously. Three-phase and single-phase simply have different numbers of lines which each require individual power electronic elements. Grid-forming (islanding) inverters will require a neutral connection that typical grid-following converters do not necessarily have. This is because grid-forming inverters need to maintain performance with unbalanced loads and currents in the neutral can be expected. This neutral connection can be made with a split DC-link capacitance or an additional phase leg, depending on the design priorities of the application.

The following section describes the proposed topology that can be used to interface with each of the grid types, both in grid-forming and grid-following applications.

III. Topology

As described previously, the proposed topology leverages second harmonic injection (SHI) [10] to minimize the required capacitance when operating in single-phase and/or unbalanced three-phase configurations. SHI, as used in the proposed, requires control of the common-mode components of the grid. A connection is made between the negative terminal of the grid-side filter capacitors C_F back to the inverter, as done in [10], [14], [16], which allows for a common-mode conduction path between the grid and the inverter and control of the common mode voltage.

Fig. 2 shows two different types of inverter topologies, one with the neutral connection made by a split DC-link cap and another with the neutral connection made with an additional phase leg, interfacing with each of the grid topologies shown in Fig. 1. The inverters with the additional phase leg connected to neutral (Fig. 2-(A1, B1, C1, D1)) can be considered full-bridge implementations and are referred to as Type 1. The inverters with the split DC-link capacitor (Fig. 2 - (A2, B2, C3, D4)) supporting the neutral connection can be considered half-bridge implementations and are referred to as Type 2.

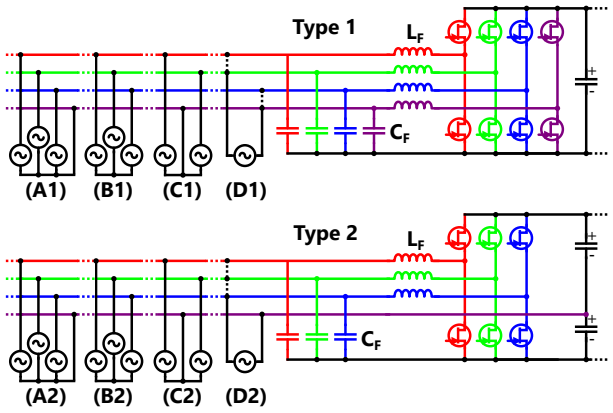

Fig. 3. Type 1 (full-bridge, top) and Type 2 (half-bridge, bottom) adaptable power converter topologies.

The Type 1 inverter, when interfacing with a three-phase four-wire grid (Fig. 2-(A1)), will require four half-bridge modules. Both the three-phase three-wire and split single-phase (Fig. 2-(B1) and 2-(C1), respectively) require three half-bridge modules, and the single-phase configuration (Fig. 2-(D1)) requires two.

For the Type 2 inverter, both the three-phase four-wire grids (Fig. 2-(A2) and 2-(B2), respectively) require three half-bridge modules as the grid neutral interfaces with the split DC-link node. The split single-phase grid configuration ((Fig. 2-(C2)) requires two half-bridge modules, and the single-phase configuration (Fig. 2-(D2)) requires one.

The entirety of the full-bridge implementations (Fig. 2-(A1, B1, C1, D1)) can be made with a single circuit. Likewise, the entirety of the half-bridge implementations can also be covered with a single circuit. These circuits can be seen in Fig. 3.

Both Type 1 and Type 2 inverters can use the same half-bridge module design. The Type 1 uses four half-bridge modules as one is used for the neutral connection. The Type 2 uses three as the neutral connection is made with the split DC-link capacitor. Individual power electronics component quantities can be found in Table II, where M represents switching devices.

Table II also shows what components are used when interfacing with each grid topology. It is important to note that the entirety of the power electronics components are not used for every configuration. Furthermore, there are opportunities to parallel modules for additional power in single-phase grid operation (parallel connections are made with dotted lines in Fig. 3). However, parallel connections are out of the scope of this paper but are a potential area of research.

There are also different required component values for each configuration. The following section provides some guidelines on component sizing for different configurations.

IV. Design

As the design of this inverter is intended to be used for multiple different grid interfaces, the component sizing needs to satisfy all possible grid interfaces. Minimum values must be defined for all possible configurations, and only values that satisfy the minimums of all the possible grid configurations can be considered.

Sizing the filter capacitance C_F and inductance L_F can be done using typical methods and their design process is not within the scope of this paper. Within the scope of this paper is the required minimum sizing of the DC-link capacitance, which can vary significantly between three-phase and single-phase configurations.

The inherent pulsating power that is present in single-phase configurations but not in three-phase configurations presents a unique design challenge for the proposed adaptable inverter. This pulsating power flow of single-phase converter can be seen in Fig. 4. This pulsating power flow is in stark constrast to the constant power flow of three-phase systems.

Typically it is the job of the DC-link capacitance to filter this pulsating power by acting as a source and sink of charge. Because of this, the three-phase inverter has a small minimum required DC-link capacitance and the single-phase converter has a relatively larger minimum required DC-link capacitance. This is true for the typical design, however, leveraging SHI allows for the minimum required DC-link capacitance of the single-phase converter to approach the minimum required DC-link capacitance of the three-phase converter.

To understand the improvement offered by second harmonic injection it is first necessary to understand the typical approach to sizing the DC-link capacitance. As shown in Fig. 4, the DC-link capacitance needs to absorb the pulsating energy of the grid P_{pulse} [17]. This is equivalent to the difference between the average and the instantaneous power. For single-phase, the instantaneous (P_{inst}) and average (P_{avg}) powers are equal to

$$V = \sqrt{2}V_s\cos(\omega t) \tag{1a}$$

$$I = \sqrt{2}I_s\cos(\omega t + \phi) \tag{1b}$$

$$P_{inst} = I_sV_s\cos(\phi) + I_sV_s\cos(2\omega t + \phi) \tag{1c}$$

$$P_{avg} = I_sV_s\cos(\phi), \tag{1d}$$

where V_s and I_s are the nominal grid voltage and current RMS values, respectively. ϕ is the phase difference, in radians, between the grid voltage and current. The power that needs to be absorbed by the DC link filter capacitance, P_{pulse}, can then be found as the difference between P_{inst} and P_{avg} and is equal to

$$P_{pulse} = I_sV_s\cos(2\omega t + \phi). \tag{2}$$

TABLE II
Adaptable Inverter Component Quantities

Grid Topology	Type 1			Type 2		
	L	C	M	L	C	M
A	4	5	8	3	5	3
B	3	4	6	3	5	3
C	3	4	6	2	4	4
D	2	3	4	1	3	2
Total	4	5	8	3	5	3

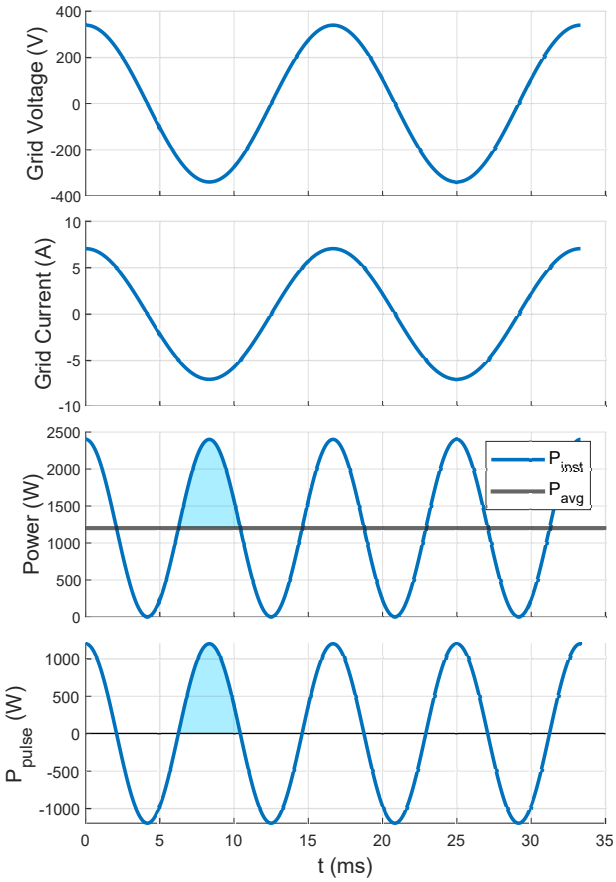

Fig. 4. Grid voltage, grid current, and power flows of the single-phase grid. The area shaded in blue represents the energy that the DC-link capacitance must absorb.

Lastly, the energy that the DC-link capacitance needs to absorb E_{Cdc} is the integral of P_{pulse} over one the shaded region in Fig. 4

$$E_{Cdc} = \left| \int_{\phi+\frac{\pi}{4\omega}}^{\phi+\frac{3\pi}{4\omega}} P_{pulse} dt \right| = \frac{I_s V_s}{\omega}. \tag{3}$$

It can be seen in (3) that the E_{Cdc} depends only on the apparent power of the converter and the grid frequency. The reactive power does not influence P_{pulse} or E_{Cdc}. The required capacitance sizing is then a function of the tolerable voltage ripple according to

$$C_{DC} = \frac{I_s V_s}{\omega V_{DC} \Delta V_{DC}} \tag{4}$$

where C_{DC} is the total DC-link capacitance, V_{DC} is the DC-link voltage, and ΔV_{DC} is the allowable peak-to-peak ripple voltage of the DC-link. It can be seen that the required capacitance is linearly related to the power of the converter, and in many cases, will be quite large for single-phase operation. This is in contrast to three-phase operation, where the power flow is constant and the pulsating power negligible. In this scenario, the DC-link capacitance is sized in accordance with the high frequency ripple of the switching converter. However, unlike

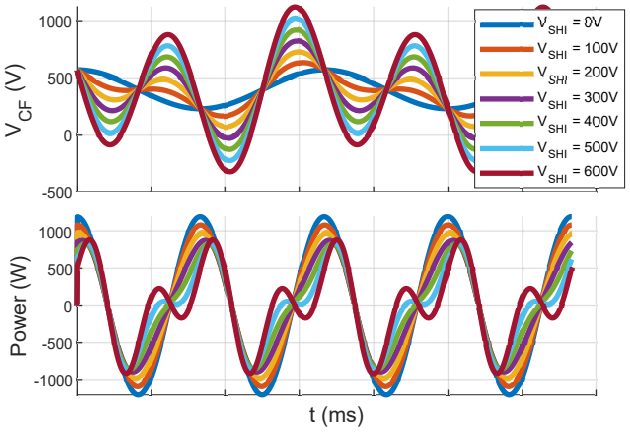

Fig. 5. Filter capacitor C_F voltage and instantaneous power P_{inst} for different amounts of applied SHI.

single-phase, this ripple is not inherent to the type of grid connection but is instead a function of the switching converter design parameters and will therefore vary for different designs.

A. Second Harmonic Injection

The instantaneous pulsating power of (2) drives the need for large DC-link capacitance. If the instantaneous power of the converter can be controlled, then the pulsating power P_{pulse} can be driven towards zero. One way of controlling the instantaneous power of the converter is by controlling the common-mode voltage of the filter capacitors

$$V_{CF1} = \frac{V_{DM}}{2} + V_{CM} \tag{5a}$$

$$V_{CF2} = -\frac{V_{DM}}{2} + V_{CM}, \tag{5b}$$

where the differential voltage V_{DM} is equal to the instantaneous grid voltage of (1a). The nominal value of common mode voltage V_{CM} is considered as, but is not necessarily limited to, one-half the DC-link voltage.

(1a) - (4) assumes the common-mode voltage of the filter capacitors C_F to be constant. This is not strictly necessary as the connection of the negative terminal of the filter capacitors to the negative DC-link allows for the common mode voltage

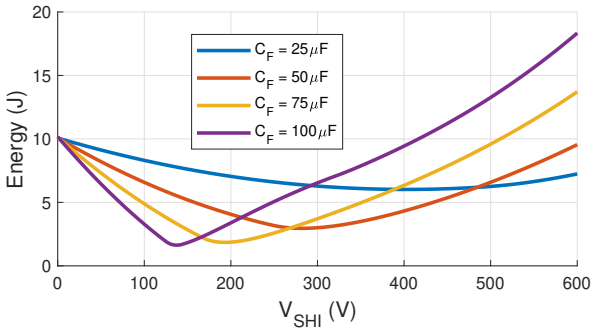

Fig. 6. Energy required to be absorbed by the DC-link capacitance as a function of applied SHI for different filter capacitor C_F values.

of the filter to be controlled. Harmonics can be injected into the common-mode of the capacitor voltage, resulting in

$$V_{CF1} = \frac{\sqrt{2}V_s}{2}\sin(\omega t) + \frac{V_{DC}}{2} + V_{inj} \tag{6a}$$

$$V_{CF1} = -\frac{\sqrt{2}V_s}{2}\sin(\omega t) + \frac{V_{DC}}{2} + V_{inj}, \tag{6b}$$

where the first terms of (6a) and (6b) are the differential mode terms and the second two terms are the common mode terms. V_{inj} is the second harmonic term that is injected into the common mode voltage of the filter capacitors.

Leveraging the common mode of the filter capacitors to absorb the pulsating power of (2) results in

$$I_{CF1}V_{CF1} + I_{CF2}V_{CF2} = P_{pulse} \tag{7a}$$

$$C_{F1}\frac{dV_{CF1}}{dt}V_{CF1} + C_{F2}\frac{dV_{CF2}}{dt} = I_sV_s\sin(2\omega t + \phi). \tag{7b}$$

This SHI process follows the one taken in [10], which also includes a full solution to the differential equation of (7b). Importantly, as shown in [10], is that a solution does exist and is dominated by (but not entirely composed of) the second harmonic. Simply injecting a purely second-order signal into the common mode can significantly reduce the pulsating power required to be absorbed by the DC-link capacitance.

This can be visualized in Figs. 5 and 6 where varying amounts of the second harmonic are injected into the common mode. Specifically, V_{inj} is set to

$$V_{inj} = V_{SHI}\cos(2\omega t + \tfrac{\pi}{2}), \tag{8}$$

where V_{SHI} is varied to control the amount of the second harmonic that gets injected into the common mode.

Figs. 5 and 6 consider an example single-phase converter that operates on a 240V 60Hz grid at $5A_{RMS}$ of current. For Fig. 5, the filter capacitor C_F is set to 24μF. It can be seen that the second harmonic injection is not capable of entirely removing the pulsating power, but can significantly reduce it. Furthermore, the value of the filter capacitance C_F has a significant effect on the magnitude of this reduction. This is because a larger filter capacitance C_F allows for more second harmonic current to be injected into the common mode.

The reduction in pulsating energy allows for the reduction of the required DC-link capacitance. For the example case of the above converter, the energy required to be absorbed by the DC-link capacitance without SHI is 10J. The energy required with SHI and a 100μF filter capacitance C_F value is, at its minimum, 1.7J. For a $10V_{p-p}$ ripple on a 450V DC link voltage, these values reflect 700μF and 120μF, respectively, for with SHI and without SHI. This represents a over an 80% reduction in DC-link energy ripple capacitance.

This effect is demonstrated, experimentally, for the Type 1 topology converter in the following section.

V. Results

An experimental prototype of the Type 1 topology is used in this section. Each half-bridge module consists of a pair of CREE C3M0032120k SiC FETs, a filter capacitor C_F value

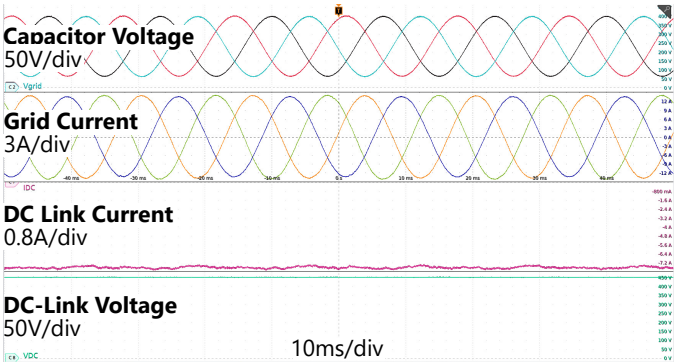

Fig. 7. Three-phase results.

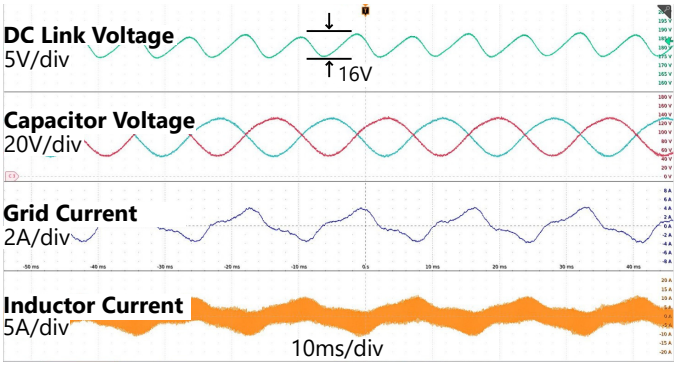

Fig. 8. Single-phase results without SHI.

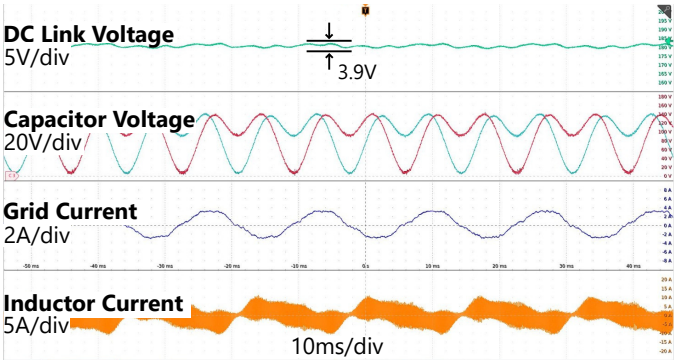

Fig. 9. Single-phase results with SHI.

of 24μF, a filter inductance L_F value of 45μF, a DC-link capacitance of 216μF, and a switching frequency of 80kHz. A Texas Instruments TMDSCNCD28379D control card is used to read sensor values, perform calculations, and actuate duty cycles.

There are three relevant scenarios included in this paper. First are the the three-phase results, which can be seen in Fig. 7. These results are found using an 450V DC-link while interfacing with a $208V_{L-L}$ grid. A constant DC-link voltage and minimum distortion on both the grid voltage and grid current can be seen. This can be attributed to the balanced nature of the prototype, as the three-phase grid requires small DC-link capacitance, and the experimental prototype has

sufficient DC-link capacitance.

This is not the case for single-phase operation, where the experimental prototype purposely uses insufficient DC-link capacitance. These results can be seen in Fig. 8, where the prototype is configured to interface with the single-phase grid. A voltage lower than the 120V single-phase grid is used here to avoid damage to the experimental prototype caused by the fluctuating DC-link voltage. A phase shift between grid current and voltage is introduced as the prototype is only flowing reactive power. This allows for the DC-link to be left floating.

It can be seen in Fig. 8 that there is significant fluctuation on the DC-link voltage. This is due to the inherent pulsating power of single-phase operation. A second harmonic is then injected into the common mode of the capacitor voltages, resulting in Fig. 9. It can be seen that this SHI significantly reduces the fluctuations in the DC-link voltage.

This shows that second harmonic injection enables this converter, sized for a nominal three-phase operation, to be adapted to a single-phase configuration while maintaining acceptable levels of DC-link ripple.

VI. Conclusion

This paper shows two different adaptable converter topologies that can be used to interface with three-phase, single-phase, or split-single phase grid topologies. The DC-link capacitance of the converters can be sized to accommodate the three-phase configuration instead of the excessively large DC-link capacitance required by single-phase configurations. This is because in single-phase mode, second-harmonic injection can be used to mitigate the inherent pulsating power of the single-phase grid, reducing its required DC-link capacitance. The proposed topology that works with second harmonic injection is key as it enables the adaptability of the proposed system to different grid interfaces. Further work on this topic would largely be centered around the construction of a higher power prototype with optimization of component values that allow for the SHI scheme to be fully leveraged along with defining a more rigorous design process.

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