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Extended ZVS Modulation for a Dual Cell Link in the Demand of Faster Balancing

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Abstract

The novel balancing circuit integrating auxiliary power modules for xEV applications is enhanced, in terms of light load performance, balancing speed, and current ripple of the inductive component. The improvements are realized by varying the operating frequency of the power switches within a reasonable range. The soft-switching range as a function of frequency, phase shift and the initial leakage inductance current is derived in detail. Faster balancing speed is achieved with little introduced losses. The power regulation strategy is also given to ensure delivering desired power designed for nominal frequency. All the concepts are verified in the high-fidelity converter model and approved to improve the balancing speed by 10 % at 110 % nominal frequency. 50 % power range increased can be achieved at 120 % nominal frequency. Higher frequencies will ensure more features, such as decreased current ripple.

1. Introduction

The battery pack, as the main and fragile component in the electrified vehicles, needs extra cares in terms of hardware and software. Many undesired accidents happen when the battery cells operate without the properly functioning battery management systems (BMSs). For example, the overuse of the battery would result in irreversible health degradation [1, 2] or catching fire in extreme cases; The battery performance is also limited by state of charge prediction [3] or the imbalance among the battery pack [4–6].

Imbalance of the battery pack is unavoidable [7]. There will always be a first fully-charged/discharged cell(s) among the unbalanced cells without cell balancing due to internal and external factors [8].

On the other hand, the charging/discharging process is usually terminated as a protection protocol if one cell/module reaches the voltage limit (either upper or lower limit) in most BMSs. The available capacity of the whole battery pack is determined/shrunk by the weakest/strongest cells. In addition, the batterys capacity will be degraded dramatically if the cells are overcharging/discharging. Therefore, the battery balancing techniques are the options to mitigate the concern. The attempts of integrating auxiliary power module with balancing circuits have been made to reduce the cost and make implementing active balancing affordable in the future EV designs [9, 10]. In authors' previous research [5, 11], a half-full bridge (HFB) DC/DC topology has been proposed to further lower the cost of the integrated balancing circuits, which requires 5 power switches less compared to dual-active bridge counterpart. One more dimension of balancing, i.e. cell-to-cell (C2C), is achievable using HFB.

As the soft-switched devices are designed around the nominal operating load, the common difficulty that they are facing is the reduced efficiencies at the light load conditions. At light load conditions, the circulating current in the transformer increases the conduction losses as well as causes the converter to lose the natural soft switching, leading to high switching loss for high-frequency devices. Even though there are many researchers have been investigating on variable frequency modulation (VFM) [12, 13] to mitigate the problem, the lack of context of battery balancing is the motivation of this paper. In addition, the C2C balancing speed is highly limited by the light-load soft switching requirement in the HFB configuration. So how to enable soft switching at light load not only can increase the efficiency but also can have the flexibility to control the balancing speed at a wide range of load conditions. The VFM for balancing HFB circuit is proposed to solve the two problems aforementioned.

The paper is organized as follows: the topology is briefly discussed in Section 2, as well as its limitation. In Section 3, the variable frequency modulation is introduced to the control in order to mitigate the limitation mentioned in previous section. The relationship between control variables and operating frequency as well as power regulation is derived in detail. A comprehensive and statistical verification has been conducted in Section 4. Lastly, the paper concludes in Section 5.

2. Dual-cell balancer and its limitation

A dual-cell balancer integrated with APM has been proposed from the authors' previous work [5, 11], as the architecture shown in Fig. 1. The concept will be briefly discussed in the following. The conventional DC/DC converter connecting high voltage battery pack and low-voltage battery is replaced by several dedicated converters illustrated

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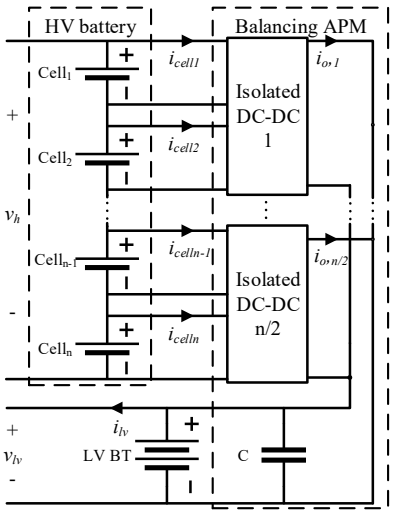

Figure 1: The layout of battery-balancing APM

in Fig. 2. Each converter is connecting with two cells/sets of paralleled cells. The output voltage of each DC-DC converter is regulated to LV range (e.g. 11 - 16 V) in the electrified vehicles. The current drawn from each converter (battery cell) is controlled to balance the HV battery pack and to meet the load current requirements at the same time.

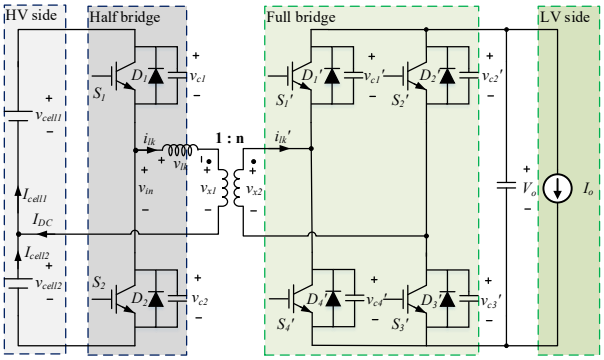

Figure 2: The proposed half-full bridge converter for dual-cell balancing

The topology has been verified to provide four balancing modes, including cell-to-cell (C2C) only, cell-to-LV (C2LV) only, C2LV & C2C, and LV-to-cell (LV2C) & C2C, as summarized in Table 1. The unique C2C path within one DC link is the advantage the topology brings without extra circuitry. The exchange current level between the two cells is controlled by the lower-level controller [5] but limited by soft-switching region where the switches can operate without introducing switching losses at high frequency (e.g. $>$ 500 kHz).

3. Extended ZVS Range by Variable Frequency Modulation

3.1. Exchange current between cells

It is important to understand the definition of the exchange current between cells since it will be a critical criteria to justify the paper's work. Aside from the AC component transferring to LV side, there is a DC current (I_{DC}) provoked by the leakage inductor parasitic in the transformer. The DC current in one battery balancing auxiliary power module (BB-APM) link determines the net current difference provided by the two cells. The exchange current ensures the link operates at the conditions where (1) no charge transfer from cell 1 to cell 2, (2) cell 1 provides more energy than cell 2 (including charging cell 2), and (3) cell 2 provides more energy than cell 1 (including charing cell 1). In each case, the higher the exchange current is, the faster the cells are balanced within one link.

Table 1: Feasible balancing modes and corresponding power flow

Conditions	Charging	Discharging
$I_{DC} > 0$ $(d = 0)$	Cell 2	Cell 1
$I_{cell1} > I_{DC} > 0$ $(d > 0)$	LV	Cell 1 and Cell 2
$I_{DC} > I_{cell1} > 0$ $(d > 0)$	Cell 2 and LV	Cell 1
$I_{DC} > I_{cell1} > 0$ $(d < 0)$	Cell 2	Cell 1 and LV

3.2. ZVS boundaries expansion

At low power load, high exchange current between the cells is difficult to achieve due to the zero voltage switching (ZVS) requirement. It will be justified theoretically by investigating the steady-state leakage inductance current in the rest of this paper.

Assuming the phase shift and duty cycle adjustment control in [5] is applied to the topology, the leakage inductance waveform is bounded by the ZVS operation, as shown in Fig. 3. The boundaries are defined by allowing the parasitic capacitor of the power switch to be fully discharged. Therefore, the switch can be turned on without generating loss. Two specific points on the waveform need to meet the commutating current level I_{com} specified by the manufacturers of the switch in order to consume all the energy stored in the parasitic capacitor. They are highlighted by red and green circles in Fig. 3. At these two points, the following equations need to be satisfied when $V_{x1} < V_{cell1}$ and V_{cell2}:

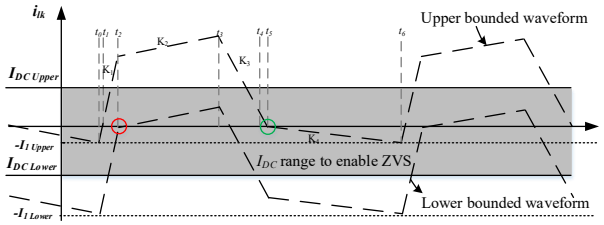

Figure 3: The waveform of leakage inductance current and its ZVS boundaries

$$i(t_2) > I_{com} \text{ and } i(t_4) < I_{com} \tag{1}$$

For the case where $V_{x1} > V_{cell1}$ and V_{cell2}, the conditions $i(t_3) > I_{com}$ and $i(t_5) < I_{com}$ need to be met. Expressing (1) as a function of I_1 is helpful to derive the boundaries for

I_{DC}. I_1 is the initial inductance current during each switching period.

$$\begin{aligned} i(t_2) &= I_1 + K_1(t_2 - t_0) > I_{com} \\ i(t_4) &= I_1 + K_1(t_2 - t_0) + K_2(t_3 - t_2) + K_3(t_4 - t_3) < I_{com} \end{aligned} \tag{2}$$

The relation between the initial leakage inductance current and the averaged one can be derived by integrating the current and being divided over the switching period.

$$I_{DC} = \underbrace{\frac{T}{8L_{lk}}(V_{cell1}\beta_1 + V_{cell2}\beta_2 + V_x\beta_3)}_{C} + I_1 \tag{3}$$

where

$$\begin{aligned} \beta_1 &= 3 - 2\theta' - \theta'^2 \\ \beta_2 &= -1 - 2\theta - \theta'^2 \\ \beta_3 &= -2 + 4d' \\ \theta' &= \frac{V_{cell1} - V_{cell2}}{V_{cell1} + V_{cell2}} \end{aligned}$$

θ' is the normalized duty cycle adjustment proposed in [5] to avoid VA imbalance in the transformer especially for the dual-cell balancing link. Combining (2) and (3) gives the boundaries for the average leakage inductance current, which is the level of exchange current to facilitate the balancing procedure. The higher the current can achieve without violating ZVS requirement, the faster the cells are balanced with minimum energy loss. For simplicity, I_{com} is assumed to be zero in this study. However, one can simply replace the value of I_{com} with the value specified by data sheet, and the equations hold. The boundaries can be expressed as follows:

$$I_{DCLower} \leq I_{DC} \leq I_{DCUpper} \tag{4}$$

where

$$\begin{aligned} I_{DCLower} &= C - K_1(t_2 - t_0) \\ I_{DCUpper} &= C - K_1(t_2 - t_0) - K_2(t_3 - t_2) - K3(t_4 - t_3) \end{aligned}$$

where, K_1 to K_4 are the slopes in the current waveform defined in Fig. 3. These equations provide the insights of the maximum and minimum of the achievable exchange current with certain system configurations, e.g. switching frequency, leakage inductance of the transformer, etc. Without going into details, the boundaries can be controlled by the parameters mentioned above. However, if the system is designed, the leakage inductance is not an option to vary but frequency is. As the frequency increases, according to (4), the upper and lower I_{DC} boundaries expand simultaneously, leading to extended I_{DC} range without violating ZVS requirement. The statement will be verified by the model of the HFB in Section 4.

3.3. Constant Power Regulation

It has been verified from previous work [11] that the output power is also a function of the frequency. If the frequency is varied to achieve higher level of the exchange current, the output power will be affected by this action as well. Sometimes, the cells are needed to generate the required constant power as well as speed up the balancing procedure, which is interpreted as constant power and increased exchange current. This requires the knowledge of I_{DC} boundaries and output power to find a proper operating point on the power curve.

The expression for output power is directly adopted from previous work [5], as repeated in (5). It is noteworthy to point out the upper boundary of I_{DC} is concerned in this study due to the assumption $V_{cell1} \geq V_{cell2}$. Otherwise, the lower boundary should be considered. Because when $V_{cell1} \geq V_{cell2}$ appears, in order to balance the cells, cell 1 will be providing more/entire power needed for the load, whereas cell 2 is expected to provide less or absorb energy. The statement $I_{DC} > I_{cell1}$ is necessary to realize cell 2 absorbing energy. Therefore, the upper ZVS boundary for I_{DC} is critical and limits the maximum exchange current instead of lower boundary in this case. Extending/increasing the upper ZVS boundary allows the higher current exchange rate with limited switching loss.

$$\begin{aligned} P_o = V_o I_o &= V_o f \int_0^T i_o(t)dt \\ &= \frac{V_o}{8fL_{lk}n}[V_{cell1}\alpha_1 + V_{cell2}\alpha_2] \end{aligned} \tag{5}$$

where

$$\begin{aligned} \alpha_1 &= -1 + 4d' + 4\theta' - 2d'^2 - 4\theta'^2 - 8d'\theta' \\ \alpha_2 &= 1 + 4\theta' - 2d'^2 - 4\theta'^2 - 8d'\theta' \end{aligned}$$

To investigate the appropriate approach to locate the optimal operation point, the example power curves at 9 different frequencies are depicted in Fig. 4 given (5). In this example, the leakage inductance and cell voltages are assumed known and follow the assumption that cell 1 has higher voltage, i.e. cell 1 needs to provide more energy. The plot shows the power curve has a higher peak as the frequency decrease, which is consistent with the theoretical analysis beforehand (i.e. frequency is proportional to output power). We also can observe that to achieve the same output power (e.g. 2 W), we have three options in this figure which are point A, B and C. But please remember one will have infinite number of combinations of frequencies and phase shifts to provide desired output power (2 W here).

Combining (4) and (5) will result in multiple roots on the power trajectory at each possible frequency. A higher I_{DC} can be realized at higher frequency and with larger phase shift while keeping output power constant. The frequency and phase shift in steady state can be obtained by substituting desired I_{DC} and P_o to (4) and (5).

3.4. Reduced current ripple

The VFM also brings another advantage in addition to increased level of exchange current. It is the reduced peak-to-peak current of the leakage inductance. The current ripple can be expressed as a function of frequency and leakage

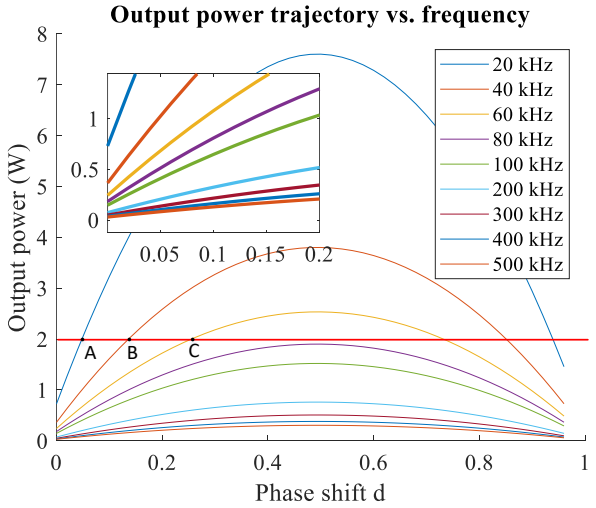

Figure 4: Output power trajectories vs. phase shift at different frequencies

inductance, as shown in (6). As long as the increment of phase shift is controlled less than the frequency counterpart, the current ripple will be deduced with increased frequency. It means as long as the circuit can tolerant the frequency and the level of the exchange current, the peak current will automatically satisfy the design requirement.

$$I_{ripple} = \frac{2dV_x - (V_1 - V_x)(\theta + 1)}{2fL_{lk}} \tag{6}$$

4. Verification

Three frequencies (20 kHz, 40 kHz, and 60 kHz) are substituted in (4) to visualize the improvement on the level of soft-switched I_{DC}. The leakage inductance is selected to be 6 uH to meet a requirement of 1-3 W output power. Please note that it does not imply this approach is only applicable at low power requirements, the leakage inductance or operating frequency range can be adjusted to satisfy the high output power.

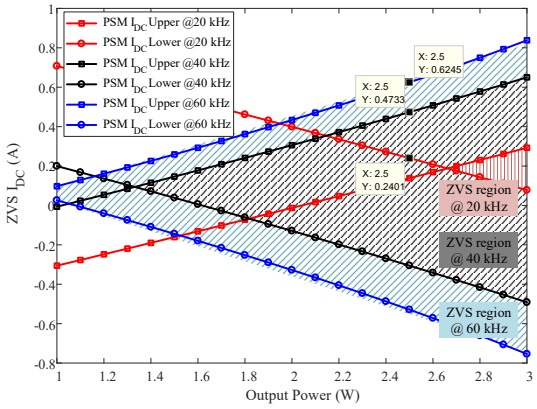

Figure 5: The visualized relationship of exchange current, output power and frequency

A ZVS region map has been created to identify the benefit of introducing VFM, as shown in Fig. 5. Two boundaries, the upper and lower boundaries of I_{DC} to achieve ZVS, have been illustrated at 20, 40, and 60 kHz. The area between these two boundaries is the operational ZVS region. For 20 kHz (red in Fig. 5), the minimum ZVS-achievable output power is around 2.6 W. In addition, the exchange current is limited to 0.1 A in order to achieve soft switching. The higher exchange current can be achieved by increasing the load, which is exactly opposite to what is expected to do. As explained previously, the battery cell has a preferred operating current level where it will not degrade the cell significantly. The cell current should not be higher than the limit. Therefore, when a cell is charging another unbalanced cell, it should not be expected to provide a high power on LV side due to the physical current limitation.

At 40 kHz, it is clear to see that the ZVS-operational area is significantly expanded compared with the counterpart at 20 kHz. Now, the soft switching can be achieved at even low load, directly to 1.4 W. By keeping increasing the frequency to 60 kHz, the ZVS range is further extended. The higher I_{DC} can be realized at the lower output power. To better visualize the benefit of VFM, a high-fidelity model for the HFB topology with two 2.8 Ah battery cells is applied to show the improvements.

The operation condition is configured to the following: cell 1 (4.0 V) has higher voltage than cell 2 (3.8 V). In order to facilitate the balancing procedure, the cells are not expected to provide high power to LV. Instead, cell 1 is needed to directly transfer energy to cell 2 at a high average current level where it does not violate the maximum C-rate that the batteries can handle. In this study, the average current level is set to be 0.24 A as well as output power to be 2.5 W. The numbers are arbitrarily selected to better explain the theory. From the previous analysis and Fig. 5, soft switching cannot be achieved with 2.5 W and 0.24 A for 20 kHz. On the other hand, for 40 kHz and 60 kHz cases, not only can they operate in ZVS mode but also they will have around 0.2 and 0.4 A margins on the leakage inductance current at the switching instant to ensure the commutating current.

The detailed leakage inductance current waveforms are illustrated in Fig. 6, showing the soft switching condition is violated when a switch is turning on at 20 kHz even though the exchange current reaches 0.24 A. The other two frequencies fulfill the ZVS switching while delivering the desired exchange current between the cells. Please note that the x-axis is normalized frequency to deliver a clearer drawing.

Another verification is to guarantee the current ripple at higher frequency is not increasing beyond the design requirement for nominal operating frequency. As analyzed in previous section, the peak and valley currents should decrease with the frequency increases. It can be verified by observing Fig. 7 that the current ripple indeed follow the theoretical analysis.

To quantify the improvements that the VFM brings, a statistic analysis is carried out in terms of ZVS-operatable

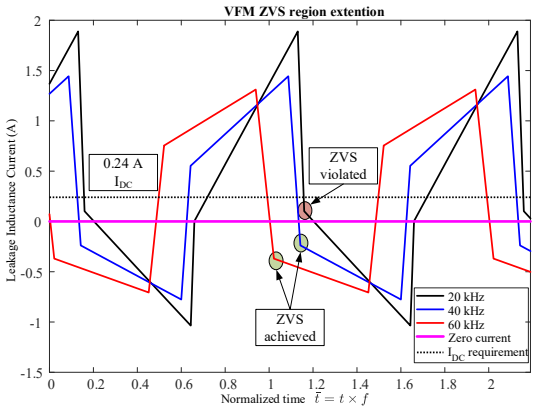

Figure 6: The detailed waveforms of leakage inductance current at 20, 40 and 60 kHz frequencies

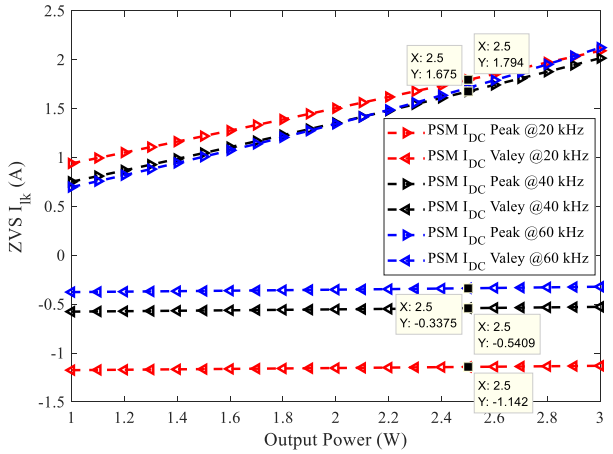

Figure 7: The peak and valley current distribution in terms of output power and frequency

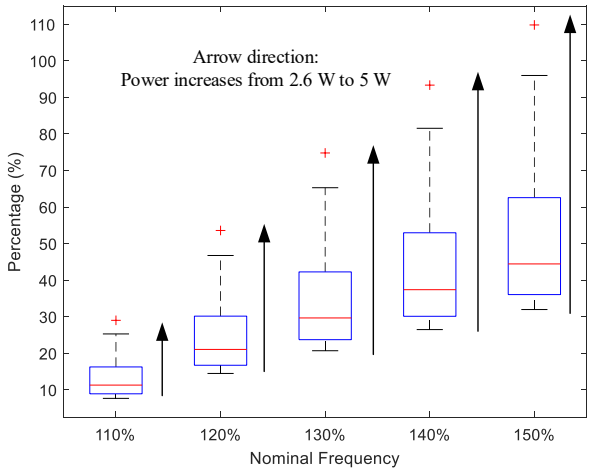

Figure 8: Box and whisker plot of upper I_{DC} improvements at different frequencies

minimum power load, upper bound of I_{DC}, and ripple current. Given the frequency change should not be too significant in practice due to EMI issue, 110% - 150% of nominal frequency is considered. Theoretically, the VFM can infinitely improve the ZVS range by increasing frequency as the current ripple is not increasing, if EMI can be properly treated at higher frequency.

As Fig. 5 and equation (3) show, $I_{DC,upper}$ is indirectly related to output power which is a function of phase shift, and frequency. The increments of the upper boundary of the DC current at different frequencies other than nominal one are summarized in Fig. 8 as a form of Box-and-Whisker plot. The red line at each condition shows the average improvement when the output power is between 2.6W and 5W. The base line 2.6 W is the minimum ZVS-achievable output power at nominal frequency 20 kHz. The blue boxes illustrate the 50% that are concentrically distributed around median, the red line. The other 50% is located in the blue-black range. For example, $I_{DC,upper}$ at 110% nominal frequency is increased by 13% average, 29% at 5 W, 8% at 2.6 W. The other frequencies can be explained similarly. It can be seen that boosting the frequency by only 10% can reduce the balancing time by 10%, assuming the cell capacities are the same. The higher frequency the circuit operates at, the faster the balancing can get. However, the trade-off must be made considering the EMI issue, efficiency, etc.

The current ripples are smaller than the nominal ones as the load sweeping from 1 - 5 W, as shown in Fig. 9. Another benefit by using VFM is to extend the ZVS to light-load conditions. The minimum power required to achieve the soft-switching is plotted from 110% - 150% nominal frequency in Fig. 11. The blue bars show that the minimum load can be decreased by around 10%, 18%, 22%, 28%, 31% with the frequency increasing. The average current ripple is also decreased. An average 5% current ripple deduction can be achieved by increasing 10% of the frequency.

For higher power rating, e.g. in the order of 10 W, the designer can either decrease the leakage inductance or increase the frequency thanks to the modularized design process. The same conclusion aforementioned will hold for the VFM. The variable frequency modulation can be easily implemented in the old controller design [5] by adding a pre-calculated VFM block which could be a look-up-table or optimization-based solution. The updated controller diagram is depicted in Fig. 10.

5. Conclusions

The paper proposed a VFM-based control to boost up the balancing speed without costing extra circuitry. With this modulation, the ZVS range can also be extended to light load conditions. The theoretical derivations of the relationship between the power load and frequency have been given and justified by statistic analysis. The advantages from the VFM that bring to the dual-cell APM balancing link are (1) shorter balancing time - increased exchange current level; (2) soft-switched and extended load range - lowered switching loss; (3) natural current ripple deduction - less stress on the inductive components;

A scalable statistic analysis is performed to quantify the

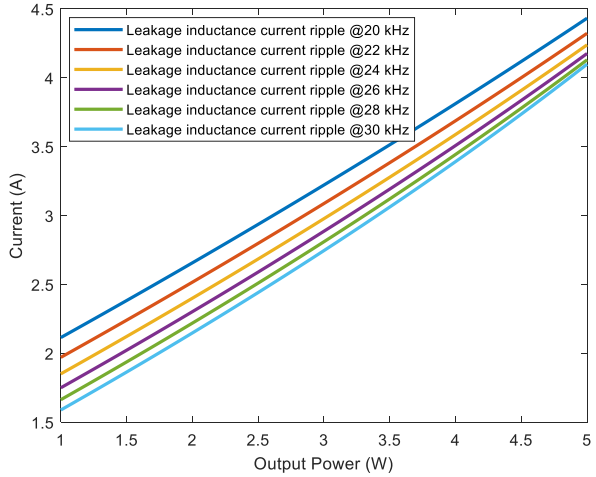

Figure 9: The leakage inductance current ripple vs. power and frequency

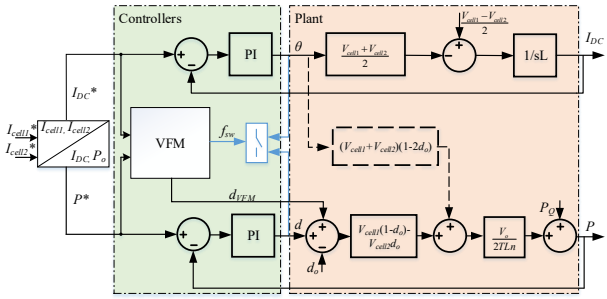

Figure 10: Modified control diagram for VFM based on the fixed frequency operation

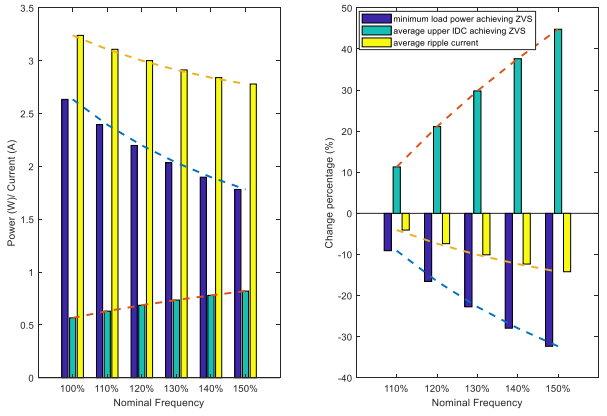

Figure 11: Improvements summary of increasing the frequency by 10% to 50%, left plot: value-based summary, right plot: percentage-based summary

improvements. It is shown that the minimum power load at 110% nominal frequency while achieving soft switching is decreased by around 10% compared with the counterpart at nominal frequency. A higher deduction rate can be achieved with a higher frequency. It means, at light load, the switching loss can be mitigated significantly. Similarly, a smaller current ripple and higher exchange current at higher frequencies are justified. The original control algorithm for the APM-BB link can be modified to enable VFM control with only a calculation-efficient LUT or a optimization process. The paper showed the advantages of VFM to the existing control logic. It can be implemented by updating the controller's law when aggressive balancing strategy is needed in the EV applications.

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