

Dual Cell Links for Battery-Balancing Auxiliary Power Modules: a Cost-Effective Increase of Accessible Pack Capacity

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Abstract—This paper focuses on the design of a half-full bridge balancing link that can reduce the cost of redistributive battery balancer in electrified vehicle applications by combining the functionalities of a battery balancer and auxiliary power module. The benefits of redistributive balancing are quantified based on existing data sets of commercial battery cells. The power rating for the electric vehicle’s auxiliary power module and balancing capability are discussed. A half-full bridge module prototype is designed to validate the proposed concept. How to reduce the current ripple on the battery cells is presented in order to minimize the degradation of the cells due to highly dynamic current. Nickel-manganese-cobalt cells are installed on the module to investigate the balancing performance in real life. The efficiency map is also given for the prototype. Compared with existing balancing methods, the improvement under the same driving cycle is shown in the long-term simulation.

Index Terms—battery balancing, high-frequency GaN switches, DC/DC converter, auxiliary power module, electromagnetic design, battery aging.

I. INTRODUCTION

ELECTRIFIED vehicles (EVs) are the most promising technologies to reduce the carbon footprints. As the main power source in EVs, batteries are the biggest concern in terms of energy density and efficiency [1]. Due to internal and external factors of battery, such as impedance/capacity variations from manufacturing process and inconsistent temperature distributions over the entire battery pack, battery cells become unbalanced during normal operations. Therefore, battery balancing is regarded as a means to increase power efficiency and cruise range [2].

A. Battery imbalance

When the cells that are connected in series have significant charge difference among them under the same load condition, this phenomenon is called the imbalance of the battery. The unbalanced battery string/pack can neither be charged or discharged once one of the cells is fully charged/discharged as the cells are protected from overcharging and discharging [3]. Unlike natural chemical process that the Lead-acid and Nickel-based batteries leak gas when overcharged, overcharging Li-ion batteries will cause irreversible damage [4]–[6]. Therefore, Li-Ion batteries require external controllers and circuits to monitor and regulate the battery behaviors in order to make them operate properly and well balanced. Typically, the balancing strategies can be categorized to

passive and active balancing. The balancing strategy is classified as active balancing when the intelligent control is engaged to regulate the balancing process.

B. Passive balancing

Conversely, if the balancing operates without any control action, it is passive balancing. For example, the small parallel resistors that always connect to the cells will slowly balance the cells. Clearly, the efficiency is relatively low as the energy is always wasted [5]–[7]. In addition, the balancing constantly operates even when the cells are balanced [8].

C. Active balancing

As one of the advantages for active balancing, the balancing process can be carefully controlled instead of applying the balancing strategy in open-loop, then undesired energy waste can be minimized. The controlled balancing process is divided into dissipative balancing and redistributive balancing.

1) *Dissipative balancing*: The excessive energy is dissipated through the resistors in a form of heat [4], which is similar with aforementioned passive balancing but in a controlled fashion using relays/switches [6], [9]. Even though the accurate state of charge (SOC) estimation is not mandatory for the dissipative balancing that can operate based on voltage, it complicates the thermal design since the resistors generate heat [10] and suffers from low efficiency. However, it is commonly used in the applications that is not performance-constrained but life-oriented, e.g. portable devices.

2) *Redistributive balancing*: The redistributive balancing is proved to be the more efficient approach by shunting the energy from stronger cells to weaker cells, such that the full capacity from the battery pack can be utilized [5]–[7]. The redistributive balancing consists of a temporary energy buffer, e.g. inductors and capacitors, that absorbs the excessive energy from strong cells and releases it to weak cells. As a result, all the cells’ SOCs are maintained at similar level. Detailed topologies to realize redistributive balancing will be discussed later.

D. Dissipative balancing vs. redistributive balancing

The most significant benefit of the redistributive balancing is the improved utilization of the available energy stored in the battery pack [11], [12]. In the battery pack that is equalized by the dissipative balancing strategy, the pack capacity is limited by the minimum-capacity cell/module [11], [12] assuming same initial SOCs, as the ‘weakest’ cell will be depleted and

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trigger the voltage protection [13] with energy left in other relatively 'stronger' cells.

To quantify the life time improvements using redistributive balancing in both first and second lives, four previously published datasets [14]–[17] where the capacity variation is captured during the same testing condition are visualized in Fig. 1. Each dataset consists of more than 10 cells with similar initial capacities, cycled under approximately same testing conditions (e.g. temperature, current). The capacity deviation is unexpectedly severe, including worst 1000 cycles difference in [16], as shown in Fig. 1(c). Due to the incomplete data at high cycle number for strong cells, necessary extrapolation is applied to project to the range where the average capacity reaches the end-of-life (EOL) capacity (80% of initial capacity in EV application).

If dissipative and retributive balancing are applied to the battery cells at certain age stage, the available capacity and remaining useful life seen by them are completely different. For example, if both balancing strategies are applied to the battery pack in Fig. 1(a) at 80% normalized capacity of weakest cell, the dissipative one will not meet the 80% EOL requirement because the available capacity is limited by weakest cell. However, the redistributive balancing can still operate and expand usable capacity to roughly 90%. Compared with the dissipative balancing where the limiting factor is the minimum-capacity cell, the life time can be extended by 17% - 36% by redistributive balancing since the usable capacity for redistributive balancing is average capacity of all series-connected cells. Even more life time can be achieved as the cells age slowly when they are well balanced. The Fig. 1(e) and 1(f) assume redistributive balancing is applied to diversely aged packs extracted from literatures [14]–[17]. They show the life time extension and increased capacity utilization within 40% capacity loss of the weakest cell while the average capacity is still above 80%, which reveals the significant improvements across not only EV but all possible secondary-life applications. In addition, there has been researches showing that the life time improvement by using redistributive balancing techniques can be as high as 21% compared with passive/dissipative balancing [18]. In addition, the usable energy is also reported to improve by maximum 23% and 7% for small-Ah and large-Ah packs [19], respectively. Therefore, the benefits of redistributive balancing are hardly convinced to be negligible, especially for recycled battery packs.

E. Existing redistributive balancing topologies

1) *Capacitor- and inductor-based*: There are extensive researches on the redistributive mechanism [5], [6], [9], [12], [20], [21], especially switched-capacitor[22], [23] and switched-inductor (or multi-winding transformer) [5], [19], [24], [25] due to their simplicity. However, transferring excessive energy from top cell to bottom cell is time-consuming as the energy needs to go through every single cell in the string [6]. In other word, the switched-capacitor/inductor configuration takes long time to balance a large battery pack and sensitive to how the imbalance distributes in the battery pack. In particular, another disadvantage for capacitor-based balancing strategy is that the balancing mechanism relies on voltage

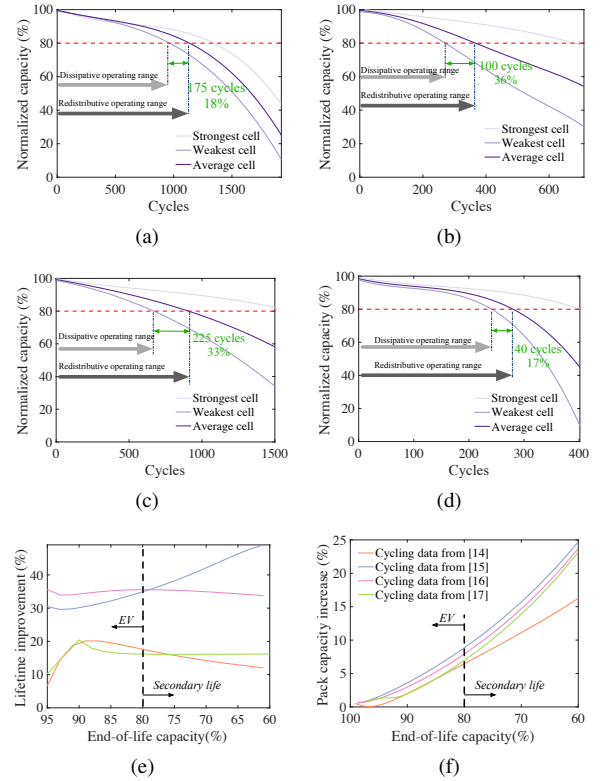


Fig. 1. Conservative projected life extension of using redistributive balancing in EV application based on cycling data from (a) [14], (b) [15], (c) [16], (d) [17]; (e) life extension within 40% weakest cell capacity loss, (f) increase of pack capacity utilization within 40% weakest cell capacity loss

difference. The nature of capacitor-based balancing utilize the voltage difference to generate the current. In the cases where the voltage barely changes while SOCs could differentiate more than 10%, the capacitor-based hardly operates properly.

2) *Converter-based*: The converter-based redistributive balancing can overcome the aforementioned concerns that capacitive and inductive balancing faces. It also enables modular design and is generalized enough to be installed in most energy storage systems.

There are two major approaches to achieve modular design: the series [26] and parallel modular designs [21], [27]–[30]. They are categorized by the bus with which the converters are linked: series modular or parallel modular design. The parallel modular design has a shared voltage bus that has an amplitude of the output voltage. Should higher output power at rated bus voltage be required, stacking more cells with paralleled converters is straightforward. However, in the case of high output voltage required (e.g. EV high-voltage (HV) bus), high step-up voltage conversion from cell-level to HV bus puts extra stress on circuit design. On the other hand, the series modular design releases the burden on voltage conversion ratio as it can bank up several modules to achieve high voltage. Nevertheless, if higher output power is required without leveling up the output voltage, the DC/DC converter needs a re-design.

To accommodate both situations, a novel auxiliary power module (APM) based balancing topology has been proposed and proved to bring the cost comparable with the dissipative balancing method [21], [31]. Especially for high-energy and

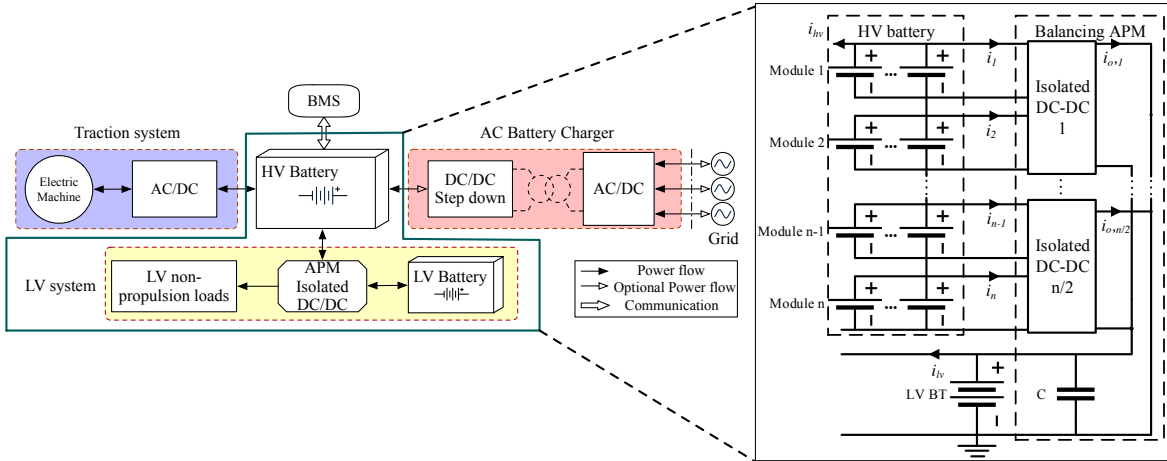


Fig. 2. Simplified EV system architecture with proposed HFB APM

relatively low-power applications like long-range electric buses or trucks, increasing the amount of the cells are more expensive than applying active balancing to fully utilize the available energy [11].

A simplified EV system architecture is given in Fig. 2. HV battery is linked with traction system, charging system, and the low-voltage (LV) battery with its LV loads via the isolated step-down DC/DC converter. Integrating the balancing functionality in the APM's converter not only reduces the cost of active balancing, but also replaces the converter that is costly and large due to high step-down voltage ratio and voltage rating [3].

F. Proposed topology

A dual active bridge (DAB) technique applied in APM battery balancing is discussed in [21]. The design fulfilled the purpose of balancing and voltage level conversion, but it is difficult to be convinced as a compact or cost-friendly design due to a large number of power switches used (8 power switches and one high-frequency transformer for balancing one battery cell/module) in DAB.

Therefore, to further reduce the cost of the concept, in this paper a half-full bridge (HFB) topology exclusively for battery balancing application is proposed to reduce the number of switches (3 switches for balancing one battery cell/parallel-connected cells) and transformers (one transformer for two cells/parallel-connected cells); offers an extra cell-to-cell (C2C) balancing mode to increase the balancing speed, without increasing the complexity of the topology, as shown in Fig. 2 and 3. Assuming same components being used for DAB and HFB, the proposed topology can reduce more than 50% of the cost on the components and corresponding footprint. Switching at MHz range also facilitates the integration of the conductive inductor in HFB into a transformer's leakage inductor instead of two independent designs of components.

The paper is organized as follows, Section II explains the basic concept and modeling of the HFB topology. The achievable balancing modes for this topology are listed and explained in Section III. Section IV shows the optimal design procedures for the filtering capacitors, transformer,

HFB power rating and balancing capability compared with state-of-art counterparts. The experimental validation and conclusions are given in Section V and VII, respectively.

This paper is the extension work of the original conference paper [32], by adding the 1) deep discussion on the benefits that redistributive balancing can bring for the EV application, 2) detailed circuit operating analysis, 3) circuit design guideline in terms of optimal filtering capacitance selection and transformer design considering electrical and magnetic limitations, 4) experimental validation to showcase and verify the operations of the circuit.

II. HFB TOPOLOGY AND AVERAGE MODELING

The proposed isolated HV-LV converter consists of a half bridge on the primary side and a full bridge on the secondary side. The systematic layout is shown in Fig. 2 and proposed isolated DC-DC converter topology is shown in Fig. 3. The half bridge allows two cells or parallel-connected cells (modules) balanced by one converter, instead of one cell/module per converter. The term 'cell' will be used to represent cell/module in the rest of paper without losing the generality. On the other hand, the full bridge offers more reliable and stable voltage on the secondary side. The high frequency transformer in between is responsible for energy transfer and galvanic isolation. Normally, an external inductor in the topology is required for the circuit operation. However, if the switching frequency is high enough and the transformer is customized for the operation, the inductor can be integrated as leakage inductor in the transformer to achieve more compact design. To simplify the analysis in this study, LV battery and loads are represented by a controlled current source depending on the load condition and HV loads are neglected. However, it is straightforward to reconsider those omitted components due to the simplification given a simple current divider rule.

A. Circuit operation

The current on primary and secondary sides is governed by the leakage inductor from the transformer by the following equation:

$$v_{lk}(t) = L \frac{di_{lk}(t)}{dt} \quad (1)$$

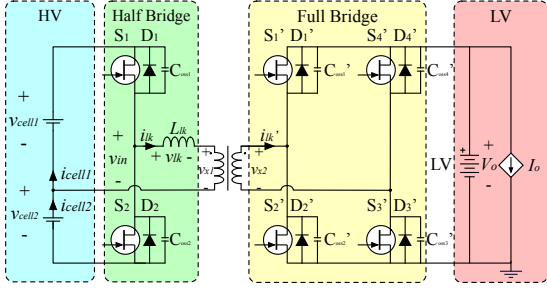


Fig. 3. The HFB topology applied in APM

As the voltage across the inductor is depending on which voltage source is connected, the current can be regulated by pulse-width modulation (PWM) control.

The proposed circuit is operating with 6 noticeable states with different combinations of switches being turned on/off and the direction of leakage inductor current, as shown in Fig. 4(a) - 4(f). The Fig. 4(a), 4(b), 4(d) and 4(e) illustrate the phase-shifted operations, which are the sources of the power transfer between primary and secondary sides in both directions [33]–[35]. In the break-down analysis, the initial leakage inductor current is assumed to be negative as the circuit is expected to operate in zero-voltage switching (ZVS) mode. Otherwise, the state 1 and 5 can be omitted during the circuit analysis.

B. Basic Control Logic

1) *Phase-shifted control*: The phase shift control is adopted in this study to enable bi-directional power flow. During the non-phase-shifted operation, the switch sets $[S_1, S_1', \text{ and } S_3']$ or $[S_2, S_2', \text{ and } S_4']$ will be turned on at the same time instance. Introducing a phase delay d between primary side (S_1 or S_2) and secondary side (S_1' and S_3' , or S_2' and S_4') switches leads to positive power flow (HV to LV), and the negative power flow can be realized by a phase lead. Without phase shift, shown in Fig. 5 (e), the average current of the secondary referred leakage inductor current is zero, thus no power. The introduced phase shift acts as a rectifier to regulate the average current, leading to a non-zero output power, as illustrated in Fig. 5 (d).

2) *Leakage inductor current drift*: The high-side switch S_1 and low-side switch S_2 are alternatively turned on for 50% of a switching period in traditional phase shift control, also known as symmetric control. Less than 50% symmetrical duty cycle can be used in phase shift control as well, but 50% duty cycle allows the largest output power range since longer phase shift can be applied. It is because the phase shift is proportional to output power, which will be explained in Section II-D.

In the isolated topology, the transformer plays an important role in integrating the series inductance into the leakage inductance. The magnetizing inductance is neglected due to its little effect on the operation of the HFB. Conversely, the leakage inductance dominates the formulations of the fundamental operations. Kirchhoff Voltage Law defines the voltage across L_{lk} on the primary side during all operation modes in Fig. 4:

$$v_{lk} = v_{celln} - v_{x1} \quad (2)$$

where the subscript $n \subseteq \{1, 2\}$ in v_{celln} indicates the index of the battery cell(s) that is currently conducting during one switching period. The battery cells can be modeled as a constant voltage source with voltage V_{celln} during a extremely short switching period. v_{x1} is the output voltage referred to primary side, which can also be assumed constant within the switching period. Therefore, the leakage inductance current changes at a rate of v_{lk}/L_{lk} , which differs when the two cells have different voltage levels, i.e. unbalanced. It results in non-zero net change of the inductor current within one period and thus it will drift towards discharging higher-voltage cell more.

The waveforms of current and voltage for L_{lk} can be depicted in Fig. 5 (c), under the condition where $V_{cell1} > V_{cell2}$. In this paper, this condition will be assumed always true. For the condition where $V_{cell1} < V_{cell2}$, one can reverse the assumption and the conclusion still holds.

As discussed above, the imbalance of cell voltages causes the the net current change on the leakage inductance non-zero within one period if symmetric control is applied, i.e. VA imbalance of leakage inductance. Consequently, the leakage inductor current diverges, as shown by red dotted line in Fig. 5 (c). The uncontrolled leakage inductor current causes many consequences, such as flux saturation, overheating and circuit damage.

3) *Duty cycle compensation*: To compensate the VA imbalance, an asymmetric control is proposed by introducing a duty cycle adjustment θ on the primary side switches. This adjustment is directly fine-tuning the conducting time for each cell based on their voltages. For example, if cell 1 has higher voltage, its duty cycle will be set to $50\% - \theta$ and cell 2 will have a complementary conducting time of $50\% + \theta$, as shown in Fig. 5 (a). It guarantees the accumulative effects of two cells on the leakage inductor current change are identical.

The duty cycle adjustment that relies on the input voltages can be derived by letting $i_{lk}(0) = i_{lk}(T)$ in one period:

$$\theta = \frac{T}{2} \left(\frac{V_{cell1} - V_{cell2}}{V_{cell1} + V_{cell2}} \right) = \frac{T}{2} \frac{\Delta V}{V_{DC}} \quad (3)$$

where, the cells' voltages v_{cell1} and v_{cell2} are approximated as constant V_{cell1} and V_{cell2} due to their slower variation at high frequency as discussed previously. ΔV is the voltage difference between the two cells, V_{DC} is the voltage of the HFB bus voltage on primary side.

C. DC current control for leakage inductance current

As the transformer transmits the electrical energy from primary to secondary side by the principle of electromagnetic induction, only alternating current can create a changing magnetic field. As a result, DC component will not produce the magnetic field change, therefore it will be blocked from primary to secondary as well as from secondary to primary. So the average/DC signals of the primary-side can be separated from the secondary side, as shown in Fig. 6(a). The average leakage inductor current is replaced by a constant current source to simplify the circuit analysis. The average current I_{DC} , which is called DC offset current in this paper, is the sum of I_{cell1} and $-I_{cell2}$ by Kirchhoff Current Law. The

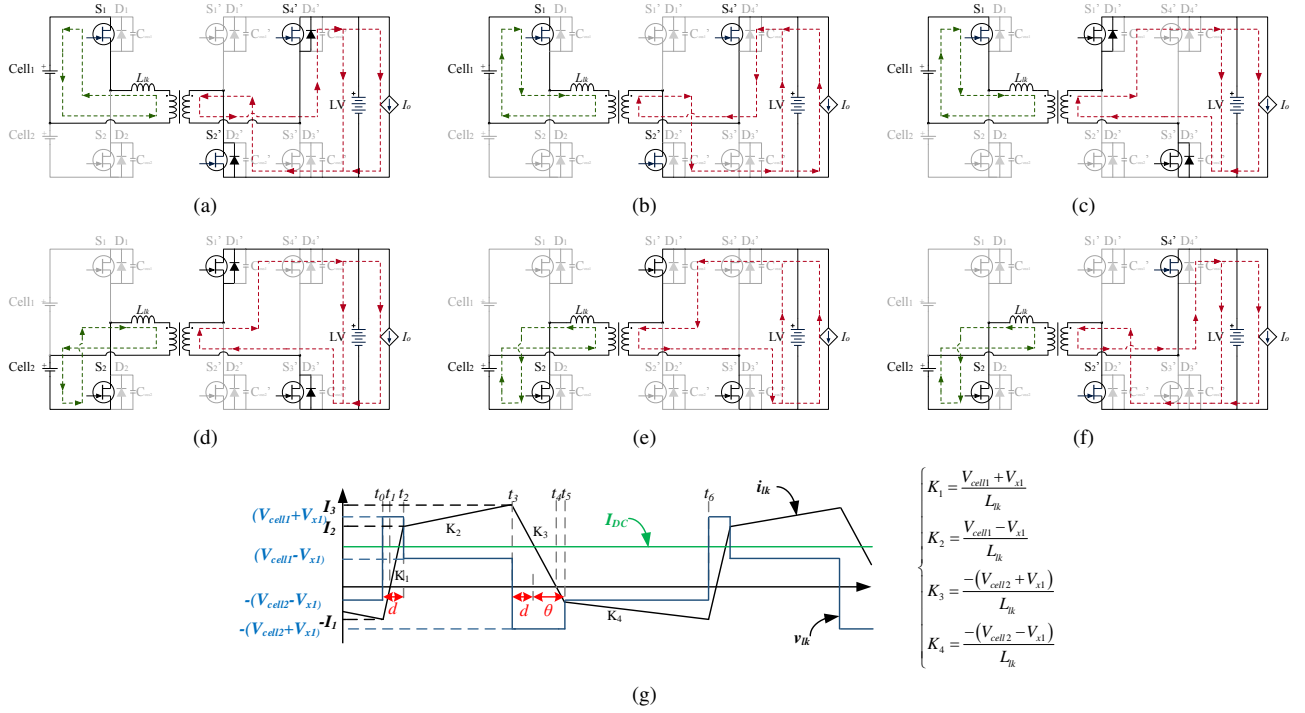


Fig. 4. Operating states of the HFB. (a) ECM between t_0 and t_1 , (b) ECM between t_1 and t_2 , (c) ECM between t_2 and t_3 , (d) ECM between t_3 and t_4 , (e) ECM between t_4 and t_5 , (f) ECM between t_5 and t_6 , (g) the leakage inductor current waveform with time stamps

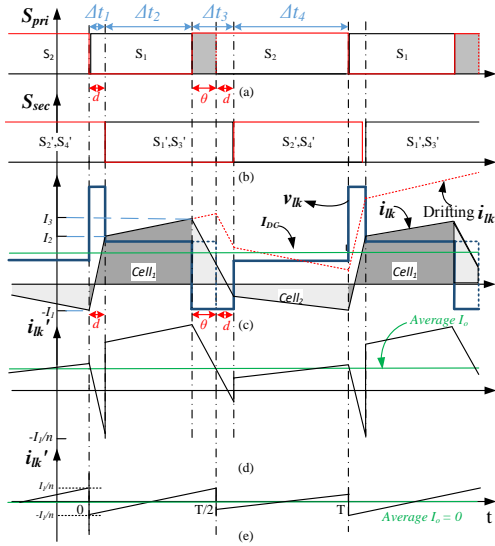


Fig. 5. Switching PWM signals: (a) primary switches, (b) secondary switches; (c) primary referred leakage inductor voltage and current: red dot - symmetric control, black line - asymmetric control; secondary-referred leakage inductor current (d) with phase shift and (e) without phase shift

current difference ($I_{cell1} - I_{cell2}$) then can be controlled by the amplitude and polarity of I_{DC} .

Actually, the manually triggered VA imbalance can guide I_{DC} to any arbitrary reference by properly introducing the duty cycle compensation at precisely controlled timings. The current difference makes the cells drain at a different rates, so that the SOC differences can be eliminated eventually, if there is any. A control example is given in Fig. 6(b) with assumption that $V_{cell1} > V_{cell2}$. Initially, the leakage inductor

current is operating at steady state with introduced duty cycle compensation based on the cells' voltages and a zero average current. If a positive I_{DC} is desired ($I_{cell1} > I_{cell2}$), a smaller compensation θ_2 is applied at $2T$, resulting in a positive net inductor current change within one period. The current will start to drift up and can be stabilized to current value by applying another duty cycle compensation θ_3 that makes the net change zero. The described process can be implemented in the microcontroller after deriving the dynamic equations of the system [30]. The higher DC offset current is, the faster the cell 1 is discharged. At the point where $I_{cell1} > I_{DC}$, the current flowing out of the cell 2 will start to reverse, i.e. charging cell 2 using cell 1, which is C2C balancing.

D. Output Characterization

It has been seen that the multiple power flow and transfer can be realized by duty compensation and phase shift previously. However, the correlation between the deliverable power and circuit parameters is still unrecognized in order to properly design the components in the HFB circuit.

The average output current can be obtained by averaging the integral of the current during one period. Due to nearly constant voltage drop over the leakage inductor on secondary side, the current waveform can also be divided into four piece-wise linear sub-intervals, i.e. $\Delta t_1, \Delta t_2, \Delta t_3$, and Δt_4 , as shown in Fig. 5 (d). The average output power from HFB can be derived as follows:

$$\begin{aligned}
 P_o &= V_o I_o = \frac{V_o}{T} \int_0^T i_o(t) dt \\
 &= \frac{V_o T}{8L_{lk}n} [V_{cell1}\alpha_1 + V_{cell2}\alpha_2]
 \end{aligned} \tag{4}$$

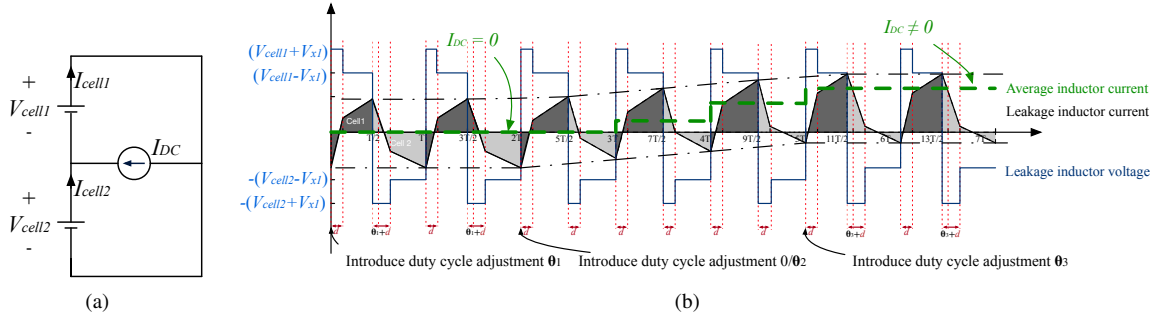


Fig. 6. Average current control: (a) the average equivalent circuit model of the primary side, (b) the average current is introduced by controlling the duty cycle adjustment

and

$$\begin{aligned} \alpha_1 &= -1 + 4d' + 4\theta' - 2d'^2 - 4\theta'^2 - 8d'\theta' \\ \alpha_2 &= 1 + 4\theta' - 2d'^2 - 4\theta'^2 - 8d'\theta' \end{aligned} \quad (5)$$

where normalized duty cycle adjustment θ' and phase shift d' are calculated by $x' = x/(T/2)$. These equations will be used to guide the design of the transformers. It should be noted that when designing the controller for duty cycle compensation and output power regulation, as the output power is coupled with duty cycle compensation term θ , separating the controllers' bandwidth by a factor of 10 will reduce/eliminate the undesired interaction between them [30]

E. Limited ZVS range due to the C2C balancing current

As the DC bias current fluctuates up and down due to the C2C balancing requirement, the circuit eventually loses soft-switching capability if large DC bias presents. The achievable ZVS boundaries are defined by the minimal circulating current that allows the parasitic capacitor of the power switch to be fully discharged before turn-on signal arrives. Therefore, the switch can be turned on with zero drain-source voltage. Should higher DC bias current be desired, increasing switching frequency contributes to a higher DC bias current while keeping circuit running in ZVS region. The extensive analysis has been performed previously in authors' research [36]. So this paper omits the derivation but providing a ZVS range of I_{DC} for the prototype: the switches will be soft-switched at rated power as long as I_{DC} is within $\pm 5A$.

III. FEASIBLE BALANCING MODES

As discussed previously, the power can be transferred between cells and/or LV system. Therefore, different combinations of power flow direction create four typical balancing modes with proper DC offset current and phase shift control: a) C2C and cell to LV (C2LV), b) C2C and LV to cell (LV2C), c) C2LV only, and d) C2C only.

A. C2C and C2LV

In this mode, the high-SOC cell is demanded to charge the low-SOC cell and power auxiliary loads. It is advisable to adopt this mode when the LV battery is charging or LV loads are online and initial SOC bias is significant. The excessive energy from high-SOC cell charges low-SOC cell to converge all cells' SOC to the same level. Meanwhile, the LV battery/loads are being powered by the rest of energy from high-SOC cell.

B. C2C and LV2C

This mode is triggered by the LV's no/low-load condition as well as the presence of significant difference between the SOC of two neighboring cells in the same HFB. LV battery and high-SOC cell merge their energy to charge the low-SOC cell. As a result, the bias among HV battery cells will be eliminated faster than the LV2C-only techniques. The improvements might be subjective to the battery status, but the C2C path will boost up the balancing speed with a reasonable amount of time. It is extremely beneficial for the systems that need the battery cells balanced in a short time, for example the scheduled super-fast charging programs. The real battery comparison between the conventional LV2C balancing and C2C direct balancing is given in the experiment results section.

C. C2LV-Only

If the neighboring cells are out of balance under conditions, e.g. (1) minor imbalance, (2) LV loads require all cells to provide maximum viable power, or (3) balancing speed is not prioritized, it is more reasonable to discharge both cells simultaneously but in different C-rates. Therefore, the initial SOC bias is gradually compensated due to the C-rate difference while charging LV battery or powering LV loads.

D. C2C-Only

The featured power flow direction is specifically available in the HFB, as cell 1 and cell 2 share the common DC current path blocked from secondary side with the primary side of the transformer. This mode is activated when neighboring cells are out of significant balance and LV system is offline. Unlike the other balancing topology to achieve C2C balancing direction indirectly, the LV system is not required as the intermediate station to pass energy from one cell to another. Therefore, the unwanted electronics losses by transferring charges from cell 1 to LV and from LV to cell 2 can be omitted.

E. Corresponding Realization of Modes A, B, C and D

As we discussed before, the I_{DC} can be controlled to be any numeric value as long as the core is not saturated and the circuits can tolerate. It can be seen from the Fig. 5 and 6(a) that DC current offset $I_{DC} = I_{cell1} - I_{cell2}$. As long as $I_{DC} > 0$, i.e. $I_{cell1} > I_{cell2}$, cell 1 offers more energy, and vice versa.

TABLE I
FEASIBLE BALANCING MODES AND CORRESPONDING POWER FLOW

Mode	Conditions	Charging	Discharging
C2C+C2LV	$I_{DC} > 0$ ($d > 0$)	LV	Cell 1 and 2
C2C+LV2C	$I_{DC} > I_{cell1} > 0$ ($d < 0$)	Cell 2	Cell 1 and LV
C2LV only	$I_{cell1} > I_{DC} > 0$ ($d > 0$)	LV	Cell 1 and 2
C2C only	$I_{DC} > I_{cell1}$ ($d = 0$)	Cell 2	Cell 1

For example, if $I_{DC} = 10A$, it indicates that cell 1 supplies 10 A more current than cell 2. When $I_{DC} > I_{cell1}$, $I_{cell2} < 0$ will happen naturally according to the circuit property. As a result, cell 1 is discharging while cell 2 is charging, despite that LV side is charging or not. Therefore, the DC current offset gives an idea of balancing direction and speed.

Given the discussion above, mode A requires that cell 1 supplies the energy (positive I_{cell1}) and cell 2 absorbs the partial energy (negative I_{cell2}) transferred from cell 1. It is feasible when $I_{DC} > I_{cell1} > 0$. In this case, I_{cell1} is definitely positive due to C2LV direction of power flow.

Except for the LV2C power flow, mode 2 is similar with mode A in terms of the behavior of cell 2. Mode B requires LV2C power flow direction which is the result of negative phase shift d . The I_{DC} inequality conditions for this mode preserve as mode 1.

The negative I_{cell2} is not valid in mode C anymore. Conversely, energy is needed from cell 2. Therefore, the condition is changed to $I_{cell1} - I_{DC} > 0$ so that cell 2 outputs power instead of absorbing power. The other requirements for cell 1 and direction of power flow remain the same as mode 1. The modes discussed above and corresponding control conditions are summarized in Table I. For the C2C-only mode, phase shift is zero while the DC current is maintained larger than I_{cell1} .

IV. DESIGN GUIDELINES

The numeric values of the circuit components will determine the behavior of the operation, such as operable switching frequency and continuity and amplitude of the output power. The design guide of two important components is given here. In addition, system-level design considerations are explained, including power rating and balancing capability.

A. Output Capacitor Design

As the output current i_{lk2} is fluctuating within a large range due to the switching, the LV loads, however, require relatively constant current to be input. The capacitive filtering is added to refine the original current waveform in order to deliver roughly constant current to the LV system, as shown in Fig. 7. Ideally, the output capacitor C_o will absorb the AC component in i_{lk2} but remain the DC component to the LV loads. By subtracting the DC component from i_{lk2} , the ideal capacitor current is drawn in the Fig. 7. The capacitor voltage change is governed by the capacitance definition $\Delta V = \Delta Q/C$.

Since the voltage ripple ΔV needs to be restricted within a negligible range (1% of operating voltage in this work) in

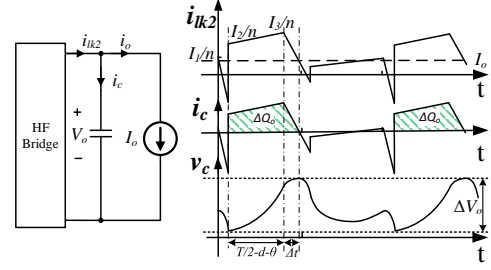


Fig. 7. Filtering capacitor design, left: equivalent circuit focusing on output, right: output-side current and voltage waveforms

order to fulfill the assumption that the output voltage is roughly constant during the circuit analysis, the capacitance is required to be adequate to absorb the energy that causes the capacitor voltage fluctuating without violating the boundaries.

The charges that elevate the cap voltage is a result of the integrated shaded area of the capacitor current. It can be calculated by integrating the current over the period, resulting in ΔQ_o . Thus, the largest peak-to-peak ripple happens when the ΔQ_o reaches the maximum. The geometry analysis can be applied and the expression of ΔQ_o can be obtained:

$$\Delta Q_o = \left(\frac{T}{2} - d - \theta + \Delta t\right) \frac{(I_2 + I_3 - 2nI_o)}{2n} + \frac{\Delta t I_3}{2n} \quad (6)$$

$$\text{where } \Delta t = \frac{I_3/n - I_o}{K_3} \quad (7)$$

$$I_2 = -I_1 + K_1 d \quad (8)$$

$$I_3 = -I_1 + K_1 d + K_2(T/2 - d - \theta) \quad (9)$$

$$0 < \frac{nV_{cell2} - V_o}{nL_{lk}} \frac{(1 - d')T}{2} \leq I_1 \leq \frac{nV_{cell1} + V_o}{nL_{lk}} \frac{d'T}{2} \quad (10)$$

where K_1 and K_2 are the slopes of the inductor current change, as shown in Fig. 4(g).

It can be seen that the initial inductor current I_1 is inversely proportional to the charge ΔQ_o , so that the minimal I_1 will result in largest change in capacitor charge regardless of other dependencies. To remain minimal soft switching during turn on and find minimum capacitance to stabilize voltage at all conditions, the initial inductor current is chosen to be the lower boundary described in Eq. (10) derived in [32]. Due to highly coupled dependencies on phase shift d , duty cycle compensation θ and cell voltages V_{cell1} and V_{cell2} , a parameter sweep is performed to find the optimal capacitance, as shown in Fig. 8. The voltage is swept within the following range: $3.5 \leq V_{cell1} \leq 4.2V$, $2.7 \leq V_{cell1} \leq 3.4V$. Phase shift is spanned from 0.1 to $(T/2 - d - \theta)$ while keeping θ constant based on Eq. (3).

The largest ripple appears when the cell voltage difference is maximized as well as the power (phase shift), as the figure suggests $66 \mu F$ capacitance is required to remain current nearly constant. However, when cell voltages are similar, the required capacitance to keep I_o constant is reduced to less than $10 \mu F$. A comparison of filtering performance using different capacitance is given in Fig. 9, which is simulated in MATLAB/Simulink with PLECS toolbox. The cell voltages are selected to be [2.7V, 4.2V] as the worst case indicated. The simulated capacitances are $10 \mu F$ that is adequate for [3.4V, 3.5V]

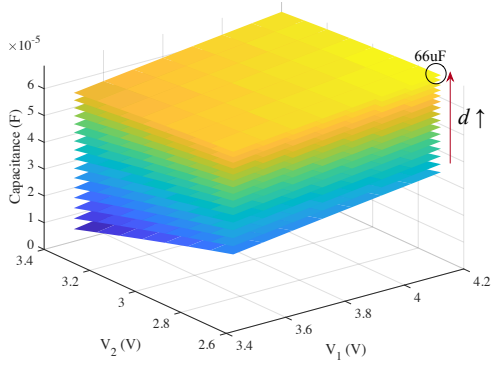


Fig. 8. Required capacitance across combinations of cell voltages and phase shift

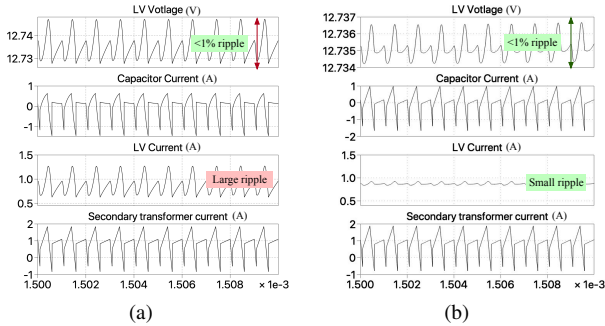


Fig. 9. Simulation results of output current ripple with 4.2V and 2.7V cell voltages: (a) $10\mu F$ filtering capacitance, (b) $66\mu F$ filtering capacitance

combination, and $66\mu F$ that can handle worst case scenario. The simulation results indicate that $66\mu F$ is capable of stabilizing the output current reasonably well, whereas $10\mu F$ capacitance will introduce large oscillation on the output current.

B. Transformer Design

As the power is limited by the leakage inductance in Eq. (4), optimally selecting the leakage inductance will achieve more compact design and reduced cost from over designing.

1) *Output power requirement*: The rated output power per HFB should be considered for transformer design. The conditions that physically/electrically limit the output power are switching frequency T , leakage inductance L_{lk} , and turns ratio n . On the other hand, the range of phase shift d and the duty cycle adjustment θ are the controllable variables that tune the output power within the physical/electrical range.

Based on Eq. (4), the power spectrum can be obtained by sweeping phase shifts d and the leakage inductance levels L_{lk} under the worst scenario of cell voltages (cut-off), which is shown in step 4 in Fig. 10. The power spectrum helps designer locate the optimal leakage inductance to achieve rated power in the worst case scenario. For general design procedure, a flowchart for selecting the leakage inductance is given in Fig.10.

2) *Magnetic design considerations*: In contrast with conventional transformer design, due to the presence of DC current in the leakage inductor for C2C operation, the core saturation needs to be carefully checked at rated C2C current level. If the core will be saturated at the rated current bias

level, a better (higher saturation flux density) or larger core is needed. The overall design is a combination of designing a transformer and an inductor. The following inequality has to be satisfied to stay away from core saturation:

$$I_{DC} < \frac{(B_{sat} - \Delta B/2) \times MPL}{0.4\pi\mu_r\mu_0 N} \quad (11)$$

where B_{sat} is the maximum flux density that the core can operate without saturation, ΔB represents the flux swing induced by periodically alternated square-wave voltage applied to the primary side of the transformer. MPL indicates the magnetic path length, which is normally given by the manufacturer. μ_r and μ_0 are the relative permeability respect to free space and permeability of the free space, respectively. N is the number of turns on primary side.

Even if the transformer for HFB needs to operate at a DC current without saturation, the design barely induces difference compared to conventional transformer design in terms of losses and design complexity, such as the one in [21]. Transformer losses consist of core and copper losses. The winding property contributes to copper loss. The core loss is determined by the hysteresis effect of the core material which hardly relates to where the hysteresis loop starts (DC-operating point), as long as the peak/valley current will not drive the core to saturation. Therefore, the only trade-off when designing the transformer for HFB is the airgap/material as inducing airgap increases the DC current carrying capability for the core, or simply a better material with high saturation flux density.

Even though a precise leakage inductance can be achieved and validated in the computer aided programs like ANSYS/Maxwell or JMAG, the manufacture variation can be introduced to degrade the coupling between primary and secondary, leading to higher/lower leakage inductance than designed. The rated power requirement might not be guaranteed due to the change of leakage inductance. But it should not be worried, the advanced control strategy like variable frequency [36] can be adopted to overcome the short of power and provide other benefits like extended soft-switching range and smaller peak current.

C. Power rating and balancing capability

1) *APM power rating*: Depending on the identity of the electric vehicle, the rated power for the auxiliary power modules is undetermined. The more luxury the vehicle is, the heavier LV loads could be as more power is needed for extra LV functionalities, e.g. steering wheel and seat heating. From previous literatures, the rated current for APM is between 100-200A, which translates to 1.2-2.4 kW power output [37], [38]d. Therefore, for a 100-cell/module HV battery system, output power of 12-24 W for each cell/module to LV should be guaranteed. As two cells are managed by one HFB, the HFB should be rated for 24-48 W and can be designed accordingly based on Eq. (4).

2) *HFB balancing capability*: The balancing capability is defined by the net current between two cells in one HFB and the net power between HFB modules. The net current I_{DC} is limited by the preferred ZVS range [36], and is rated at 5 A in the prototype that is shown in later section. Aside from

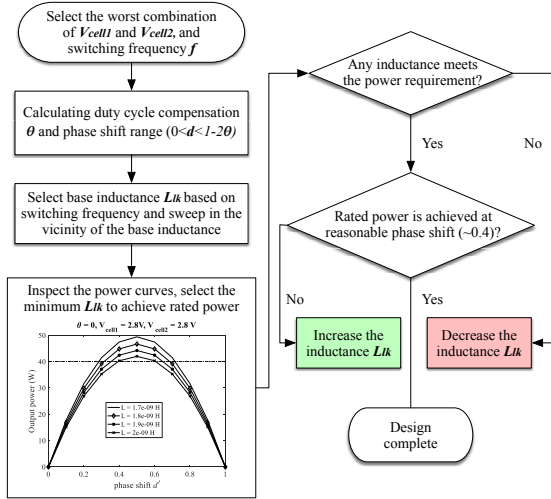


Fig. 10. Flowchart of selecting leakage inductance to achieve rated power and peak current limitation

C2C balancing, C2LV/LV2C will also assist equilibrium of the battery pack. One or more HFBs can operate at reversed power flow with respect to the rest of HFBs in order to balance the cells. A little room is given on each HFB's rated power so that the power needed from the cells under balancing can be compensated by more power from the rest of cells. Therefore, a 5W-room for each HFB is spared for C2LV/LV2C at maximum load. Note that the room for extra power can be tweaked by design easily, as well as the rated net current.

Aforementioned parameters would simply provide a 0.1C-rate current for balancing a 150Ah EV battery pack, which is more than enough for 'maintenance' balancing and comparable for 'gross' balancing current level mentioned in [11], as well as other individual-converter topologies [21], [26].

V. EXPERIMENTAL RESULTS

A. Experiment setup

The circuit-functional tests are performed on two DC power supplies that reacts as the battery cells/modules to simplify the validation process of requiring battery cells that are at different aging statuses. In addition, real battery cells are used to validate the balancing operation. The HFB is constructed by three off-the-shelf half-bridge GaN modules EPC9201 and EPC9203 with integrated gate drivers and a self-designed planar PCB transformer due to the lack of commercial transformers that are suitable for this circuit operation. The goal of the tests is to experimentally verify all the feasible operation modes described in Sec. III via a real-time microcontroller, TI 28377s. The testing conditions and hardware parameters are listed in Table II. The continuous-time PI controller equation is approximated by Forward Euler method in order to implement the control algorithm in digital signal processors. The corresponding outputs (phase shift d and duty cycle adjustment θ) from the discrete-time PI controller are input to the HRPWM module in TI 28377s to regulate the energy transfer between cells and LV system. The prototype setup is shown in Fig. 11.

The prototype might not fit into the space-constrained applications, such as portable devices. Further optimization

TABLE II
EXPERIMENTAL PARAMETERS OF THE PROPOSED HFB TOPOLOGY

Switching frequency (MHz)	1
Sampling frequency (MHz)	0.2
Transformer turns ratio	1:5
Transformer leakage inductance (nH)	76
Output filtering capacitor (μ F)	66
HV cell voltages (V): Mode A, B, and D	Cell ₁ = 4, Cell ₂ = 3.5
HV cell voltages (V): Mode C	Cell ₁ = Cell ₂ = 4
LV cell voltage (V)	12

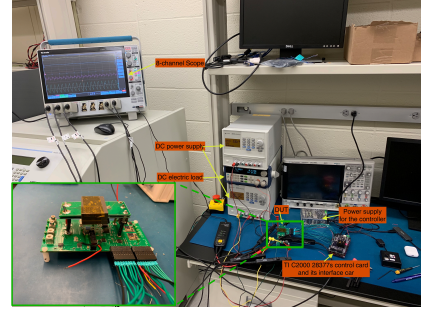


Fig. 11. Testbench setup

on the design can be achieved to shrink the footprint. For example, the transformer can be integrated into the circuit board. Note that the HFB prototype is validated on cell basis. However, the HFB module is intended to work on both cell level and module/pack level. Therefore, the size restriction can be loosed for large-scale high-Ah battery packs. In addition, the necessary sensors and computation power are completely embedded in the HFB module, so that other BMS functions can be integrated into the HFB module (e.g. SOx estimation and over/under voltage protection) without adding extra circuitry.

B. Asymmetric control to eliminate the core saturation

Due to the unbalanced voltage on the two cells, the current will drift without duty cycle compensation as explained in Section II-B. In order to experimentally validate the asymmetric control, the cell 1 and cell 2 voltages are selected to be 4V and 3.5V, respectively. The circuit operation is captured in Fig. 12.

The conducting time for high voltage cell 1 needs to be decreased to maintain the net change of the leakage inductor current to be zero so that the current is stable. A 3.33% duty cycle reduction on cell 1 can be calculated according to the Eq. (3), which leads to 46.67% and 53.33% theoretical conducting duty cycles for cell 1 and cell 2, respectively. In the experimental results, 46.6% and 53.4% duty cycles are observed on the PWM signals. The theoretical and experimental results are consistent considering the switch transition from one state to another and measurement inaccuracy.

C. Balancing mode validation (A-D)

The four balancing modes listed in Table I are also validated in the prototype testbench with real-time controller. The

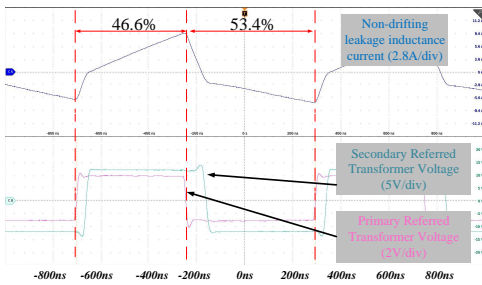


Fig. 12. Leakage inductor current measurement: asymmetric control regulating unbalanced cells non-drifting

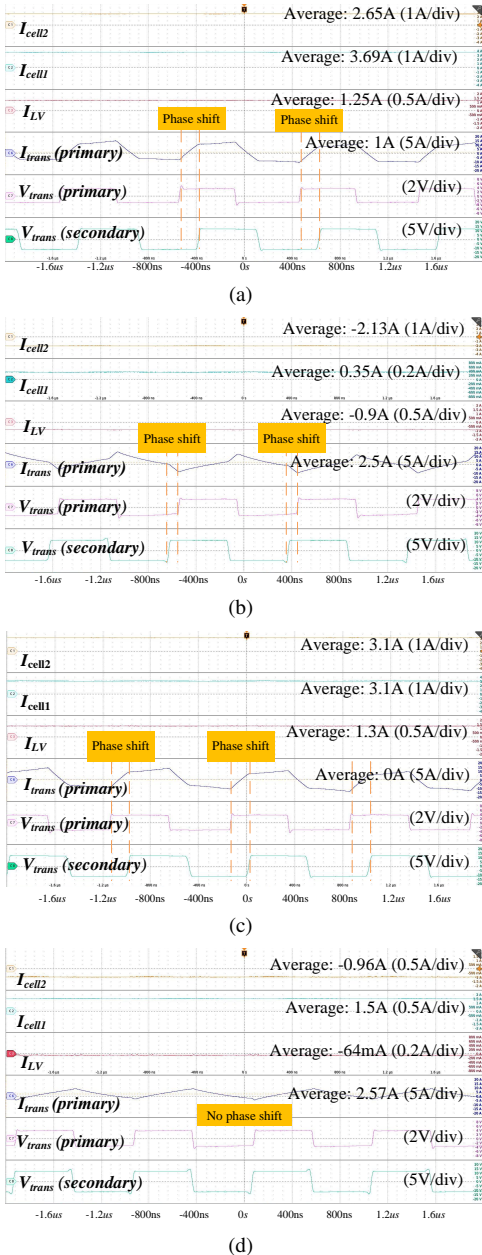


Fig. 13. Operating modes validation captured by Tektronix Oscilloscope, (a) Mode A C2LV + C2C with unequal cell currents, (b) Mode B LV2C + C2C, (c) Mode C C2LV only with equal cell currents, (d) Mode 4 C2C only

measured currents I_{cell1} , I_{cell2} and I_{LV} are given to show the power flow and C2C energy transfer. Again, the positive cur-

rent convention is defined as follows: the currents discharging the cell 1 and cell 2, and the current charging the LV system.

When the neighboring cells are slightly unbalanced and LV system has to be supplied, the Mode A activates both cells to transfer energy to the LV side while demanding more current on the stronger cell. So the unbalanced cells should be eventually converging to the same SOC level after certain amount of time depending on the balancing current level, then the Mode C will be initiated to drain the cells equally afterwards. During the validation of Mode A, cell 1 is set to be 0.5V higher than cell 2 for demonstration of imbalance. The averaged leakage inductor current is controlled to be 1A to drain 1A more for cell 1 than cell 2, as it can be seen from the Fig. 13(a). Positive phase shift also enables the power transfer from HV cells to LV system.

If the two cells in one link are of significant imbalance and the LV system is at no/low-load condition, the faster balancing speed can be achieved by utilizing C2C+LV2C. The negative phase shift and DC current that is higher than I_{cell1} result in charging the weak cell 2 at 2.13A while discharging the cell 1 and LV battery at 0.35A and 0.9A, respectively.

For the third operating mode, no relative current between the two cells is required, therefore $I_{DC} = 0$. That is, the two cells are supplying/charging LV loads/battery at the same current level 3.1A. The positive phase shift between primary switches and secondary switches is applied in order to realize the power transfer from primary to secondary. This mode is designed for the two well-balanced neighboring cells that are demanded to provide power to LV battery/loads.

Lastly, the unique C2C energy path is verified. The phase shift control is disabled to only activate the C2C path. By controlling the $I_{DC} = 2.5A$, the stronger cell 1 is discharging at 1.5A. Meanwhile, the lower-SOC cell 2 is being charged at roughly 1A. After all, four individual balancing modes are presented and validated in experiments. A higher-level controller can be installed to simultaneously operate multiple HFB links.

D. Higher-level controller with LV load regulation

The LV battery also has a preferred operating range in terms of voltage. However, the controller on each HFB has limited vision on the information of LV battery and load. It might lead to over-stressing LV battery without a systematic control strategy on when and how much to charge/discharge the LV or power the LV loads.

Therefore, a higher-level controller shown in Fig. 14. that oversees and distributes the power needed and balancing levels from/for each HFB module is installed before each HFB with its own local controller. The center controller receives SOC and state of health (SOH) statuses from an SOC estimator that could be embedded in the HFB modules, as well as the LV battery status and load condition. Based on the feedbacks, the higher-level controller determines the current references for each cell and update them with the local controller to actuate the control. During the current determination process, intelligent optimization techniques (e.g. model predictive control) can be applied to achieve the SOC equilibrium with various objectives. Three commonly referred balancing cost functions are listed in the Fig. 14.

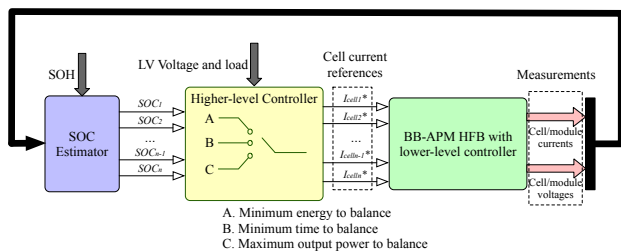


Fig. 14. Higher-level controller distributing power demands to each local controller

E. Functionality verification using real battery cells

Two 3000 mAh Li-ion nickel-manganese-cobalt (NMC) cells are installed on the HFB module as cell 1 and 2 to verify balancing operation and performance. The battery balancing is performed based on SOC feedbacks. Voltage-based feedbacks can also be used as the inputs of the HFB balancing algorithm with possible sacrifices on the balancing performance. Given the parasitic resistance/impedance of the circuit might present and voltage sensors vary in addition to cell internal resistance, the cell-to-cell voltage difference can be negligible in some cases while cells are out of balance. Therefore, balancing the cells based on the voltage difference is invalid in those mentioned cases.

An open-circuit voltage (OCV) - SOC curve for the cell is experimentally extracted to translate the open-circuit voltage to an static SOC. The continuous SOC_s are firstly obtained from fully rested cells' voltages and then updated by coulomb counting when cells are testing. The periodic OCV-SOC check is performed to prevent predicted SOC_s drifting away due to current sensor inaccuracy.

A balancing strategy that is usually found in active balancing circuit is validated first. By asking more power from strong cell and relatively less from weak cell, the SOC difference is gradually eliminated. The experimental measurements are shown in Fig. 15(a). A 10% initial SOC difference is introduced first and compensated by 1A current difference between cell1 and cell2 within 18 minutes, while keeping output power constant 20W.

Should the faster balancing speed be desired, the unique C2C energy path is utilized when LV load is light. In Fig. 15(b), during the C2C fast balance phase, cell 1 is providing the power to the LV as well as shuttling excessive energy to neighboring cell 2. It can be seen that 10% SOC difference is eliminated within 4 minutes, which is roughly 1/4 of what it takes for the previous case.

During charging phase, the balancing algorithm can also be activated. Two modes are shown in Fig. 15(c). Within first 15 minutes, the circuit intentionally enlarges the SOC difference between cell 1 and 2 by introducing a positive 1A DC bias. This period is shown to prove that the HFB module is flexible to compensate the large impedance mismatch among cells, if there is any. The rest of test is illustrating the balancing performance while charging.

It should be noted that the absolute balancing speed relies heavily on the balancing C-rate that is determined by the size of the battery pack. However, the two discussed cases clearly

show the relative speed benefit gained by using C2C in the neighboring cells.

The measured efficiencies under two modes at nominal cell voltages (3.6V) and LV voltage (12V) is given in Fig. 16. The peak efficiency (89.1%) under C2LV/LV2C is higher than other non-isolated converters [39] with GaN devices at similar power level in high-frequency conditions. The efficiency running in C2C-only mode is shown between 5-10 W, which translates to 1.4 A to 3A (0.5 - 1 C-rate for a 3-Ah cell) from one cell to another. The efficiency under C2C-only operation mode is higher than C2LV/LV2C mode as lower loss is generated from secondary switches.

F. Current ripple on battery cells

It is worth to point out the amplitude of current ripple on the battery cells, even though the battery cells are not very sensitive to high current ripple. However, to keep the operating voltage away from the max/min boundaries to which an unfiltered peak transformer current might drive due to the internal cell resistance, parallel capacitive filtering would help battery filter out high-frequency current ripples to a reasonable degree. In the experiments, two filtering capacitors with 100 μ F are paralleled with each battery cell. The current going to the battery is smoother and considered to be constant compared with transformer current, as shown in Fig. 17.

VI. COMPARISON WITH SIMILAR MODULAR BALANCING APPROACHES

As the modular design attracts more attention in battery balancing territory, there have been many researches discussed previously that utilize the modular design concept [21], [26], [27]. It would be beneficial to compare them with the proposed topology to highlight the features of proposed topology. The comparison for a battery system with 2n cells is listed in Table III in terms of components count, available balancing mode, balancing speed, converter efficiency, targeting power level and switching frequency. The balancing speed is concluded using the metrics proposed in [7]. Please note that the comparison between proposed topology and the counterparts that interact with HV-bus is pointless. The power loss is from 4.2 kW up to 26.6 kW for the HV-bus balancing topologies like the one proposed in [26], whereas the proposed topology only loses from 228 W to 456 W, assuming constant efficiency across the entire operation range. The benefits gained from redistributive balancing are reduced or even canceled out due to the additional power loss for HV-bus based balancing topologies. Therefore, in this study, only APM-based topologies are compared in simulation.

The existing APM-based balancing strategies balance the cells in two modes, i.e. C2LV and LV2C. The additional mode C2C available in the proposed topology can be achieved indirectly in the existing methodologies with paths of C2LV then LV2C. The additional power flows from cell to LV and LV to cell involve extra losses. So generally speaking, it is not efficient to apply the indirect C2C path in existing topologies. Instead, the central controller normally commands a higher current from stronger cells to compensate the total LV loads

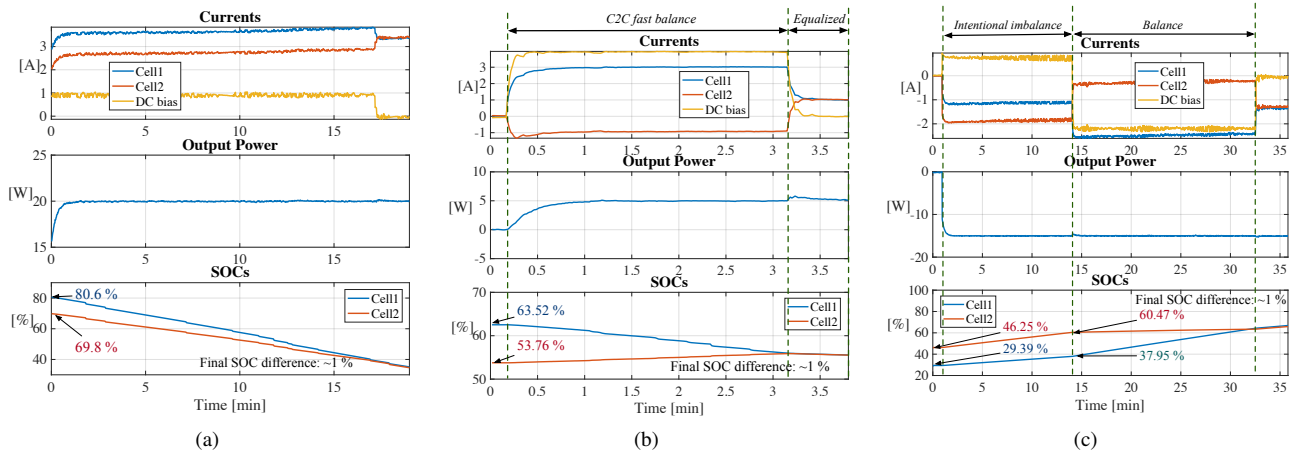


Fig. 15. Experimental balancing functionality tests on two 3000 mAh NMC cells: (a) 1A C2C current with 20W LV load, (b) 4A C2C with 5W load when balancing, (c) intentional imbalance and balance for charging

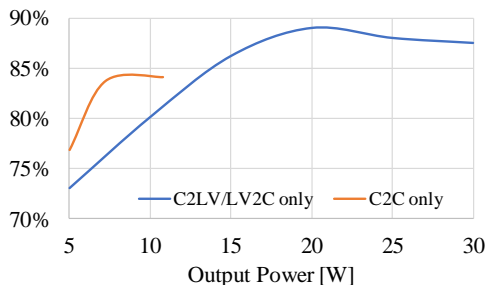


Fig. 16. The efficiency measurements of the proposed HFB module running in different modes

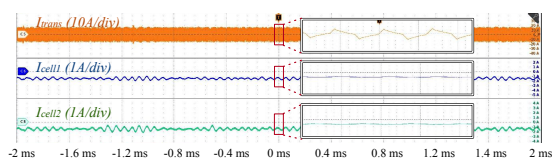


Fig. 17. Comparison between the measured cell currents and transformer current

and weak cells will be left with minimal/no interfacing with LV bus. Two equivalent circuits for proposed and existing topologies are drawn in Fig. 18 to explain aforementioned situation. The proposed topology provides an extra freedom of balancing the whole EV pack in APM-based topologies. Especially when the LV loads are fixed and cannot overload, the additional freedom of I_{DC} can be utilized to boost the balancing speed without interfering LV loads. The simulation

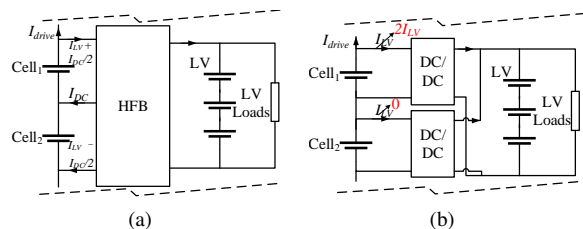


Fig. 18. Equivalent circuits for simulation using driving cycles: (a) proposed topology, (b) existing topology

of this case is shown in Fig. 19. Two UDDS driving cycles with a US06 driving cycle in between are injected to two cells composed by high-fidelity NMC battery models. The plots show that the proposed topology can provide a balancing current I_{DC} while the existing topologies are clamped by the LV loads I_{LV} . Therefore, the time to balance can be significantly reduced. In this simulation, the cells are initially unbalanced with 20% SOC difference and balanced by proposed topology and existing ones. I_{DC} is 2 A and I_{LV} is 0.5 A. In this case, the time to balance is reduced by 50%. In general, the improved time can be quantified by the following equation for imbalance of neighboring cells:

$$t_{imp} = \frac{\Delta SOC \times Cap}{I_{DC} - I_{LV}}, [min] \quad (12)$$

where the initial SOC difference is denoted as ΔSOC , average capacity of two neighboring cells is Cap in A-min. I_{DC} and I_{LV} are the applied DC bias current and LV load referred

TABLE III
COMPARISON AMONG MODULAR BATTERY BALANCING TOPOLOGIES FOR A BATTERY SYSTEM WITH 2N CELLS

Topology	Components*	Balancing modes	Balancing Speed	Efficiency	Targeting power level	Switching frequency
Proposed topology	6n/n/0	C2C + C2LV + LV2C	Fast (< 1) ⁺	89.1%	1.2 - 2.4 kW	1 MHz
DAB [21]	16n/2n/0	C2LV + LV2C	Relatively fast (< 1) ⁺	92%	1.2 - 2.4 kW	200kHz
Inductive [27]	2n/0/2n	C2C	Slow (> 20) ⁺	86%	0.5 - 2 KW	100kHz
Buck-boost [26]	4n/0/2n	C2HV+ HV2C	Relatively fast (< 1) ⁺	93%	60 - 380 kW	250kHz

*Number of power switches/transformers/inductors

⁺Number of hours to balance for a 100-cell pack under same condition [7]

to the input of the converter. Higher improvement should be observed when the LV bus is at light load, i.e. I_{LV} is small.

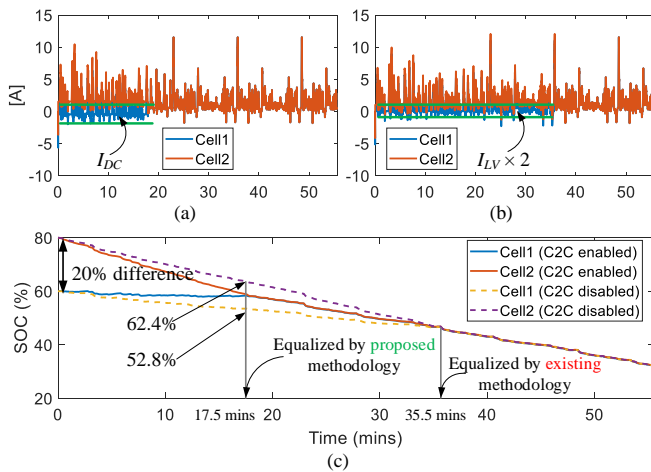


Fig. 19. Simulation results leveraging non-C2C APM and proposed methodology with combination of UDDS and US06 driving cycles: (a) cell currents with proposed topology, (b) cell currents with existing APM balancing topology, (c) comparison of balancing performance in terms of SOC

In Table III, it can be seen that the proposed topology outperforms the other counterparts in: (i) balancing speed: as the extra C2C path in addition to C2LV takes less time to balance same SOC difference compared with C2LV/HV-only techniques as shown in experimental validation; (ii) switching frequency: steps towards integration and higher power density; (iii) total power losses: it is significantly smaller compared with the series modular design that is directly connected to HV bus [26].

Besides, the proposed topology has significantly less component count compared with DAB counterpart and is comparable with the other two topologies. Further optimization can be performed to reduce the component count to 50% on switching devices by replacing full bridge with half bridge.

VII. CONCLUSIONS

A HFB converter is applied in APM based balancing circuit, which allows the isolated power transfer from HV to LV as well as balancing two cell in one half bridge. The phase shift and duty cycle control are introduced to enable bi-direction power flow and controllable C2C balancing path. The circuit operation and balancing mode realizations are explained. The design guidelines for the filtering capacitor and transformer in this topology are given to convenience the future developments. The experimental prototype is presented with self-designed converter and magnetics. The balancing performance is shown by two NMC battery cells. The unique C2C path provides significant balancing speed boost compared with the conventional cell-to-stack balancing direction at which universal isolated DC/DC converters (e.g. DAB and resonant converter) normally operate. The feasible balancing modes are validated in the prototype at 1 MHz switching frequency. The proposed topology is compared with other modular designed balancing topologies and shows promising benefits.

In the future, a slightly modified version can be investigated which reduces the number of switches to 2/cell and circuit

footprint by replacing full bridge by half bridge with minimal modifications in the design and control.

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