# Modeling and Design of A Cost-Effective Redistributive Dual-Cell Link Battery Balancer for Electrical Vehicle Applications

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# Abstract

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The electric vehicles, as the most promising solution for achieving high fuel economy, have significantly better emission profile than conventional vehicles powered by fossil fuels. However, range anxiety and the limited accessible fast-charging infrastructures mainly restrain the drivers from adopting the electric vehicles that have much higher energy efficiency. Due to the internal and external factors, the cells in the battery pack degrade differently, leading to a usable capacity that is less than the available capacity if they are left unbalanced, which ultimately shortens the driving range. Therefore, an external circuitry, i.e. battery balancing circuit, that manages the unbalanced cells is installed to maximize the usable capacity, and thus, to prolong the driving range. However, the most commonly adopted balancing circuit is the dissipative balancing strategy in the large-scale electric vehicle productions, where the available capacity is underutilized. One of the most efficient redistributive balancing strategies that overcome the drawbacks of the dissipative one is converter-based strategy that monitors and regulates each paralleled-connected cell module. Nevertheless, installing the individual DC-DC converters on each module is not cost-friendly, and thus, reducing the cost of the converter-based balancing system becomes the priority for large adoptions of the redistributive balancing systems in electric vehicles.

This thesis proposes a dual-cell link that integrates the functionalities of the auxiliary power module, battery gauging and battery balancing, leading to a low-cost solution comparable with the dissipative balancing. The topological improvements are made achieving 50% less number of the needed converters compared with the existing topologies. In addition, the integration and minimization are the design targets in terms of the main circuit components. The costly components,

such as MOSFETs and magnetic components, are curtailed by 62.5%-75% and 50% - 100%, respectively, with no sacrifices on the balancing speed. In order to achieve the magnetic integration, the detailed circuit model is developed using average- and small-signal modeling techniques. The design procedure for the half-full bridge converter with the cored transformer is firstly discussed, followed by a further minimized dual-half active bridge converter with a coreless transformer. Following the design procedure, two systems are characterized, built, tested and validated with the real batteries.

Not only is the cost reduced, but also the balancing process is facilitated, which is realized by an additional balancing path. A DC current offset between the adjoining cells in one link can be introduced to the circuit by utilizing a normally undesired volt-amp imbalance in the transformer, which provides the extra cell-to-cell balancing path. An asymmetric duty cycle control is proposed to regulate the DC current offset so that the different balancing modes can be achieved. With the enabled cell-to-cell path, the balancing speed can be reduced by 50% compared with the conventional cell-to-stack only balancing methods with a state-of-charge difference of 20% between two adjoining cells.

The auxiliary power module requires the proposed converters to work as efficiently as possible within its wide operating range. However, the efficiency of the half-bridge systems drops at light-load conditions due to the loss of the soft-switching capability and high conduction loss. In order to overcome this drawback, the variable frequency modulation is normally preferred. A conduction-loss based control criteria is proposed, inheriting the benefits of the conventional variable frequency modulation while maintaining the optimized conduction loss. It is validated on the converter prototype that the proposed control criteria can achieve 1-2% better efficiency with an extremely simple but robust control logic compared with the critical soft switching.

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# Acronyms

**AC** alternating current. 18, 49, 63–65, 71–73, 139, 141, 172

**ADC** anolog-to-digital converter. 162, 163

**AP** area product. 58–60

**APM** auxiliary power module. 6, 18, 19, 21, 23, 25, 159, 162, 165, 166, 171, 172

**BB-APM** battery-balancing auxiliary power module. 4, 6, 21–23, 25, 94, 96, 97, 117, 131, 159, 162, 165, 166, 169

**BMS** battery management system. 6, 12, 18–21, 23, 159, 162, 165, 166, 171

**C2C** cell-to-cell. 4, 6, 26, 33, 44–48, 53, 55, 64, 75, 81, 85, 87, 88, 90, 92, 93, 96, 130, 137, 169

**C2LV** cell-to-LV. 45, 48, 53, 90, 127, 130

**CFM** constant frequency modulation. 156–158

**CO2** carbon dioxide. 1

**DAB** dual-active bridge. 4, 5, 7, 24, 39, 92, 98, 132, 166–168, 171

**DAHB** dual-active half bridge. 5–7, 94, 97, 98, 116, 131, 132, 155, 159, 166–168, 170–172

**DC** direct current. 4, 14, 18, 19, 21, 30, 33, 35, 37, 49, 63, 64, 71, 72, 75, 96, 127, 128, 135, 136, 141, 163, 169, 172

**DOD** depth of discharge. 17

**ECM** equivalent circuit model. 26, 33, 98, 99

**EMI** electromagnetic interference. 95

**EOL** end of life. 15, 169

**EV** electrical vehicle. 2, 3, 5, 6, 18–20, 23, 52, 159, 160, 163, 165, 167–169, 171

**FEA** finite element analysis. 6, 7, 65, 120, 127, 170

**GHG** greenhouse gas. 1

**HFB** half-full bridge. xvi, 4–7, 25, 41, 52, 53, 75, 92, 94, 96, 97, 110, 131, 132, 137, 143, 159, 166–171

**HV** high voltage. 14, 18, 21, 24, 25, 32, 36

**ICE** internal combustion engine. 2

**LS** least square. 67, 110

**LUT** look-up table. 132, 137, 140, 147, 148, 170

**LV** low-voltage. 4, 5, 18, 21, 24–26, 29, 32, 36, 37, 49, 54, 75, 118, 119, 127, 128, 148, 155, 172

**LV2C** LV-to-cell. 45, 46, 48, 53, 90, 128, 130

**MLT** mean length per turn. 64

**MMF** magnetomotive force. 121

**MPPA** maximum power per ampere. 5, 7, 146–158, 170, 171

**NMC** Nickel-Manganese-Cobalt-Oxide. 170

**OC** open-circuit. 74

**OCV** open-circuit voltage. 11, 12

**OEM** original equipment manufacturer. 20, 159, 160, 166, 167

**P2P** peak-to-peak. 30, 113, 135

**PCB** printed circuit board. 60, 61, 63, 64, 71, 95, 125, 126, 171, 172

**PP** pre-preg. xiv, 123

**PPA** power per ampere. 146, 149, 154, 158

**PS** primary side. 30, 36

**pu** per-unit. 118

**PWM** pulse-width modulation. 25, 33

**RMS** root mean squired. xiv, 44, 45, 60, 63, 72, 73, 103, 111–113, 116, 121, 128, 131, 137–139, 141–143, 145, 146, 152, 157, 158, 170

**SC** short-circuit. 74

**SOC** state of charge. 8, 10–13, 15, 17, 20, 36, 54, 55, 110, 119

**SS** secondary side. 36

**VA** volt-amp. 30–33, 40, 169

**VFM** variable frequemcy modulation. 5, 7, 132, 137, 138, 140, 152–154, 156–158, 170, 171

**ZVS** zero-voltage switching. 7, 113, 120, 132, 133, 135–139, 153, 154, 157, 170

# Chapter 1: Introduction

## 1.1 Background

"Human influence in climate has been the dominant cause of observed warming since the mid-20th century", concluded by the Intergovernmental Panel on Climate Change. As the most significant factor, greenhouse gas (GHG) is the side product of burning fossil fuels for electricity generation and transportation. In 2016, a sustainable carbon dioxide (CO2) concentration level in the atmosphere has been violated, which is believed to be catastrophic for our environment.

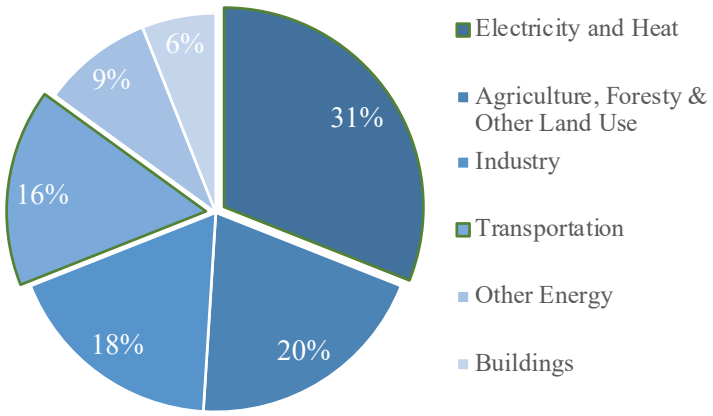



Figure 1.1: The global greenhouse gas emissions by economic sector [1]

A global GHG emission report in 2016 describes the sources and activities across worldwide economy where GHG is produced [1], as shown in Fig. 1.1. It shows that the energy-related activities generates roughly 50% of the entire GHG emissions, which includes transportation and electricity generation. Mitigating or ideally eliminating the emission of GHG from these two sectors requires the adoption of the transportation electrification and the renewable resources [2].

To regulate and boost the transportation electrification, the U.S. government has issued new fuel

economy standards where the average fuel economy of passenger vehicles and light-duty trucks is required to increase to 54.5 mi/gal (4.3 L/100 km) by 2025 [3]. The internal combustion engines (ICEs) currently have less than 30% efficiency [2], which makes complying with the fuel economy regulation by 2025 infeasible.

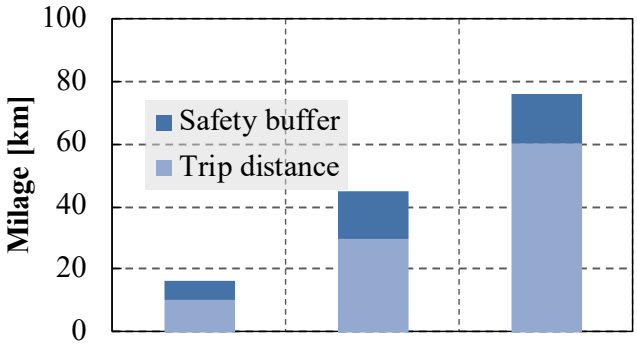



Figure 1.2: The trip distance vs. extra driving buffer due to range anxiety [4]

Alternatively, power electronics, electrical machines and energy storage systems provide significantly higher efficiency. As a result, the electrical vehicle (EV) is considered as the most promising solution. However, the bottlenecks of the EVs are not easy to be ignored either. The driving range anxiety has been one of the concerns that the EV users have. Around 46% of the EV drivers claim that the range of the EVs is not sufficient from [5]. A survey about the range anxiety and safety buffer that the users would leave for driving a EV was performed in [4]. It shows that the drivers limited their driving behaviors due to the range anxiety, such as reducing driving speed and rearranging the route to pass by charging stations. In addition, drivers would spare safe mileage buffer when they decide to drive the EVs. That is, the extra mileage (up to 65% more than what they need) needs to be available before driving comfortably, as shown in Fig. 1.2. On the other hand, the charging speed is also demanding to indirectly relieve the driving anxiety. Nearly 50% of EV owners suggest a faster charging would improve the EV charging experience most profoundly [5].

In order to improve the driving range, a larger battery pack is the straightforward solution, but it is often space-constrained. Instead, efficiently utilizing the available energy is the only

solution without increasing the battery pack capacity. Due to the variations of the manufacturing process and the temperature deviation when operating, the battery cells experience an effect called imbalance, leading to reduced driving range. As the battery cells degrade, the imbalance effect becomes more profound. In order to reduce the imbalance effect to its minimum and prolong the battery life, battery balancing needs to be implemented.

## 1.2 Motivations and challenges

The consequences of cell imbalance on the battery, which will be elaborated in the following chapter, unavoidably mandate battery balancing. The most commonly used technique for Li-Ion battery packs in the EV application is resistive balancing due to its low cost and effectiveness. However, the efficiency is extremely low as it is wasting excessive energy dissipating to the bleed resistors. In particular, the usable battery pack capacity is reduced if the cell imbalance is severe, leading to lower driving range. On the other hand, the redistributive balancing strategies shuffles the excessive energy and completely utilizes available pack capacity. But they are cost-ineffective so that implementing them is currently infeasible for mass production.

Among the redistributive balancing techniques, the converter-based solution is the most promising one due to their flexibility and efficiency. Although there are several attempts in the literature, reducing its cost is still challenging. In particular, every block of parallel-connected cells requires a converter to realize the balancing process, which not only takes up limited spaces but also increases the cost of the entire balancing system. Unless there are technological breakthroughs to lower the cost, the redistributive balancing methods remain unappealing.

## 1.3 Contributions

The study proposes several original and novel contributions to the existing research and development of the redistributive battery balancing in EV applications. All of them aim to produce a cost-effective solution for active balancing and they are verified in laboratory environment. They are elaborated as follows:

- **Novel topology for low-cost redistributive balancing:** The battery-balancing auxiliary power module (BB-APM) concept is significantly improved by proposing a half-bridge isolated topology. The advantages of this proposed circuit are not only introducing a direct path for balancing neighboring cells, which accelerates the balancing process if the imbalance is severe between the neighboring cells; but also reducing the required number of the individual converter for each cell/module by 50%. In other words, every two cells which conventionally require two converters now only need one converter. Applying the proposed topology inherently reduces the cost by half.

- **Precise circuit model and tailored control logic:** Unlike the usual balanced inputs, the unbalanced cells as the inputs of the half-full bridge (HFB) lead to the catastrophically diverging current. The detailed circuit modeling reveals the diverging current can be controlled by the proposed asymmetric duty cycle control. In addition, the asymmetric control provides a means to regulate the cell-to-cell (C2C) current. Therefore, the proposed topology can be operated at all balancing modes as other existing topologies, along with the unique path for C2C balancing.

- **Extra balancing mode:** Thanks to the tailored control logic, a direct current (DC) offset can be introduced between the two cells in one link. It can be regulated to any arbitrary reference. Even though the net power is flowing to low-voltage (LV) side, the DC offset can be set to force one cell to charge another cell in one link, leading to 50% faster balancing process according to the long-term simulation.

- **Lowered number of magnetic devices:** The conventional dual-active bridge (DAB)-based converters consist of a discrete inductor for energy transfer and a transformer for galvanic isolation. In this study, the transformer is carefully modeled and analyzed so that the inductor is integrated in the transformer. Therefore, the magnetic device is curtailed by 50%. The design steps and considerations are explained based on output power capability.

- **Further improvements on the novel topology:** Based on the HFB development, the further

simplification is performed on the elimination of the core material that is normally cost-ineffective. The full bridge on the LV side is replaced by a half bridge, leading to a fully symmetrical topology, named as dual-active half bridge (DAHB). As a result, the cost of the active balancing system can be further reduced by 33% on the power MOSFETs and 100% on the magnetic material. However, removing the core from the transformer complicates the system model as the magnetization inductance cannot be neglected. This study analyzes the effects of the imperfect coupling, and proposes the complete circuit modeling considering coupling factor. Based on the developed models, the coreless transformer prototype has been designed and validated.

- **Improved efficiency at low load condition with simplified variable frequemcy modulation (VFM):** The conventional VFM that achieves soft-switching requires the entire knowledge of the components, e.g. MOSFETs parasitics and transformer losses, leading to the optimal operating conditions. However, a sophisticated loss model is needed to locate them. As a result, implementing this kind of control logic is infeasible in real-time embedded systems. Observations of the efficiency measurements inspired a simplified criteria named as maximum power per ampere (MPPA). The proposed MPPA-VFM method only needs to solve a linear equation along with a frequency controller, such as a PI controller. It is drastically simplified to implement on an embedded system compared with the conventional VFM without the noticeable efficiency sacrifice. It is also verified to improve the efficiency against critical soft-switching which is also computational-intense.

- **Achievable low cost:** The cost breakdowns on each component for two proposed topologies are presented. As the number of units being produced increases, the redistributive balancing applying DAHB and HFB is achieved "free of charge" with a reasonable number of EVs sold. On the other hand, conventional DAB barely approaches the $4.2/cell-budget to achieve complimentary battery balancing. In addition, the simplification from HFB to DAHB reduces the needed number of units to achieve "free" redistributive balancing by at

least 80%.

## 1.4 Thesis outline

The thesis presents the detailed circuit design, modeling, controller design and validation of the proposed cost-effective redistributive balancer as well as its cost analysis. This study is organized as follows.

Chapter 2 elaborates the causes and consequences of the battery pack imbalance. The dissipative balancing and redistributive balancing are explained and compared in terms of the balancing speed and circuit complexity. The improvement on driving range of implementing redistributive balancing is highlighted. With the guidance of the road map on auxiliary power module (APM) and battery management system (BMS) in modern EV systems, the technical and financial targets for BB-APM are demonstrated. In addition, the functionalities of BB-APM are defined to guide the design of BB-APM circuitry.

Chapter 3 presents the HFB topology for redistributive balancing. The detailed circuit operations are explained, leading to a transformer current drift effect. An asymmetric control is proposed to overcome the drift effect and used to realize the C2C balancing mode. The average and small signal modeling techniques are applied to obtain the system model to design the PI controllers regulating the output power and cell currents. Integrating the discrete inductor into transformer leads to a careful design of the transformer based on the power and soft-switching capability. Theoretical calculation and finite element analysis (FEA) simulation are conducted to guide the transformer design. A fully self-designed prototype is verified and the long-term balancing is validated on the actual battery pack, showing all feasible balancing modes and improvements over the conventional topologies.

An improved minimal DAHB configuration is proposed in Chapter 4 based on the HFB topology. Due to the elimination on the magnetic cores, the system models change completely. The updated power and current models are derived considering the coupling factor of the coreless transformer. The iterative design process is proposed to finalize the transformer parameters us-

ing FEA simulations. The prototype equipped with the coreless transformer and minimal DAHB configuration is tested to show all balancing modes function.

Chapter 5 proposes a computation-friendly VFM to improve the system efficiency at low load conditions implementing soft switching. The zero-voltage switching (ZVS) requirements for the primary and secondary power MOSFETs are derived to achieve the critical soft switching. An observation on the efficiency curves reveals a simple factor that determines the system losses. The theoretical analysis is conducted to validate the observation and produces a linear mathematical solution to find the optimal VFM operating points, so called MPPA points. The proposed MPPA-VFM method is able to operate the system at the pseudo-optimal efficiency range, which is validated on the prototype test bench.

In Chapter 6, the cost analysis of the two proposed configurations, DAHB and HFB compared with conventional DAB, is conducted based on the number of units produced, i.e. prototype, batch and mass productions. Component selection guidance is given to optimize the unit cost.

Lastly, the study is concluded and the future works are discussed in Chapter 7.

# Chapter 2: Battery Charge Equalization and Solution for Low-Cost Balancing Circuit

When the cells that are connected in series have significant charge difference among them under the same load condition, this phenomenon is called the imbalance of the battery string/pack. The unbalanced battery string/pack can neither be charged or discharged once one of the cells is fully charged/discharged as the cells are protected from overcharging and discharging [6]. Regardless of cell capacity differences, a simplified phenomena has been illustrated in Fig. 2.1, which is assumed that the cells are out of balance in terms of state of charge (SOC). It can be seen from the plot that the cells are not completely drained to the same level when discharging the unbalanced pack, leading to an under-utilized pack capacity. The discharging process is terminated since all the cells are protected from over-discharging where a voltage below minimum allowable voltage occurs. In other words, the driving range will decrease because the energy that is intended to be consumed still remains in some of the cells. In addition, the cell 1 and 2 are not fully charged even though cell 3 has been at full charge. The under-utilized capacity will persist until the scenario becomes worse. Furthermore, a more complicated scenario when the cell capacities diverge results in even lower pack capacity utilization. Therefore, in order to correct the imbalance and fully utilize the available capacity of the battery pack, the excess energy in strong cells needs to be managed, i.e. a balancing strategy should be implemented.

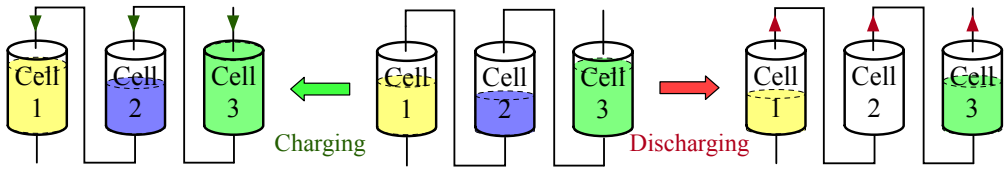



Figure 2.1: The consequences of charging or discharging unbalanced battery cells in series connected configuration

Unlike the natural chemical process that the Lead-acid and Nickel-based batteries leak gas when overcharged, overcharging Li-Ion batteries will cause irreversible damage [7]–[9]. Therefore, Li-Ion batteries require the external controllers and circuits to monitor and regulate the battery behaviors in order to make them operate properly and well balanced. Typically, the balancing strategies can be categorized to the passive and the active balancing. The balancing strategy is categorized as active balancing when the intelligent control is engaged to regulate the balancing process.

## 2.1 Battery balancing

### 2.1.1 Passive balancing

Conversely, if the balancing operates without any control action, it is passive balancing. For example, the paralleled bleed resistors that always connect to the cells will slowly balance the cells, as shown in Fig. 2.2. According to Ohm's Law, the cells that have higher potential will naturally discharge faster than those that have lower potential and eventually have the same potential over the entire pack. However, the balancing constantly operates even when the cells are balanced. The operation of balancing with the bleed resistors also relies on the voltage differences among the cells. The resistance should be selected wisely. If the resistance is too high, it is time consuming to correct the critical imbalance. If it is small, the energy is wasted. Clearly, the efficiency of the passive balancing is relatively low as the energy is always wasted [8]–[10]. In addition, the balancing constantly operates even when the cells are balanced [11].

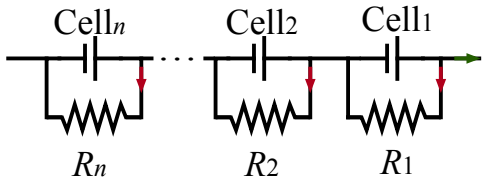



Figure 2.2: The passive balancing strategy - excess energy is dissipated in the paralleled resistors

### 2.1.2 Active balancing

As one of the advantages of active balancing, the balancing process can be carefully controlled instead of applying the balancing strategy in open-loop, and thus, undesired energy waste can be minimized. The controlled balancing process is further divided into the dissipative balancing and the redistributive balancing.

**Dissipative balancing**

The excessive energy is dissipated through the resistors in a form of heat [7], which is similar with aforementioned passive balancing but in a controlled fashion using relays/switches [9], [12], as shown in Fig. 2.3. Even though the accurate SOC estimation is not mandatory for the dissipative balancing that can operate based on voltage, it complicates the thermal design since the resistors generate heat [13] and suffers from low efficiency.

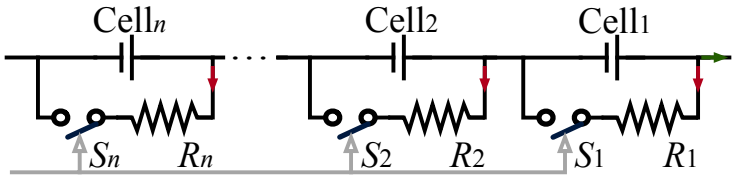



Figure 2.3: The dissipative balancing strategy - excess energy is dissipated in the paralleled resistors by active control

The dissipative balancing is applied to the same battery pack shown in Fig. 2.1, yielding a result illustrated in Fig. 2.4. If the bleeding resistor is selected properly, during charging, the balancing is engaged and it guarantees the pack is fully charged. Due to the energy conservation, the result of discharge remains the same.

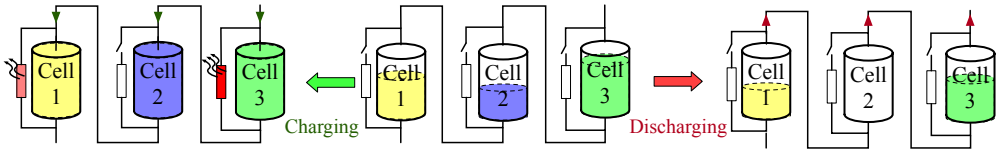



Figure 2.4: The balancing results utilizing dissipative balancing strategy

### Redistributive balancing

The redistributive balancing is proved to be the more efficient approach by shunting the energy from stronger cells to weaker cells, such that the full capacity from the battery pack can be utilized [8]–[10].

The redistributive balancing consists of a temporary energy buffer, e.g. inductors and capacitors, that absorbs the excessive energy from strong cells and releases it to weak cells. As a result, all the cells' SOCs are maintained at a similar level. Detailed topologies to realize redistributive balancing will be discussed later. The expected balancing results of using redistributive balancing is illustrated in Fig. 2.5. As the excessive energy can be shuffled around, all the cells can be simultaneously discharged and charged, leading to fully-utilized capacity.

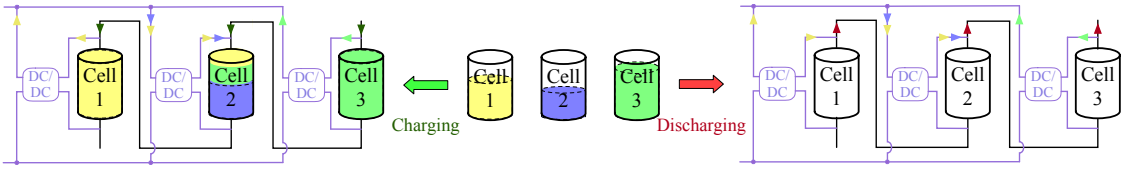



Figure 2.5: The balancing results utilizing redistributive balancing strategy

However, single-inductor/capacitor configuration that is relatively cost-effective can only balance one cell at a time while leaving other cells diverge. It brings the serious drawback of this method — slow balancing speed. Even though the multi-winding inductor or multi-capacitor can ease the aforementioned problem of the single inductor/capacitor, in practice the fact that how many windings can be designed in a magnetic core limits the applications of inductive method. This will only allow the strategy to be implemented in small battery packs instead of large ones in EV or grid-tied applications. On the other hand, the capacitive configuration is highly dependent on the voltage difference between cells so that small voltage change within a relatively large SOC range in Li-ion battery makes the capacitive method hardly functional. Therefore, the capacitive method is not suitable for those Li-Ion chemistries that have fairly flat SOC-open-circuit voltage (OCV) curves.

In addition, all aforementioned methods are relatively ineffective when the battery pack is un-

balanced in terms of the impedance. As the battery ages, the cells demonstrate different internal resistance growths that will cause exceptionally diverse voltage drops on each cell/module terminal. For the BMS that protects the battery pack based on voltage limitations, the normal operation of the battery pack will be terminated if any voltage limitations are reached, such as maximum voltage or minimum voltage. The Fig. 2.6 is a straightforward example that shows five cells under the same current load exhibit different operating voltage ranges. It can be seen that the $cell_4$ with smallest OCV/SOC reaches the maximum voltage limitation when charging before $cell_3$ that is expected to trigger the voltage protection because it has higher SOC. This phenomena is caused by the higher internal resistance that $cell_4$ has, which further leads to not fully charged battery pack and less available power and energy. When discharging, the available energy will be limited by either the highest resistance cell or the cells with smallest capacity [14], so the utilizable energy might be even lower if no action is taken.

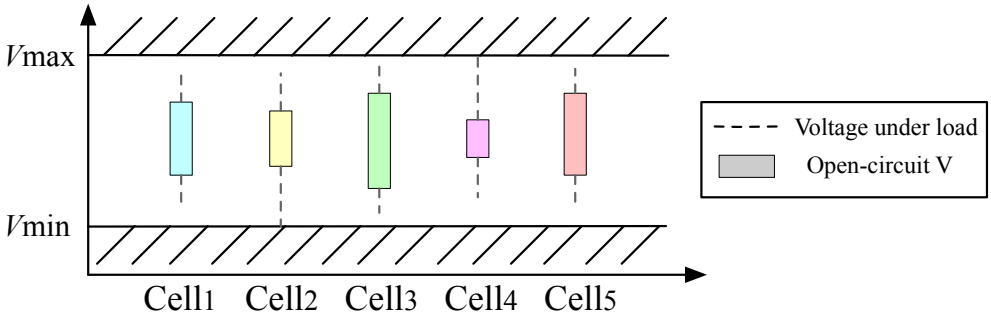



Figure 2.6: Early triggered protection due to the impedance mismatch

### 2.1.3 Existing redistributive balancing topologies

**Capacitor- and inductor-based**

There are extensive researches on the redistributive mechanism [8], [9], [12], [15]–[17], especially switched-capacitor [18], [19] and switched-inductor (or multi-winding transformer) [8], [20]–[22] due to their simplicity. However, transferring excessive energy from top cell to bottom cell is time-consuming as the energy needs to go through every single cell in the string [9]. In other word, the switched-capacitor/inductor configuration takes long time to balance a large bat-

tery pack and sensitive to how the imbalance distributes in the battery pack. In particular, another disadvantage for capacitor-based balancing strategy is that the balancing mechanism relies on voltage difference as explained previously. The nature of capacitor-based balancing utilize the voltage difference to generate the current. In the cases where the voltage barely changes while SOCs could differentiate more than 10%, the capacitor-based hardly operates properly.

**Converter-based**

The converter-based redistributive balancing can overcome the aforementioned concerns that capacitive and inductive balancing faces. It also enables modular design and is generalized enough to be installed in most energy storage systems. The converter-based method is more advanced and provides full controllability of each cell/module by paralleling the individual DC/DC converters with the battery cells. With controller rules based on accurate SOC and impedance estimations, the individual converters can arbitrarily and intentionally unbalance the cells to the SOC ranges where the unnecessary violations of the voltage limitations can be avoided, thus the full available energy can be utilized. For example, the operating SOC range of cell 4 can be adjusted to lower such that the voltage will not reach maximum before others while charging. It is another advantage of the converter-based balancing methodology that the battery pack is always controlled to operate at the optimal state. Besides, the balancing speed is considerably faster than the other counterparts mentioned previously. It will actively monitor the cells' statuses and adjust the load on each cell to drain the battery pack at the same pace regardless of the capacity variation/impedance variations.

However, the cost of the converter-based balancing circuitry is the obstacle for it to be implemented in practice. Therefore, many attempts have been made by the researchers to reduce the cost and modularize the circuit. There are two major approaches to achieve modular design: the series [23] and parallel modular designs [17], [24]–[27]. They are categorized by the bus with which the converters are linked: series modular or parallel modular designs, as shown in Fig. 2.7. The parallel modular design has a shared voltage bus that has an amplitude of the output voltage. Should higher output power at rated bus voltage be required, stacking more cells with paralleled

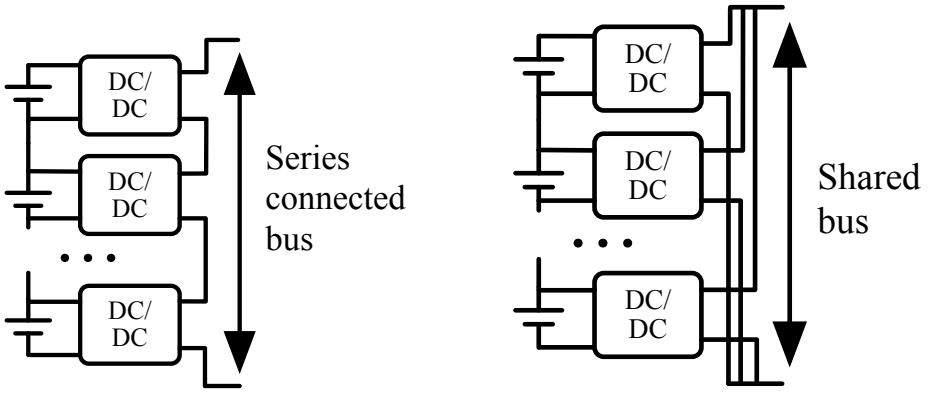



Figure 2.7: Converter-based battery balancing structure: (a) series modular design, (b) parallel modular design

converters is straightforward. However, in the case of high output voltage required (e.g. EV high voltage (HV) bus), high step-up voltage conversion from cell-level to HV bus puts extra stress on circuit design. On the other hand, the series modular design releases the burden on voltage conversion ratio as it can bank up several modules to achieve high voltage. Nevertheless, if higher output power is required without leveling up the output voltage, the DC/DC converter needs a re-design. The summarized comparison among the aforementioned techniques is given in Table 2.1.

## 2.2 Benefits of redistributive balancing

The most significant benefit of the redistributive balancing is the improved utilization of the available energy stored in the battery pack [16], [28]. In the battery pack that is equalized by the

Table 2.1: Comparison of the major balancing techniques

| **Attributes** | **Passive** | | **Active** | | |
|---|---|---|---|---|---|
| | Natural | Resistive | Inductive | Capacitive | Converter based |
| Method | Gas leaking | Heat generation | Shuttling energy | | |
| Applicable to | Lead-acid<br>Nickel based battery | Most battery chemistries, e.g. Li-ion batteries | | | |
| Advantages | Cost-effective | - SOC not needed [13] | - Less complex control [21] | - Straight-forward [15]<br>- Modularizable [9] | - Fault tolerance<br>- Cell-level BMS<br>- Modularizable [17], [23]–[25] |
| Disadvantages | - Low efficiency<br>- Causing over/under charging | - Complex thermal design<br>- Only charging<br>- Low efficiency | - Impractical for large battery pack<br>- Only one cell at a time [17]<br>- Slow [16] | -Relying on voltage difference<br>- Slow [16] | Cost-ineffective |

dissipative balancing strategy, the pack capacity is limited by the minimum-capacity cell/module [16], [28] assuming the same initial SOCs, as the 'weakest' cell will be depleted and trigger the voltage protection [14] with energy left in other relatively 'stronger' cells.

### 2.2.1 Quantified life improvements

To quantify the life time improvements using redistributive balancing in both first and second lives, four previously published data sets [29]–[32] and the self-collected cycling data on Nickel-Manganese-Cobalt-Oxide (NMC) cells where the capacity variation is captured during the same testing condition are visualized in Fig. 2.8. Each data set consists of more than 10 cells with similar initial capacities, cycled under approximately same testing conditions (e.g. temperature, current). The capacity deviation is unexpectedly severe, including worst 1000 cycles difference in [31], as shown in Fig. 2.8(c). Due to the incomplete data at high cycle number for strong cells, necessary extrapolation is applied to project to the range where the average capacity reaches the end of life (EOL) capacity (assumed 80% of initial capacity in EV application depending on the EOL definition).

If dissipative and retributive balancing are applied to the battery cells at certain age stage, the available capacity and remaining useful life seen by them are completely different. For example, if both balancing strategies are applied to the battery pack in Fig. 2.8(a) at 80% normalized capacity of the weakest cell, the dissipative one will not meet the 80% EOL requirement because the available capacity is limited by weakest cell. However, the redistributive balancing can still operate and expand usable capacity to roughly 90%. Compared with the dissipative balancing where the limiting factor is the minimum-capacity cell, the life time can be extended by 6.25% - 36% by redistributive balancing since the usable capacity for redistributive balancing is the average capacity of all series-connected cells. Even more life time can be gained if the EOL definition is lower than 80%. The Fig. 2.9 assumes redistributive balancing is applied to diversely aged packs extracted from literature [29]–[32] and the self-collected NMC data. They show the life time extension and increased capacity utilization within 40% capacity loss of the weakest cell, which reveals the sig-

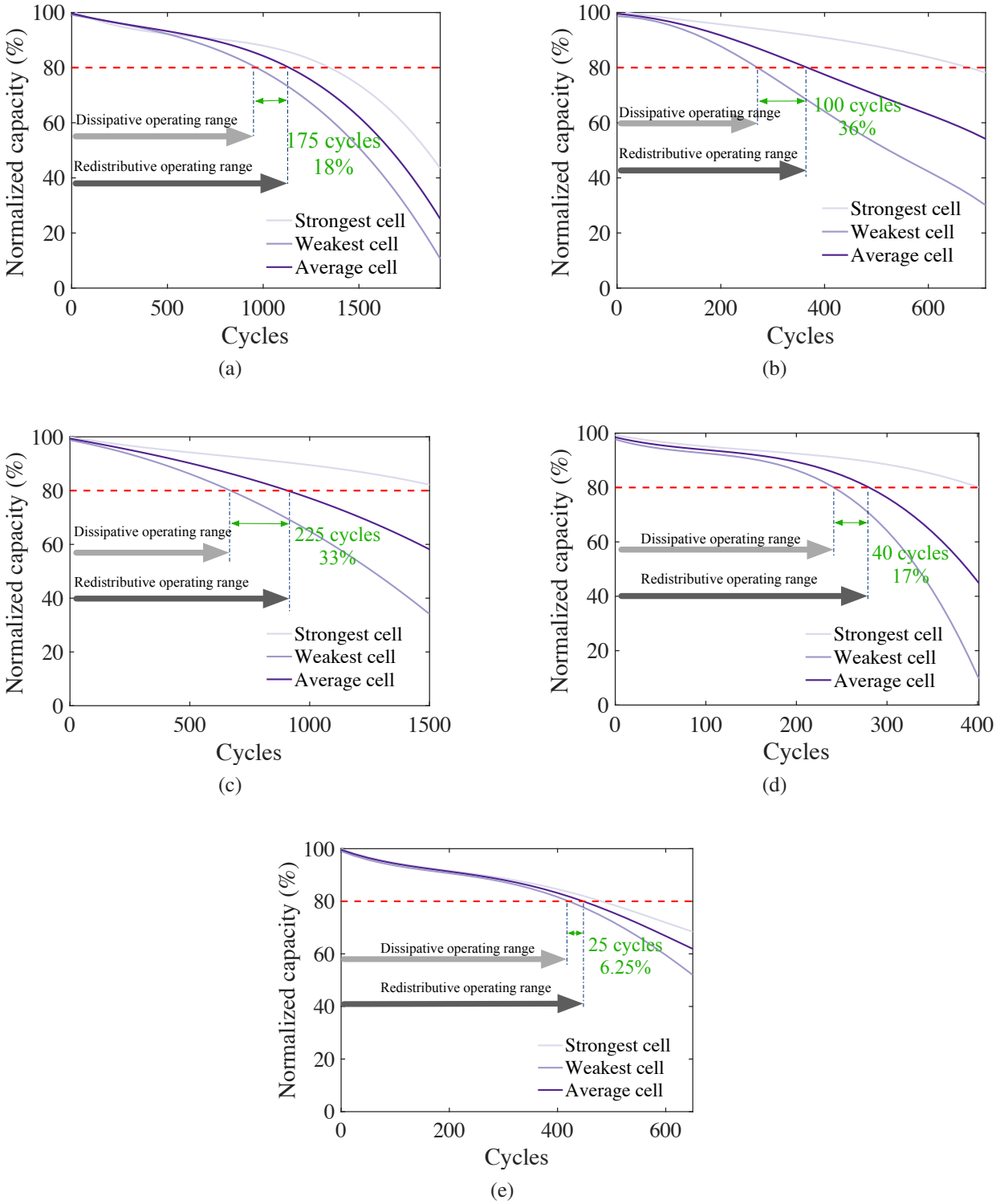



Figure 2.8: Conservative projected life extension of using redistributive balancing in EV application based on cycling data from (a) [29], (b) [30], (c) [31], (d) [32] (e) NMC cycling data

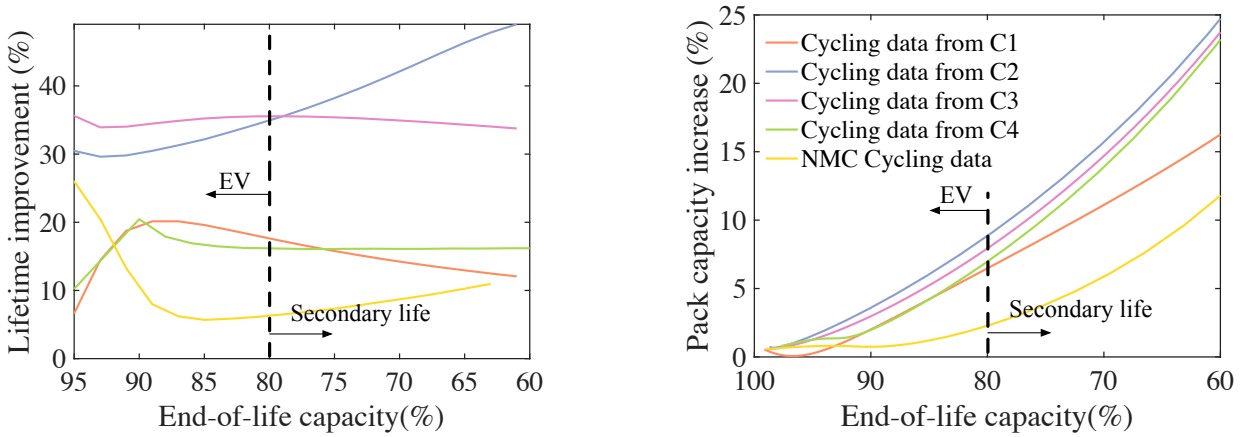



Figure 2.9: The benefits of redistributive balancing in (a) life extension within 40% weakest cell capacity loss, (b) increase of pack capacity utilization within 40% weakest cell capacity loss. C1: [29], C2: [30], C3: [31], and C4: [32]

nificant improvements across not only EV but all possible secondary-life applications. In addition, there has been researches showing that the life time improvement by using redistributive balancing techniques can be as high as 21% compared with passive/dissipative balancing [33]. In addition, the usable energy is also reported to improve by maximum 23% and 7% for small-Ah and large-Ah packs [21], respectively. Therefore, the benefits of redistributive balancing are hardly convinced to be negligible.

### 2.2.2 Slowed aging trend

Given previous statistic analysis based on existing literature, it shows obvious benefit of applying redistributive balancing in an unbalanced battery pack in terms of capacity variation. Furthermore, as explained, a well-balanced battery pack may suffer from a slower or less degradation since the extreme cells are stressed equally as the other nominal ones.

The disadvantage of using dissipative balancing is that the balancing function will not be activated during discharging, or it is not fast enough to balance the cells into a balanced equilibrium before cutoff. Therefore, the cells will end up with different depth of discharges (DODs) assuming they are discharged from the same SOC point after a fully charged cycle. It has been shown that

the DOD has a great impact on the cell aging characteristics [34]–[36].

Unlike the dissipative balancing that is only active when charging, the cells will be discharged at the same C-rate instead of the same current amplitude, so that the cells will be reaching the predefined cut-off SOC threshold simultaneously. That being said, there should not be a single or a few cell(s) that trigger the shut-down procedure of the the pack as they are fully depleted while the other cells have, for example 20%, more SOC in them. The repetitive over-stressing will leads to faster aging as mentioned previously.

## 2.3 Battery-balancing auxiliary power module

Every vehicle that is equipped with air conditioner, radio and powered steering wheel needs a LV system. Unlike the conventional gasoline/diesel vehicles that power the LV systems by the mechanically driven alternators, EVs do not have internal combustion engine. In addition, the compressor used for air conditioning and power steering pump are not available to EV. Instead, the DC or alternating current (AC) motor has to be used as the replacement of the mechanical compressor [37]. Therefore, a voltage converter is installed to step down the traction battery pack to 12 V system and provide the power required for LV applicants, which is called APM. The simplified architecture of the EV power train and BMS is illustrated in Fig. 2.10.

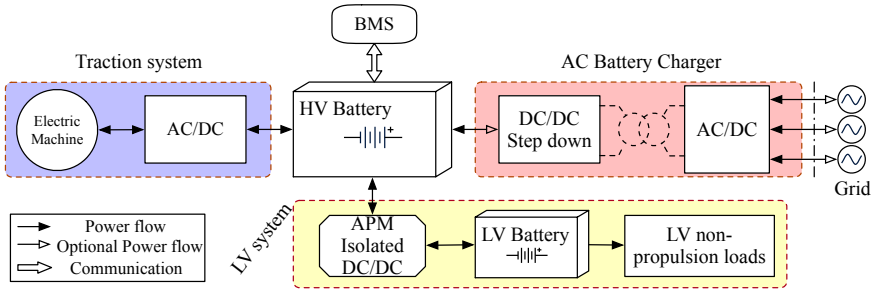



Figure 2.10: The simplified EV architecture

### 2.3.1 Technical road map for APM

The report from U.S. DRIVE [38] lists the technical targets for the EV's electrical systems, such as electric traction drive system, HV power electronics, motors as well as DC/DC converters. APM

is currently belonging to DC/DC converters and regulated by the targets of the DC/DC converter. The targets for 2020 and 2025 have been summarized in Table 2.2. The metrics are normalized with respect to cost per kilowatt and power density.

Table 2.2: Technical targets for DC/DC Converter

| DC/DC converter targets | 2020 | 2025 |
|---|---|---|
| Cost [$/kW] | <50 | 30 |
| Specific power [kW/kg] | >1.2 | 4 |
| Power density [kW/L] | >3.0 | 4.6 |
| Efficiency | >94% | 98% |

The current APM power required for EV is up to 3 kW of 12-14 V LV according to [38] as of 2017. However, the power is dependent on the auxiliary equipment (e.g. heated seats and entertainment systems) and vehicle architectures. Due to the development of autonomous driving, there is significant increase on the LV power consumption of the relative components/systems, such as visual data collection system and powerful post processing units. The rated power for APM is expected to increase up to 5 kW by sometime between 2020 and 2025.

### 2.3.2 Cost of the BMS and APM

The cost breakdown for each component in EV is normally considered as confidential and hard to find. There are few literatures summarizing this information, but one report from UBS Evidence Lab [39] stated the detailed cost for Chevy Bolt, which is summarized in Table 2.3. The applicable areas from Chevy Bolt are compared with 2020 and 2025 targets. The DC/DC converter (APM) as of 2017 Chevy Bolt is $179 which satisfies the 2020 target. To achieve less than $150 requirement by 2025, additional 20% cost reduction is needed.

Even though cost analysis of other EVs cannot be easily accessed, the author believes that the similar number would be expected. Therefore, the combined cost of a BMS and APM is around $400 and potentially more expensive as the market sharing of Chevy Bolt is statically larger.

Table 2.3: The cost breakdown of Chevy Bolt vs. 2020 target [39], [40]

| Component | Cost [$] | 2020 Target [$] | 2025 Target [$] |
|---|---|---|---|
| Battery cell | 8,700 | N/A | 5,400 |
| BMS (w/ resistive balancing) | 222 | N/A | N/A |
| DC/DC Converter (APM) | 179 | <250 (5kW) | <150 (5kW) |
| Electric drive module | 1,200 | 705 ($4.7/kW) | 495 ($3.3/kW) |
| Inverter | 697 | ($3.3/kW) | 523 |
| On-board charger (excl. fast-charge option) | 273 | 360 (7.2 kW) | 252 (7.2 kW) |
| Power distribution module | 328 | N/A | 295 |
| Vehicle interface control module | 93 | N/A | 84 |

### 2.3.3 Market price of the commercially available BMS

The redistributive balancing is rarely applied in the existing EVs while most of them is using only dissipative balancing in the BMS, including Chevy Bolt. In order to evaluate the cost of the state-of-art BMS with redistributive balancing, few options on the market either commercially available or for evaluation only are reviewed and listed in Table 2.4. On the other hand, not every original equipment manufacturer (OEM) is capable of developing its own BMS, so many of them would potentially seek the commercial BMS solutions on the market. Therefore, the conventional BMSs with traditional dissipative balancing are also investigated. It is also intriguing to evaluate the commercially available BMSs for a fair comparison with the proposed concept in this study.

Table 2.4: Market price for commercial BMS

| Manufacturer/Model | Featured Functions | Cell Configuration | Market Price [$] | Notes |
|---|---|---|---|---|
| Orion/BMS2 [41] | Balancing<br>SOC estimation<br>Cell monitoring | 96 cells<br>(up to 180 cells) | 1,225 ($12.7/cell) | Passive balancing<br>(activated only when charging) |
| Renesas/ISL78714 [42] | IC package<br>Balancing<br>Cell monitoring | up to 70 cells | 324 × 5 = 1,620 ($27/cell) | External balancing circuit needed<br>(built-in drivers) |
| STMicroelectronics/L9963 [43] | IC package<br>Balancing<br>Cell monitoring | 14 cells<br>(8 for 96 cells) | 175 * 8 = 1,400 ($14.6/cell) | Internal 200 mA passive balancing |
| Linear Technology/DC2100B [44] | Redistributive balancing<br>Cell monitoring | 12 cells<br>(8 for 96 cells) | 475 × 8 = $3,800 ($39.6/cell) | Bidirectional fly-back<br>converter on each cell |

It can be seen from the Table 2.4 that the commercially available BMSs mostly support only passive/dissipative balancing instead of the redistributive balancing. Even though DC2100B is capable of redistributive balancing, the cost is roughly three times more than Orion/BMS2. So

transitioning from dissipative balancing to redistributive one for small OEMs is debatable from the cost prospective. Even for the high-end OEMs, such as GM and Tesla, the feasibility without over budget is also unpromising according to the road map of the EV targets in Table 2.3.

### 2.3.4 Integrating battery balancing into APM

Given the challenges and regulations of the BMS, it is extremely difficult to implement reliable and fast redistributive balancing solely on BMS hardware without sacrificing performance or cost. The extra cost originates from the added components needed for turning a dissipative balancing to a distributive one, considering using one of the reviewed topological options from Section 2.1. The relatively cost-friendly distributive solution is inductor/capacitor-based balancing circuit while it suffers from slow equilibrium and costly magnetic materials. The converter-based modular design has significantly better performance and various of the balancing modes. Nevertheless, the active switches increase the cost by a considerably large amount.

Without significantly cheaper components from the manufacturers, it is barely possible to achieve low cost but fast and intelligent redistributive balancing. Clearly, the one of the benefits of applying the redistributive balancing is improving pack usable capacity for the aged or second-life battery packs. If the functions of several systems can be integrated into one device without introducing significant cost, the entire cost of the combined systems is then reduced.

As explained in the previous section, the APM is a single HV-to-LV DC/DC converter that provides the LV loads powered by HV pack. If the single converter can be topologically split to several individual converters, similar to the converter-based battery balancing structure with parallel modular design, the functions of APM and BMS can be combined to reduce the cost. This concept is named as battery-balancing auxiliary power module (BB-APM). In addition, if the proposed BB-APM circuitry can relatively be cost-competitive compared with the combined system, then the redistributive balancing is achieved with no or little extra charge. The proposed BB-APM system is illustrated in Fig. 2.11.

Many power DC-DC converters can be applied in this APM balancing circuit, as long as

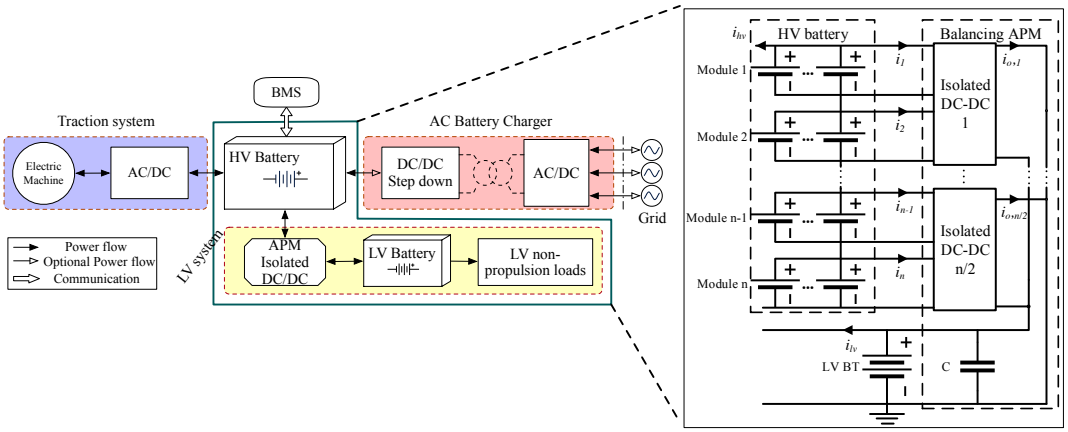



Figure 2.11: Simplified EV system architecture with proposed APM

they are bi-directional and isolated. For higher efficiency and smaller size, soft switching, high-frequency operation and less power switches are normally preferred. The concept has been investigated by a dual active bridge (DAB) technique as the power electronics medium from HV to LV [17]. The design fulfilled the purpose of balancing and voltage level conversion, but it is hard to be convinced as a compact or cost-friendly design due to a large number of power switches used (8 switches for balancing one battery cell) in DAB. So this study focuses on the evolution on the hardware design, aiming to reduce the cost of the BB-APM concept and bring new functions without extra cost.

## 2.4 Functionalities of BB-APM and translated circuit parameters

According to the mechanism of redistributive battery balancing, to actively compensate the imbalance among the battery cells requires that

1. the output power of the entire system is guaranteed with little compromise
2. the load on each cell is dynamically adjusted based on the state of the cell
3. the cell status is properly monitored

The requirements above can be translates to the following circuit-related parameters for $x$th isolated converter link

1. regulating the output current — $i_{o,x}$

2. adjusting the cells currents — $i_x$ and $i_{x+1}$

3. measuring the cell currents and voltages — $i_x$, $i_{x+1}$, $v_x$, and $v_{x+1}$

The aforementioned functionalities should be satisfied for the BB-APM.

## 2.5 Conclusion

The battery balancing is necessary to prolong the driving range and protect the battery pack. Dissipative and redistributive balancing strategies are two options for battery balancing, where the former one is commonly used due to its simplicity and low-cost. However, the benefits of implementing the redistributive balancing cannot be neglected. The publicly available aging data and self-collected testing data show that the cell capacities significantly diverge, up to 36% cycle difference when the weakest and average cells reach 80% of their original capacities. The dissipative balancing strategy, however, cannot utilize that part of capacity, leading to a up to 36% shorter lifetime compared with redistributive balancing. The technical road map for the components inside the EVs and the cost breakdown for Chevy Bolt are summarized, showing a rough cost of $400 of the BMS and APM. In order to achieve such target with redistributive balancing, the concept BB-APM is proposed, whose functionalities are also defined.

# Chapter 3: Half-Full Bridge Converter for BB-APM

Allowing the industry to adopt the redistributive balancing without extra effort, reducing the cost of the redistributive balancing is the priority of this thesis in terms of power electronics design and balancing function development. The topological requirements of the BB-APM are galvanic isolation and bidirectional power flow. The design starts from a review of the state-of-art isolated bidirectional DC/DC converters.

## 3.1 State-of-art isolated bidirectional DC/DC converters

The DC/DC converters are categorized into current-fed, voltage-fed converters and the combination of those [45]. The voltage-fed converters connect power stage directly to the voltage source, whereas the current-fed one connects an inductor before the voltage source. The current-fed converters will not cause catastrophic failure when half-bridge is shot through because the circuit is inductive. However, the current-fed converters are less commonly used as additional power stage is required, leading to higher cost and complexity.

The commonly adopted primary topologies for high-frequency isolated converters are shown in Fig. 3.1. The full bridge (FB) topology is normally preferred over the half bridge (HB) because of its lower MOSFET's voltage stress for high-voltage applications [46]. The HB switches should be voltage rated at least doubled compared to FB counterpart. However, in BB-APM application, the input voltage is a single cell voltage that is usually below 5 V and thus, HB becomes appealing. Not only is high voltage rating needed for L-type HB, but also the extra high-current inductors are required. Therefore, from the cost prospective, the L-type HB is not preferred in this thesis. Even though the discrete inductors in the push-pull converter can be integrated into the center-tapped transformer, designing the center-tapped transformer with high utilization factor remains

challenging [47].

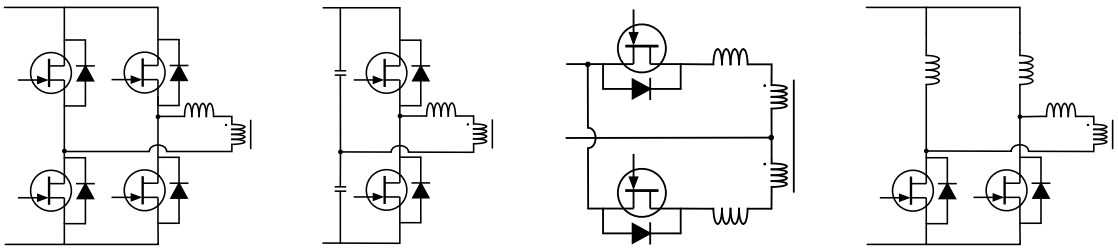



Figure 3.1: Major primary topologies for high-frequency converters: (a) full bridge, (b) half bridge, (c) push-pull, and (d) L-type half bridge

The biggest advantage of the HB topology is that two stabilization capacitors can be substituted by two battery cells without affecting the circuit operation. As a result, with a proper controller that will be explained later, the HB configuration can manage two cells, which realizes the lowest MOSFET-per-cell ratio of 1 MOSFET/cell on the primary side. The FB has a MOSFET-per-cell ratio of 4 MOSFETs/cell while L-type HB and push-pull converters achieve 2 MOSFETs/cell. Then the HB on primary side is the best candidate in terms of the circuit cost and complexity.

The secondary side can be either FB or HB. The HB has the potential to stress the devices unevenly due to the uneven voltage sharing on the output capacitors. Some care has to be taken of to balance the capacitor voltage. Therefore, in this chapter, the HB + FB configuration, named as HFB in this thesis, is firstly discussed. The HB + HB configuration will be presented in next chapter with more aggressive circuit simplification to further lower the cost.

## 3.2 HFB topology and steady-state operation

The proposed isolated HV-LV converter consists of a half bridge on the primary side and a full bridge on the secondary side. The systematic layout is shown in Fig. 2.11 and proposed isolated DC-DC converter topology is shown in Fig. 3.2. The half bridge allows two cells or parallel-connected cells (modules) balanced by one converter, instead of one cell/module per converter for conventional converter topologies, such as DAB [17], [48], [49] and flyback converter [50]–[54].

This topology then inherently reduces the number of the individual converters needed. The term cell will be used to represent cell or parallel-connected cells in the rest of paper without losing the generality. On the other hand, the full bridge offers stabler voltage and less filtering capacitance needed on the secondary side. The high frequency transformer in between is responsible for energy transfer and galvanic isolation. Normally, an external inductor in the topology is required for the circuit operation. However, if the switching frequency is high enough and the transformer is customized for the operation, the inductor can be integrated as the leakage inductor in the transformer to achieve more compact design.

To simplify the analysis in this thesis, LV battery and loads are represented by a controlled current source depending on the load condition. HV loads are neglected without affecting the analysis because all the cells share the same current. The operation of the APM and battery balancing has little impact on the HV loading. However, it is straightforward to reconsider those omitted components due to the simplification given a simple current divider rule.

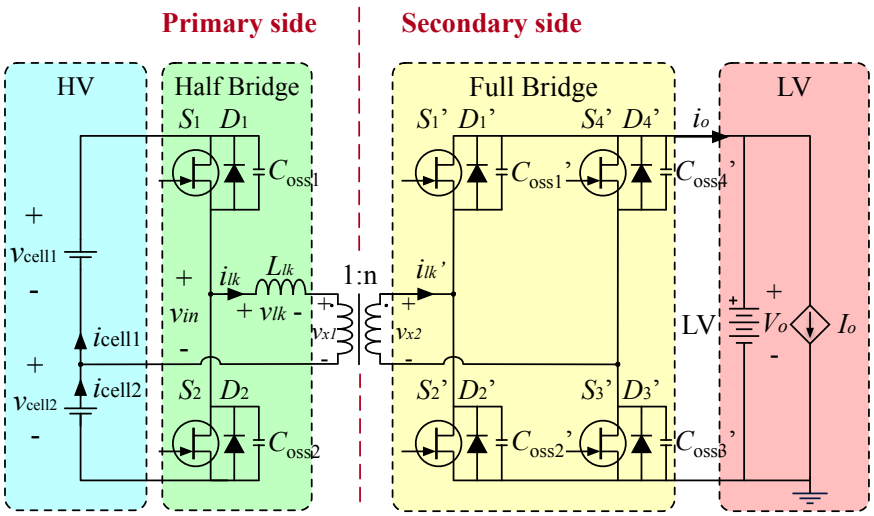



Figure 3.2: The HFB topology applied in APM

Achieving the BB-APM requirements specified in section 2.4 necessitates a means to independently control the cell currents, $i_{\text{cell1}}$ and $i_{\text{cell2}}$ in Fig. 3.2, as well as the LV loads, i.e. $i_{\text{o}}$. Asymmetric duty cycle enables arbitrary cell currents, otherwise the cells share the same current within one HFB, leading to impossibility of balancing the cells in the same converter. On the

other hand, output current control is realized by phase shift control. Both aforementioned control strategies are based on pulse-width modulation (PWM). However, before elaborating the control techniques, the basic circuit operations should be explained. In Fig. 3.2, with the alternatively switched MOSFET on the primary, the cell 1 and cell 2 also alternatively conduct. During the conduction period of the cells, the average current of that period is then the effective current for charging or discharging the corresponding cell. On the other hand, the secondary switches are utilized in the similar means of active rectification with a small difference on the phase shift. The phase shift control will be explained in the later sections.

The currents on primary and secondary sides are governed by the equivalent leakage inductor $L_{\mathrm{lk}}$ which is the sum of primary leakage inductance $L_{\mathrm{lk1}}$ and primary referred secondary leakage inductance $L'_{lk2}$, i.e.

$$L_{\mathrm{lk}} = L_{\mathrm{lk1}} + \frac{L_{lk2}}{n^2} \tag{3.1}$$

where $n$ is the ratio of the number of the primary and secondary turns $N_{\mathrm{p}}/N_{\mathrm{s}}$. From the property of the inductor, the transformer current is governed by the following equation:

$$v_{\mathrm{lk}}(t) = L\frac{di_{\mathrm{lk}}(t)}{dt}. \tag{3.2}$$

Since the voltage across the inductor is depending on the voltage applied to the two terminals, the current can be regulated by adjusting the duration and polarity of the applied voltage.

The proposed circuit is operating with 6 noticeable states with different combinations of switches being turned on/off. The equivalent circuit models (ECMs) at each state are shown in Figs. 3.3(a) - 3.3(f). The Figs. 3.3(a), 3.3(b), 3.3(d) and 3.3(e) illustrate the phase-shifted operations, which are the sources of the power transfer between primary and secondary sides in both directions [48], [49], [55]. Besides the phase shift interval (denoted as $d$ in Fig. 3.3(g)), the duty cycle adjustment $\theta$ is introduced to achieve different balancing modes. Steering the current difference between two cells in one link, the duty cycle adjustment $\theta$ is introduced to the 50-50% duty cycle. Both phase shift control and duty cycle adjustment will be explained in Section 3.4.

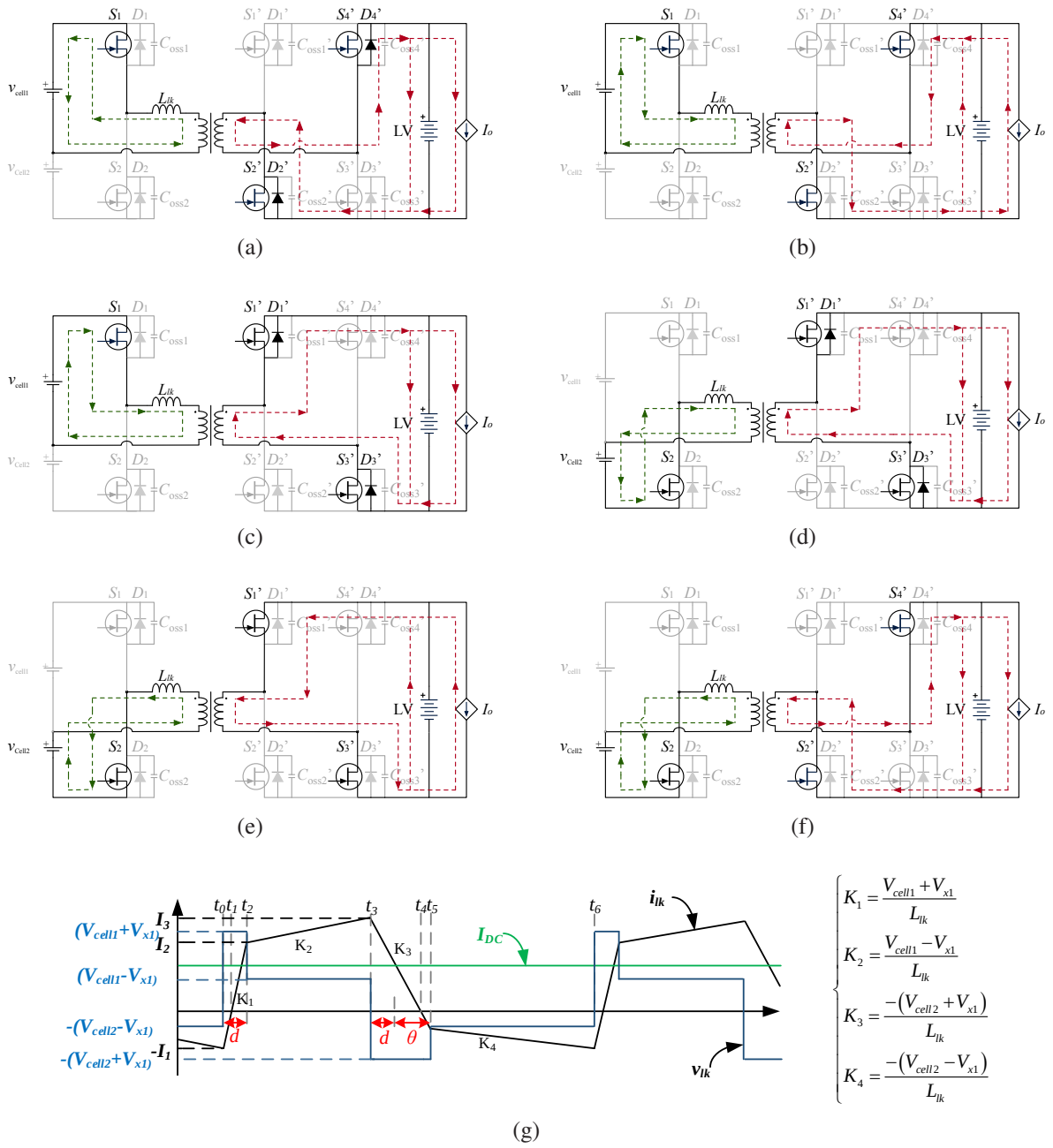



Figure 3.3: Operating states of the HFB, (a) ECM between $t_0$ and $t_1$, (b) ECM between $t_1$ and $t_2$, (c) ECM between $t_2$ and $t_3$, (d) ECM between $t_3$ and $t_4$, 4 (e) ECM between $t_4$ and $t_5$, (f) ECM between $t_5$ and $t_6$, (g) the leakage inductor current waveform with time stamps

**Duration segment 1 in Fig. 3.3 (a)** $(t_0 - t_1)$

The switches $S_1$, $S_2'$, and $S_4'$ are turned on during this period. Due to the existing current direction, the current on the primary side flows into the battery cell 1, i.e. charging the cell. On the

secondary side, the current flows into the LV side powering the loads.

How the leakage inductor current changes during this period is then based on the voltage applied on it. The gradient of the current $i_{\mathrm{lk}}$ can be expressed as follows

$$K_1 = \frac{di_{\mathrm{lk}}}{dt} = \frac{v_{\mathrm{lk}}}{L_{\mathrm{lk}}} = \frac{V_{\mathrm{cell1}} + V_{\mathrm{LV}}/n}{L_{\mathrm{lk}}} \tag{3.3}$$

where, $V_{\mathrm{cell1}}$ and $V_{\mathrm{LV}}$ are the average value of the instantaneous values over the duration. This is due to a reasonable assumption that the battery voltages are constant during the switching period. The higher switching frequency is, the more stable the voltages are. The filtering capacitors are also added for stabilizing the voltages.

**Duration segment 2 in Fig. 3.3 (b) ($t_1 - t_2$)**

During the interval between $t_1$ and $t_2$, the conducting switches remain the same as the previous state. However, the direction of the current flow is reversed as the current increases. The current in this state keeps rising at the rate of $K_1$ until switches on the secondary side commutate at time instance $t_3$.

**Duration segment 3 in Fig. 3.3 (c) ($t_2 - t_3$)**

At time instance $t_3$, the MOSEFTs $S_1'$ and $S_4'$ are switched on while $S_2'$ and $S_3'$ are shut off. By modulating the conducting MOSFETs on the secondary side, the applied voltage on the leakage inductor is correspondingly changed. Instead, the slope of the leakage inductor current now is

$$K_2 = \frac{di_{\mathrm{lk}}}{dt} = \frac{V_{\mathrm{cell1}} - V_{\mathrm{LV}}/n}{L_{\mathrm{lk}}}. \tag{3.4}$$

Compared with the slope $K_1$ during $t_0 - t_2$, $K_2$ is smaller than $K_1$ under the assumption that the turns ratio is properly designed such that the numerator of $K_2$ is positive. Therefore, the rate of current change slows down, as can be observed from Fig. 3.3(g).

**Duration segment 4 in Fig. 3.3 (d) ($t_3 - t_4$)**

During this period, the secondary switches continue to operate as segment 3 does but with primary $S_2$ switched on. The leakage current starts to decrease at a rate of

$$K_3 = \frac{di_{\mathrm{lk}}}{dt} = \frac{-V_{\mathrm{cell2}} - V_{\mathrm{LV}}/n}{L_{\mathrm{lk}}}. \tag{3.5}$$

Turning on $S_2$, the cell 2 is connected to the power stage to exchange energy.

**Duration segment 5 in Fig. 3.3 (e) ($t_4 - t_5$)**

Remaining all the operation as of in duration segment 4, the current whose direction is reversed at $t_4$ keeps decreasing at the rate of $K_3$ until the time instance $t_5$. It leads to the interchange of the switches conducting on the secondary side.

**Duration segment 6 in Fig. 3.3 (f) ($t_5 - t_6$)**

As the last state during one period of the operation, $S_1'$ and $S_3'$ are turned off, on the other hand, $S_2'$ and $S_4'$ are switched on. As a result, the rate of the current change reduces shown in Eq. (3.6), caused by the smaller voltage across the leakage inductor.

$$K_4 = \frac{di_{\mathrm{lk}}}{dt} = \frac{-V_{\mathrm{cell2}} + V_{\mathrm{LV}}/n}{L_{\mathrm{lk}}} \tag{3.6}$$

Note that all the derivation and explanation aforementioned are based on the assumption that primary-referred LV voltage is smaller than the cell voltage, i.e. $V_{\mathrm{cell}x} > V_{\mathrm{LV}}/n, x \in \{1,2\}$. However, the analysis procedure remains the same, but the waveform slightly changes accordingly.

The piece-wise expressions of the leakage inductor current $i_{\mathrm{lk}}$ can then be obtained based on

the previous derivations of the slopes during each segment.

$$i_{\text{lk}}(t) = \begin{cases} i_{\text{lk}}(t_0) + K_1 t, & t_0 < t \leq t_2 \\ i_{\text{lk}}(t_2) + K_2(t - t_2), & t_2 < t \leq t_3 \\ i_{\text{lk}}(t_3) + K_3(t - t_3), & t_3 < t \leq t_5 \\ i_{\text{lk}}(t_5) + K_4(t - t_5), & t_5 < t \leq t_6 \end{cases} \tag{3.7}$$

where the only unknown is the initial condition $i_{\text{lk}}(0)$. In steady state, the leakage inductor current, at the end of each period, converges to where it begins, i.e.

$$i_{\text{lk}}(t_0) = i_{\text{lk}}(t_0 + T) = i_{\text{lk}}(t_6) \tag{3.8}$$

where the switching period is denoted as $T$. Therefore, in steady state, the initial condition can be solved as the half of peak-to-peak (P2P) ripple current $i_{\text{lk,pp}}$ subtracted by the DC offset

$$\begin{aligned} i_{\text{lk}}(t_0) &= \frac{i_{\text{lk,pp}}}{2} - I_{\text{DC}} \\ &= \frac{K_1 d + K_2(\frac{T}{2} - \theta - d)}{2} - I_{\text{DC}}. \end{aligned} \tag{3.9}$$

This will help formulate the output power as well as mathematical modeling of the circuit.

### 3.3 Leakage inductor current

As explained previously, the leakage inductor dominates the circuit operation. Therefore, improperly regulating the leakage inductor current not only fails to deliver the designed power, but potentially will permanently damage the circuit due to an effect called volt-amp (VA) imbalance that is more severe in battery balancing application.

### 3.3.1 Unbalanced drift effect

The high-side switch $S_1$ and low-side switch $S_2$ on primary side (PS) are alternatively turned on for 50% of a switching period in traditional phase shift control, also known as symmetric control. Less than 50% symmetrical duty cycle can be used in phase shift control as well, but 50% duty cycle allows the largest range of output power range since longer phase shift can be applied. The relation is justified by the fact that the phase shift is proportional to output power, which will be explained in Section 3.4. However, the symmetric control cannot be directly applied to the proposed topology since the two cells on the primary side are normally unbalanced in terms of voltage for the lack of balancing circuits and variations of the cells [29], [34], [36]. Kirchhoff's voltage laws define the voltage across $L_{\mathrm{lk}}$ on the primary side during all operation modes in Fig. 3.3:

$$v_{\mathrm{lk}} = v_{\mathrm{cell}n} - v_{x1} \tag{3.10}$$

where the subscript $n \in \{1,2\}$ in $v_{\mathrm{cell}n}$ indicates the index of the battery cell that is currently conducting. The battery cell can be modeled as a constant voltage source with voltage $V_{\mathrm{cell}n}$ during a extremely short switching period. $v_{x1}$ is the output voltage referred to primary side, which can also be assumed constant $V_{x1}$, within the switching period.

The leakage inductance current changes at a rate of $v_{\mathrm{lk}}/L_{\mathrm{lk}}$ as explained in the previous section, which differs when the two cells have different voltage levels, i.e. unbalanced. Considering a simplest example, the circuit operates with 50% duty cycle and no phase shift control. The trends of the leakage inductor current when cell voltages are under balanced and unbalanced conditions are shown in Fig. 3.4. It can be observed that the current increases gradually cycle by cycle and ideally rises to infinite when $V_{\mathrm{cell1}} > V_{\mathrm{cell2}}$. This can be explained by the fact that the absorbed and released energy in the transformer is out of balance and the net effect is absorbing. On the other hand, in the case that $V_{\mathrm{cell1}} = V_{\mathrm{cell2}}$, the absorbed and released energy are compensated, leading to zero net change during one period. For the condition where $V_{\mathrm{cell1}} < V_{\mathrm{cell2}}$, the current will reversely increase to negative infinity.

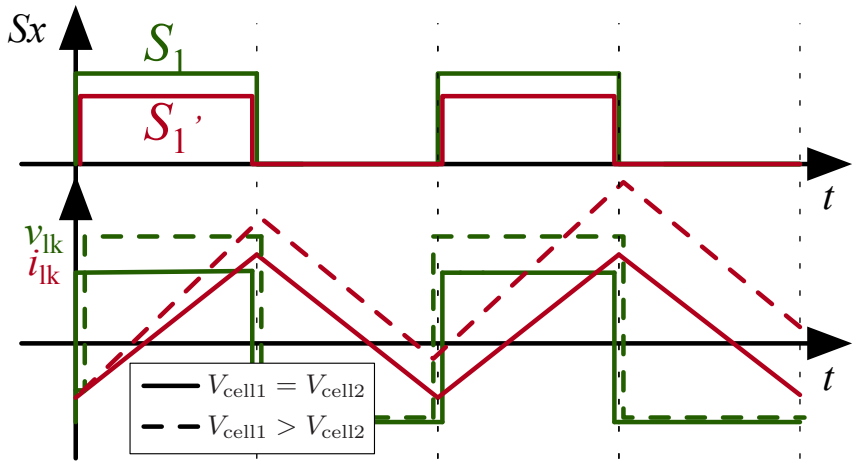



Figure 3.4: The diverged leakage inductor current compared with stable one when cells are unbalanced

As discussed above, the imbalance of cell voltages causes the net current change on the leakage inductance non-zero within one period if symmetric control is applied, i.e. VA imbalance of leakage inductance. Consequently, the leakage inductor current diverges, as shown by red dotted line in Fig. 3.5 (c). The uncontrolled leakage inductor current causes many consequences, such as flux saturation, overheating and circuit damage. It can be seen from Fig. 3.2 that the leakage inductor current $i_{lk1}$ is determined by the cells currents $i_{cell1}$ and $i_{cell2}$ by Kirchhoff's circuit laws:

$$i_{lk1} = i_{cell1} - i_{cell2}. \tag{3.11}$$

Conveniently, the partial requirement defined in the section 2.4 item 2 can be achieved if the leakage inductor current can be controlled. Furthermore, as the circuit is linear, the equation (3.11) will be still valid if it is integrated over a same period of time. As a result, Kirchhoff's current laws still apply to the average values, i.e. $I_{lk1} = I_{cell1} - I_{cell2}$. The average values are more of interest in this thesis since the cell currents can be approximated as constant after proper LC filter.

This also coincides with an approach called large-signal average modeling that is adopted to simplify the modeling process of highly dynamic current response [56], [57] by filtering out high-frequency switching behavior and remaining the low-frequency or DC response.

### 3.3.2 Introduced phase shift $d$ and duty cycle adjustment $\theta$

The phase shift is introduced between $t_0$ and $t_2$ to enable power transfer from HV side to LV side, leading to discharging or charging the cells in the link. In addition to phase shift $d$, between $t_3$ and $t_5$, a small portion of time $\theta$ that is originally part of cell 1's conduction time is partitioned to cell 2's. In other words, cell 1 is conducting for a period of $\frac{T}{2} - \theta$ and cell 2 is on for the rest of the period, i.e. $\frac{T}{2} + \theta$. When the cells are out of balance, the VA is not balanced and thus, the leakage current diverges. This asymmetrical duty cycle compensates the VA imbalance and stabilizes the leakage current. In addition, the leakage current can be controlled by $\theta$ to achieve C2C balancing, which will be explained in Section 3.4.

In order to highlight the purpose of applying both control algorithms before elaborating the theory, a figure that compares the circuit behavior with and without phase shift and asymmetric control is illustrated in Fig. 3.5. No average output current can be observed if phase shift is not introduced as shown in Fig. 3.5 (e), compared with Fig. 3.5 (d). On the other hand, the leakage current will diverge until infinite if the imbalance of the cell voltages presents and no adjustment is made on the PWM signals, as explained in Section 3.3.1. Introducing the duty cycle adjustment eliminates the non-zero net change and thus, the leakage inductor current stays stable, as shown in Fig. 3.5 (c).

### 3.3.3 Average modeling

In order to establish the system model to employ control algorithms, average modeling technique is utilized to derive the low-frequency or DC behavior. The averaged dynamic behavior can be mathematically modeled and the averaged variables are also desired, such as the averaged output current and DC offset current for the leakage inductor. The average modeling utilizes the concept that the averaged cause will lead to the same averaged response regardless of the high-frequency responses.

By assuming the voltages of the cell and transformer are constant over the short switching period, the instantaneous values are replaced by their low-frequency or averaged values denoted

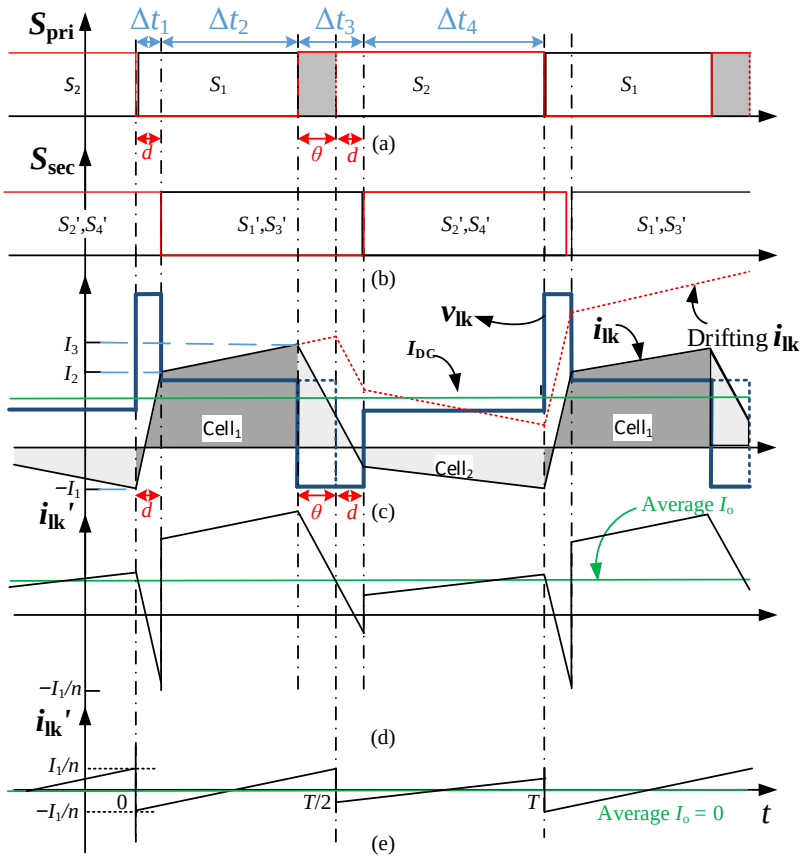



Figure 3.5: Switching PWM signals: (a) primary switches, (b) secondary switches; (c) primary referred leakage inductor voltage and current: red dot - symmetric control, black line - asymmetric control; secondary-referred leakage inductor current (d) with phase shift and (e) without phase shift

as a "bar" over the corresponding instantaneous values, e.g. $\bar{i}_{lk}(t)$. The leakage inductor voltage can be piece-wisely analyzed and divided to four sub-intervals within one period according to the ECMs in Fig. 3.3. The simplified ECMs and expressions within each subinterval are given in Fig.

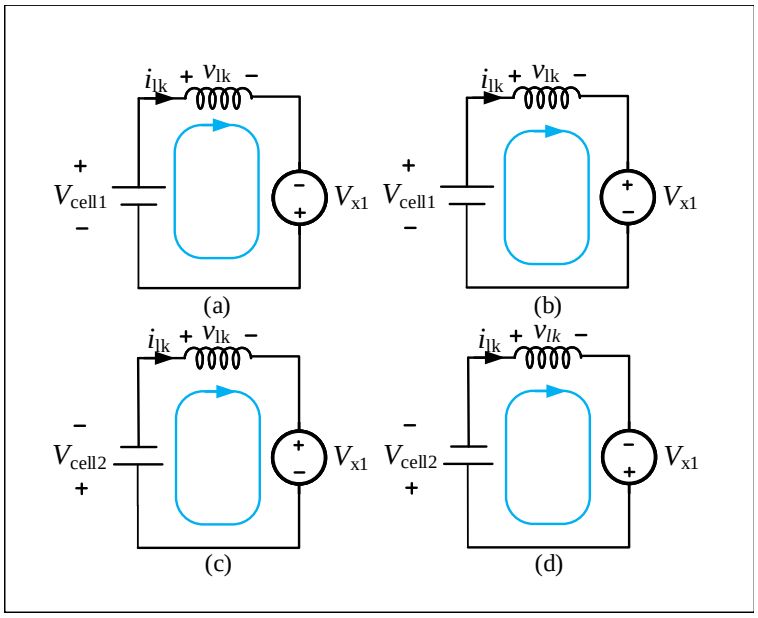



Figure 3.6: Equivalent circuit models referred to primary side during: (a) $0 \leq t < d$, (b)$d \leq t < \frac{T}{2}$, (c) $\frac{T}{2} - \theta \leq t < \frac{T}{2} + d$, and (d)$\frac{T}{2} + d \leq t < T$

3.6 and Eq. (3.12), respectively.

$$\overline{v}_{\mathrm{lk}}(t) = \begin{cases} V_{\mathrm{cell1}} + V_{x1}, & t \in [0, d] \\ V_{\mathrm{cell1}} - V_{x1}, & t \in (d, \frac{T}{2} - \theta] \\ V_{\mathrm{cell2}} + V_{x1}, & t \in (\frac{T}{2} - \theta, \frac{T}{2} + d] \\ V_{\mathrm{cell2}} - V_{x1}, & t \in (\frac{T}{2} + d, T] \end{cases} \tag{3.12}$$

where $V_{x1}$ is output voltage referred to primary side through the transformer, which is considered as constant voltage source with the voltage value of $V_{\mathrm{LV}}/n$. Therefore, the average voltage during

the entire period can be obtained by

$$\begin{aligned}\overline{v}_{\mathrm{lk}}(t) &= \frac{1}{T}\int_{t}^{t+T} v_{\mathrm{lk}}(t)dt \\ &= \frac{1}{T}[d(V_{\mathrm{cell1}}+V_{x1}) + (\frac{T}{2}-\theta-d)(V_{\mathrm{cell1}}-V_{x1}) \\ &\quad -(d+\theta)(V_{\mathrm{cell2}}+V_{x1}) - (\frac{T}{2}-d)(V_{\mathrm{cell2}}-V_{x1})] \\ &= \frac{T}{2}(V_1-V_2) - \theta(t)(V_1+V_2).\end{aligned} \tag{3.13}$$

The averaged effect of the leakage inductor's dynamics can be then calculated by substituting Eq. (3.13) into Eq. (3.13)

$$\frac{d\bar{i}_{\mathrm{lk}}(t)}{dt} = \frac{dI_{\mathrm{DC}}}{dt} = \bar{v}_{\mathrm{lk}}(t) = \frac{T}{2L_{\mathrm{lk}}}\underbrace{(V_1-V_2)}_{V_\Delta} - \theta(t)\underbrace{(V_1+V_2)}_{V_\Sigma}. \tag{3.14}$$

This equation describes how the DC components of the inductor current vary with time. It shows that the dynamic of the leakage inductor current is purely a function of duty cycle adjustment $\theta$, which implies the average leakage inductor current is controllable by properly varying $\theta$. Eq. (3.14) also mathematically explains the reason why the current tends to increase due to the voltage difference if symmetrical duty cycle is applied.

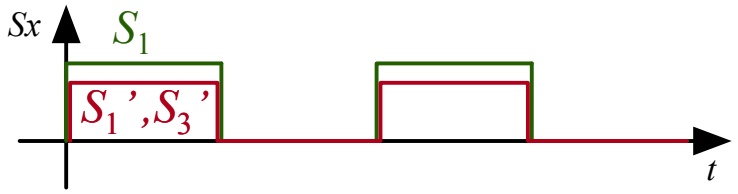
As explained before, the average leakage inductor current $\bar{i}_{\mathrm{lk}}(t)$, denoted as $I_{\mathrm{DC}}$ for a clearer representation, is the average value of difference between two cells' currents, i.e. $I_{\mathrm{DC}} = I_{\mathrm{cell1}} - I_{\mathrm{cell2}}$. It is also because the high frequency current component is transferred through the transformer to the secondary side (SS) and DC offset remains on the PS due to the property of a transformer. Therefore, controlling the DC offset current $I_{\mathrm{DC}}$ regulates the current difference between cells. Note that this matches the concept of battery balancing, which distributes the individual current demand on each cell according to corresponding SOCs/voltages. This property provides the feasibility of regulating each cell's current in one link by introducing the duty cycle adjustment $\theta$.

## 3.4 Basic control logic

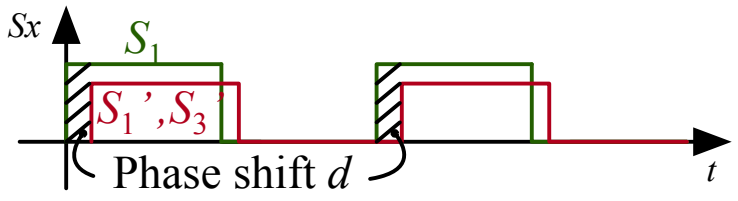
It has been mentioned that the power transfer is realized by the phase shift control; the duty cycle adjustment can regulate the current difference of the adjoining cells. This section elaborates the operations and derives the power equations based on phase shift control as well as the asymmetric duty cycle adjustment.

### 3.4.1 Phase-shifted control

The phase shift control is adopted in this thesis to enable bi-directional power flow [58]–[61]. During the non-phase-shifted operation, the switch sets [$S_1$, $S_1'$, and $S_3'$] or [$S_2$, $S_2'$, and $S_4'$] will be turned on at the same time instance, as shown in Fig. 3.7(a). Introducing a phase delay $d$ (illustrated in Fig. 3.7(b)) between primary side ($S_1$ or $S_2$) and secondary side ([$S_1'$ and $S_3'$], or [$S_2'$ and $S_4'$]) switches leads to positive power flow (HV to LV), and the negative power flow can be realized by a phase lead. Without phase shift, shown in Fig. 3.5 (e), the average current of the secondary referred leakage inductor current is zero and thus, no power is generated. The introduced phase shift acts as a rectifier to regulate the average current, leading to a non-zero output power, as illustrated in Fig. 3.5 (d).




(a)




(b)

Figure 3.7: The PWM signals (a) without phase shift and (b) with phase shift

### 3.4.2 Output power introduced by phase shift

If the two cells in one HFB are balanced in terms of voltage, i.e. $V_{\text{cell1}} = V_{\text{cell2}} = V_{\text{cell}}$, this dual-cell link is not operating under balancing mode. Instead, a pure power-delivering mode is engaged. That is, the link is only a media of transferring energy from two cells to the auxiliary without balancing functionality. In this case, the currents from both cells are at the same amplitude, which means 50% of power comes from each individual cell. The critical current waveforms under balanced condition are given in Fig. 3.8. The output power is, on the other hand, the product of

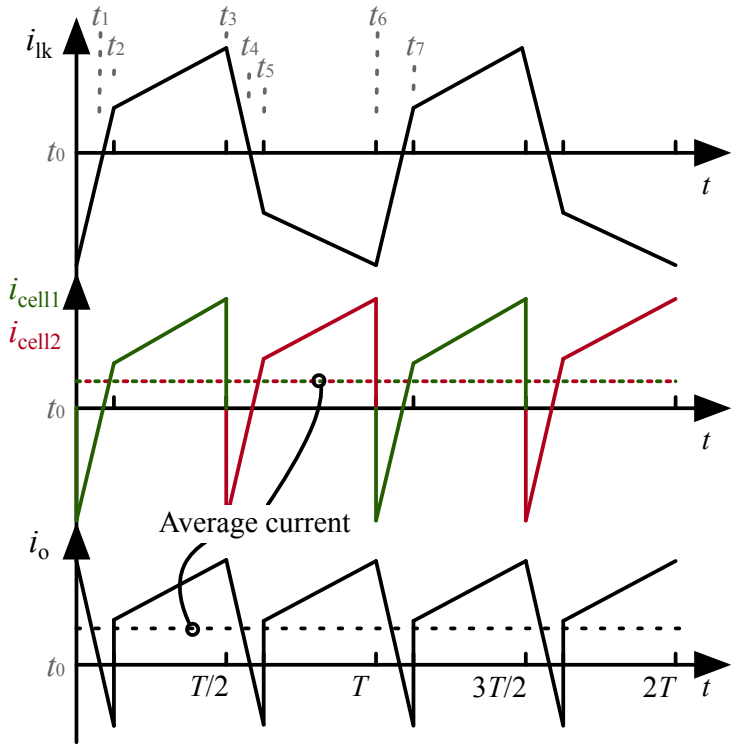



Figure 3.8: The current waveforms when battery are balanced, top: leakage inductor current on primary side; middle: cell currents; bottom: output current on LV side

output current and voltage. The output voltage determined by LV battery varies slowly with the load as the battery charges or discharges but can be assumed to be constant during one switching period. It can be seen from Fig. 3.8 that output current $i_{\text{o}}$ is a periodic signal, and thus, the area under the waveform of $i_{\text{o}}$ over one period $T$ determines the average output current and can be obtained by integrating $i_{\text{o}}(t)$ over the period.

Combining with the slopes, the continuous-time expression of $i_{\mathrm{o}}$ can be obtained piece-wisely to perform the integral. The values at those time instants are linked with leakage inductor current on the primary side. As it is rectified version of the secondary-referred leakage inductor current, the output current $i_{\mathrm{o}}$ is scaled down by the factor of the turns ratio $n$, i.e.

$$i_{\mathrm{o}}(t) = \begin{cases} \dfrac{i_{\mathrm{lk}}(t)}{n}, & t_1 < t \leq t_5 \\ -\dfrac{i_{\mathrm{lk}}(t)}{n}, & t_5 < t \leq t_7. \end{cases} \tag{3.15}$$

Therefore, the expression of the output current $i_{\mathrm{o}}$ can be obtained accordingly. It is given within a half-cycle period $\dfrac{T}{2}$ because the output current is actually periodic with period $\dfrac{T}{2}$.

$$i_{\mathrm{o}}(t) = \begin{cases} \dfrac{i_{\mathrm{lk}}(t_2)}{n}, & t = t_2 \\ i_{\mathrm{o}}(t_2) + \dfrac{K_2}{n}t, & t_2 < t \leq t_3 \\ i_{\mathrm{o}}(t_3) + \dfrac{K_3}{n}(t - t_3), & t_3 < t \leq t_5 \end{cases} \tag{3.16}$$

where $i_{\mathrm{lk}}(t_2)$ can be solved by combining Eq. (3.7) and (3.9) with the assumption that $\theta$ and $I_{\mathrm{DC}}$ are zero. Given the continuous-time expression above, the output power $P_{\mathrm{o}}$ can then be calculated, as similarly derived in DAB application [48], [49]:

$$\begin{aligned} P_{\mathrm{o}} = V_{\mathrm{o}} I_o &= V_{\mathrm{o}} \cdot \frac{1}{T} \int_0^T i_{\mathrm{o}}(t)dt \\ &= V_{\mathrm{o}} \cdot \frac{2}{T} \int_0^{\frac{T}{2}} i_{\mathrm{o}}(t)dt \\ &= V_{\mathrm{o}} \cdot \left[ \int_{t_2}^{t_3} i_{\mathrm{o}}(t)dt + \int_{t_3}^{t_5} i_{\mathrm{o}}(t)dt \right] \\ &= V_{\mathrm{o}} \cdot \underbrace{\frac{TV_{cell}}{2nL_{\mathrm{lk}}}(1 - d')d'}_{I_o} \end{aligned} \tag{3.17}$$

where $d'$ is the normalized phase shift, i.e. $d' = d/\frac{T}{2}$. $P_{\mathrm{o}}$ can be controlled by the phase shift $d'$ based on the Eq. (3.17). It can be also observed that there is no output power when phase shift is

zero, i.e. $d' = 0$, which is constant with the explanation in Fig. 3.5. The derived power expression indicates that the phase shift determines the output power to locate between 0 to $\frac{TV_oV_{cell}}{8nL_{lk}}$ (when $d' = 0.5$), where it is limited and confined by the circuit parameters such as leakage inductance and turns ratio. These electronic factors are mainly determined by the transformer. Therefore, they will be considered and used as the design guidance of the transformer for a given output power requirement.

### 3.4.3 Duty cycle compensation

As explained by the previous section 3.3.1, the unbalanced input voltages lead to divergent current response on the leakage inductor. To compensate the VA imbalance, an asymmetric control is proposed by introducing a duty cycle adjustment $\theta$ on the primary side switches. This adjustment directly fine-tunes the conducting time for each cell based on their voltages. For example, if cell 1 has higher voltage, its duty cycle will be set to $\frac{T}{2} - \theta$ and cell 2 will have the complementary conducting time of $\frac{T}{2} + \theta$ where $\theta$ will be determined based on the cell voltages, as shown in Fig. 3.5. Asymmetric duty cycle guarantees the accumulative effects of two cells on the leakage inductor current change are identical, so that the transformer current will remain stable.

The small duty cycle adjustment $\theta$ can be obtained from two perspectives as the ultimate goal is to maintain current stable without divergence. It can be derived from the fact that the current at the end of each period converges to where it begins at the beginning of cycle, i.e. $i_{lk}(0) = i_{lk}(T)$. Alternatively, $\theta$ can be calculated from Eq. (3.14) by letting the overall net effect to be zero, leading to no increment on current after a complete cycle. Both yield the same result:

$$\theta = \frac{T}{2}\left(\frac{V_{cell1} - V_{cell2}}{V_{cell1} + V_{cell2}}\right) = \frac{T}{2}\frac{V_\Delta}{V_\Sigma}, \tag{3.18}$$

where $V_\Delta$ is the voltage difference between the two cells, $V_\Sigma$ is sum of cell 1 and cell 2 voltages. Note that the phase shift $d$ is set to be the same for both $S_1$ and $S_2$ when deriving the expression.

### 3.4.4 Output power due to phase shift and duty cycle adjustment

The introduced duty cycle adjustment is added during the phase shift stage, which indirectly increases the phase-shift period of one cell. As a result, the generated power not only contains the portion introduced by phase shift $d$, but also includes the fragment produced by the additional interval of duty cycle compensation $\theta$. The expression of output power can be obtained similarly as the one with only phase shift involved. Since the duty cycle adjustment is only injected when cells in one HFB are out of balance, it is assumed that $V_{\text{cell1}} > V_{\text{cell2}}$ for the following derivations. The Fig. 3.9 shows the current responses after introducing the adjustment $\theta$ in stead-state condition. Due to the voltage difference between cells, the waveforms are not strictly symmetric compared with Fig. 3.8. Analogous with the procedure discussed in Section 3.4.2, the current waveform can

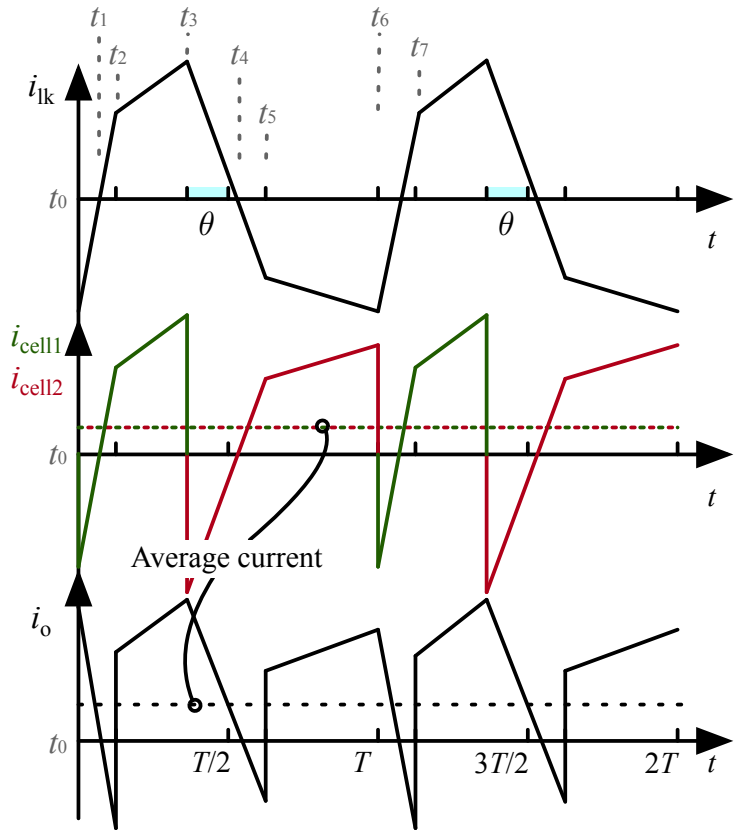



Figure 3.9: The current waveforms when battery are unbalanced, top: leakage inductor current on primary side; middle: cell currents; bottom: output current on LV side

be divided into four piece-wise linear subintervals, i.e. $[t_2, t_3)$, $[t_3, t_5)$, $[t_5, t_6)$, and $[t_6, t_7)$ as shown

in Fig. 3.9. It is noted that the output current $i_o$ is now periodic with a period of $T$ instead of $\frac{T}{2}$ when $\theta$ is not introduced. Therefore, modeling of the output current has to be extended to the full switching period:

$$i_o(t) = \begin{cases} \dfrac{i_{lk}(t_2)}{n}, & t = t_2 \\ i_o(t_2) + \dfrac{K_2}{n}t, & t_2 < t \leq t_3 \\ i_o(t_3) + \dfrac{K_3}{n}(t - t_3), & t_3 < t \leq t_5 \\ i_o(t_5) + \dfrac{K_4}{n}(t - t_5), & t_5 < t \leq t_6 \\ i_o(t_6) + \dfrac{K_1}{n}(t - t_6), & t_6 < t \leq t_7 \end{cases} \tag{3.19}$$

The average output power from HFB can be derived as follows:

$$\begin{aligned} P_o = V_o I_o &= \frac{V_o}{T}\int_{t_0}^{T} i_o(t)dt \\ &= \frac{V_o}{T}\left[\int_{t_2}^{t_3} i_o(t)dt + \int_{t_3}^{t_5} i_o(t)dt + \int_{t_5}^{t_6} i_o(t)dt + \int_{t_6}^{t_7} i_o(t)dt\right] \\ &= \frac{V_o T}{8L_{lk}n}[V_{cell1}\alpha_1 + V_{cell2}\alpha_2] \end{aligned} \tag{3.20}$$

and

$$\begin{aligned} \alpha_1 &= -1 + 4d' + 4\theta' - 2d'^2 - 4\theta'^2 - 8d'\theta' \\ \alpha_2 &= 1 + 4\theta' - 2d'^2 - 4\theta'^2 - 8d'\theta' \end{aligned} \tag{3.21}$$

where normalized duty cycle adjustment $\theta'$ and phase shift $d'$ are calculated by $x' = x/(T/2)$. The equation yields the same results when two cells are balanced by letting $\theta = 0$ in Eq. (3.20). It indicates Eq. (3.20) is a generalized expression, regardless of the conditions of the modulation strategies.

### 3.4.5 Cell-to-Cell current control

As the transformer transmits the electrical energy from primary to secondary side by the principle of electromagnetic induction, only alternating current can create a changing magnetic field. As a result, DC component will not produce the magnetic field change, therefore it will be blocked

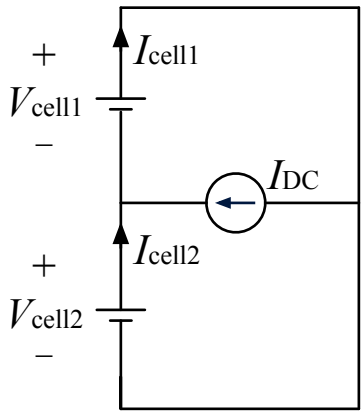



Figure 3.10: The average equivalent circuit model of the primary side

from primary to secondary as well as from secondary to primary. So the average/DC signals of the primary-side can be isolated from the secondary side. The Fig. 3.10 shows the DC equivalent circuit on primary side. Neglecting high-frequency switching, the switches $S_1$ and $S_2$ can be modeled as short circuit and the cells provide only DC currents. The average leakage inductor current is replaced by a constant current source to simplify the circuit analysis. The average current $I_{DC}$ , which is called DC offset current in this paper, is the sum of $I_{cell1}$ and $-I_{cell2}$ by Kirchhoff Current Law. The current difference $(I_{cell1} - I_{cell2})$ then can be controlled by the amplitude and polarity of $I_{DC}$.

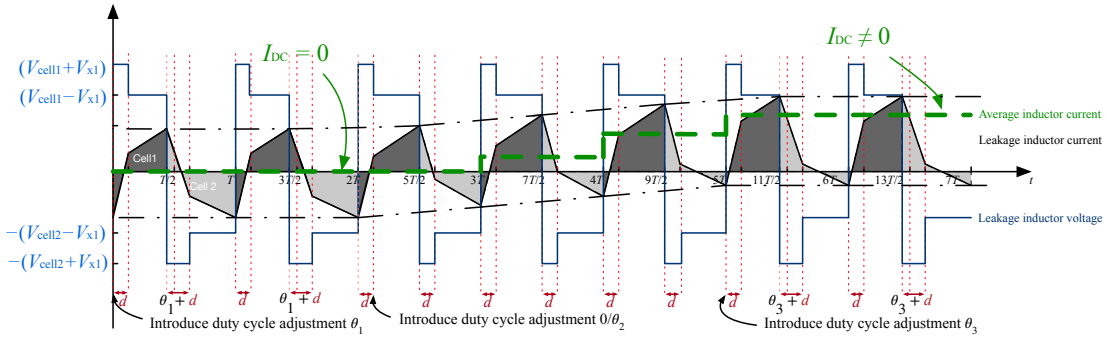



Figure 3.11: The process of regulating $I_{DC}$ to introduce a non-zero $I_{DC}$

In practice, the manually triggered VA imbalance can guide $I_{DC}$ to any arbitrary reference by properly introducing the duty cycle compensation at precisely controlled timings. The current difference makes the cells drain at a different rates, so that the SOC differences can be eliminated eventually, if there is any. A control example is given in Fig. 3.11 with assumption that

$V_{\text{cell1}} > V_{\text{cell2}}$. Initially, the leakage inductor current is operating at steady state with introduced duty cycle compensation based on the cells' voltages. And the C2C current is 0. If a positive $I_{\text{DC}}$ is desired ($I_{\text{cell1}} > I_{\text{cell2}}$), a smaller compensation $\theta_2$ is applied at $2T$, resulting in a positive net inductor current change within one period. The current will start to drift up and can be stabilized to current value by applying another duty cycle compensation $\theta_3$ that makes the net change zero. The described process can be implemented in the microcontroller after deriving the dynamic equations of the system [27]. The higher DC offset current is, the faster the cell 1 is discharged. At the point where $I_{\text{cell1}} > I_{\text{DC}}$, the current flowing out of the cell 2 will start to reverse, i.e. charging cell 2 using cell 1, which is C2C balancing. Flexibly utilizing this phenomenon in a controlled manner, the different balancing modes can be achieved. The detailed balancing modes will be explained in Section 3.5.

### 3.4.6 RMS currents of the transformer on primary and secondary sides

As part of circuit modeling, root mean squired (RMS) currents are important to analyze the system conduction losses. Therefore, this section derives the RMS currents on primary and secondary sides of the transformer. The primary RMS current on the leakage inductor can be calculated by

$$I_{\text{lk,rms}} = \sqrt{\frac{1}{T}\int_{t_0}^{t_6} i_{\text{lk}}(t)^2 dt}. \tag{3.22}$$

Applying the piece-wise current expression in Eq. (3.7) and steady-state duty cycle adjustment in Eq. (3.18) into the equation above yields the primary-side transformer RMS current:

$$\begin{gathered} I_{\text{lk,rms}} = \frac{T}{4\sqrt{3}L_{\text{lk}}(V_1+V_2)}\sqrt{V_{LV}'^2(V_1+V_2)^2 + 4n^2V_1^2V_2^2 - 4nV_{LV}'\Gamma} \\ \text{and} \\ \Gamma = V_1^3d^3 + 3V_1^2V_2d^3 - 3V_1^2V_2d^2 - 3V_1^2V_2d + 3V_1V_2^2d^3 - 6V_1V_2^2d^2 + \\ 3V_1V_2^3 + V_2^3d^3 - 3V_2^3d^2 + 3V_2^3d - V_2^3 \end{gathered} \tag{3.23}$$

where $V_1 = V_{\text{cell1}}, V_2 = V_{\text{cell2}}$ for cleaner presentation. The primary-referred secondary RMS current can be obtained by dividing the turns ratio $n$ as the current flowing through the magnetizing inductor is insignificant. However, the assumption will not be valid for coreless transformers, which will be elaborated in Chapter 4.

$$I'_{\text{lk,rms}} = \frac{I_{\text{lk,rms}}}{n} \tag{3.24}$$

The RMS current equations show the dependencies on the transformer parameters and circuit operating conditions. Therefore, for a given transformer and known operating condition, the RMS currents can be calculated and used for conduction loss estimation. The worst case scenario (maximum RMS currents) can be found using optimization tool subject to the operating boundaries shown below:

$$\min -I_{\text{lk,rms}} \text{ such that } \begin{cases} V_{\text{cell, min}} \leq V_{\text{cell1}} \leq V_{\text{cell, max}}, \\ V_{\text{cell, min}} \leq V_{\text{cell2}} \leq V_{\text{cell, max}}, \\ V_{\text{LV, min}} \leq V_{LV} \leq V_{\text{LV, max}}, \\ P_{\text{o, min}} \leq P_{\text{o}}(d) \leq P_{\text{o, max}} \end{cases} \tag{3.25}$$

where $P_{\text{o}}(d)$ is the output power which is found later that it is determined by the phase shift $d$ at a fixed operating frequency.

## 3.5 Feasible balancing modes

As discussed previously, the power can be transferred between cells and/or LV system. The different combinations of power flow directions create four typical balancing modes with proper DC offset current and phase shift control: a) C2C and cell-to-LV (C2LV), b) C2C and LV-to-cell (LV2C), c) C2LV only, and d) C2C only, as shown in Fig. 3.12.

### 3.5.1 C2C and C2LV

In this mode, the high-SOC cell is demanded to charge the low-SOC cell and power auxiliary loads. It is advisable to adopt this mode when the LV battery is charging or LV loads are online and

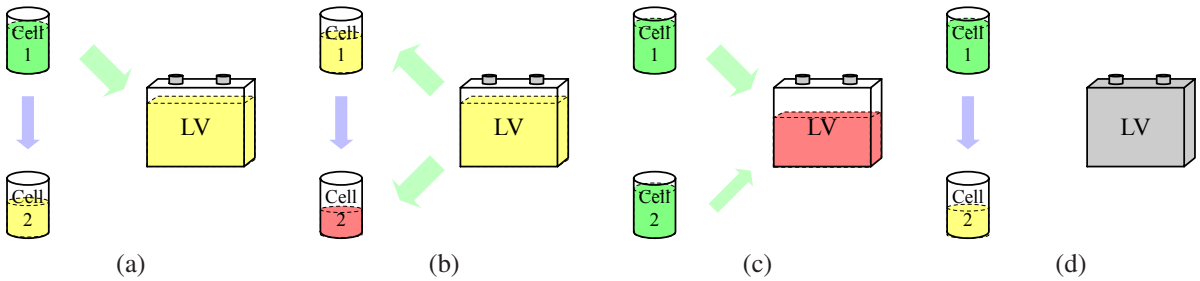



Figure 3.12: The feasible balancing modes: (a) C2C and C2LV, (b) C2C and LV2C, (c) C2LV only, and (d) C2C only

initial SOC bias is significant. The excessive energy from high-SOC cell charges low-SOC cell to converge all cells SOCs to the same level. Meanwhile, the LV battery/loads are being powered by the rest of energy from high-SOC cell. It is extremely beneficial for the systems that needs the battery cells balanced in a short time, for example the scheduled super-fast charging programs. The long-term balancing speed comparison between the conventional C2LV balancing and C2C + C2LV direct balancing is given in the experiment results section.

### 3.5.2 C2C and LV2C

This mode is triggered by the LV's no/low-load condition as well as the presence of significant difference between the SOCs of two neighboring cells in the same HFB. LV battery and high-SOC cell merge their energy to charge the low-SOC cell. As a result, the bias among HV battery cells will be eliminated faster than the LV2C-only techniques. The improvements might be subjective to the battery status, but the C2C path will boost up the balancing speed with a reasonable amount of time.

### 3.5.3 C2LV-Only

If the neighboring cells are out of balance under conditions, e.g. (1) minor imbalance, (2) LV loads require all cells to provide maximum viable power, or (3) balancing speed is not prioritized, it is more reasonable to discharge both cells simultaneously but in different C-rates . Therefore, the initial SOC bias is gradually compensated due to the C-rate difference while charging LV battery

or powering LV loads.

### 3.5.4 C2C-Only

The featured power flow direction is specifically available in the proposed topology, as cell 1 and cell 2 share the common DC current path blocked from secondary side with the primary side of the transformer. This mode is activated when neighboring cells are out of significant balance and LV system is offline. Unlike the other balancing topology to achieve C2C balancing direction indirectly, the LV system is not required as the intermediate station to pass energy from one cell to another. Therefore, the unwanted electronics losses by transferring charges from cell 1 to LV and from LV to cell 2 can be omitted.

### 3.5.5 Corresponding realization of modes A, B, C and D

As discussed before, the $I_{\mathrm{DC}}$ can be controlled arbitrarily as long as the core is not saturated and the circuits can tolerate. As long as $I_{\mathrm{DC}} > 0$, i.e. $I_{\mathrm{cell1}} > I_{\mathrm{cell2}}$, cell 1 offers more energy, and vice versa. For example, if $I_{\mathrm{DC}} = 10$ A, it indicates that cell 1 supplies 10 A more current than cell 2. When $I_{\mathrm{DC}} > I_{\mathrm{cell1}}$, $I_{\mathrm{cell2}} < 0$ will happen naturally according to the circuit property. As a result, cell 1 is discharging while cell 2 is charging, despite that LV side is charging or not. Therefore, the DC current offset quantifies the balancing direction and speed.

**Mode A**

Given the discussion above, mode A requires that cell 1 supplies the energy (positive $I_{\mathrm{cell1}}$) and cell 2 absorbs the partial energy (negative $I_{\mathrm{cell2}}$) transferred from cell 1. It is feasible when $I_{\mathrm{DC}} > I_{\mathrm{cell1}} > 0$. In this case, $I_{\mathrm{cell1}}$ is definitely positive due to C2LV direction of power flow.

**Mode B**

Except for the LV2C power flow, mode B is similar with mode A in terms of the behavior of cell 2. Mode B requires LV2C power flow direction which is the result of negative phase shift $d$.

The $I_{DC}$ inequality conditions for this mode preserve as mode A.

Table 3.1: Feasible balancing modes and corresponding power flow

| Mode | Conditions | Charging | Discharging |
|---|---|---|---|
| C2C+C2LV | $I_{DC} > 0$ ($d > 0$) | LV | Cell 1 and 2 |
| C2C+LV2C | $I_{DC} > I_{cell1} > 0$ ($d < 0$) | Cell 2 | Cell 1 and LV |
| C2LV only | $I_{cell1} > I_{DC} > 0$ ($d > 0$) | LV | Cell 1 and 2 |
| C2C only | $I_{DC} > I_{cell1}$ ($d = 0$) | Cell 2 | Cell 1 |

**Mode C and D**

The cell 2 is not being charged in this mode. Conversely, energy is needed from cell 2. Therefore, the condition is changed to $I_{cell1} - I_{DC} > 0$ so that cell 2 outputs power instead of absorbing power. The other requirements for cell 1 and direction of power flow remain the same as mode A. For the C2C-only mode, phase shift is zero while the DC current is maintained larger than $I_{cell1}$. The modes discussed above and corresponding control conditions are summarized in Table 3.1.

## 3.6 Design procedure

The circuit parameters will determine the power capability. The design procedures of two important components are given here. In addition, system-level design considerations are explained, including power rating and balancing capability.

### 3.6.1 Output capacitor design

As the rectified leakage inductor current $i_{lk2}$ is fluctuating within a large range due to the switching shown in Fig. 3.13, the LV loads, however, require relatively constant input. The capacitive

filtering is added to refine the original current waveform in order to deliver roughly constant current to the output. The ECM of the output stage and its waveform is shown in Fig. 3.13 Ideally, the output capacitor $C_o$ will absorb the AC component in $i_{lk2}$ and remain the DC component to the LV loads. By subtracting the DC component from $i_{lk2}$, the ideal capacitor current is drawn in the Fig. 3.13. The capacitor voltage is governed by the capacitance definition $\Delta V = \Delta Q/C$.

Since the voltage ripple $\Delta V$ needs to be restricted within a negligible range (1% of operating voltage in this work) in order to fulfill the assumption that the output voltage is roughly constant during the circuit analysis , the capacitance is required to be adequate to absorb the energy $\Delta Q$ that causes the capacitor voltage fluctuating.

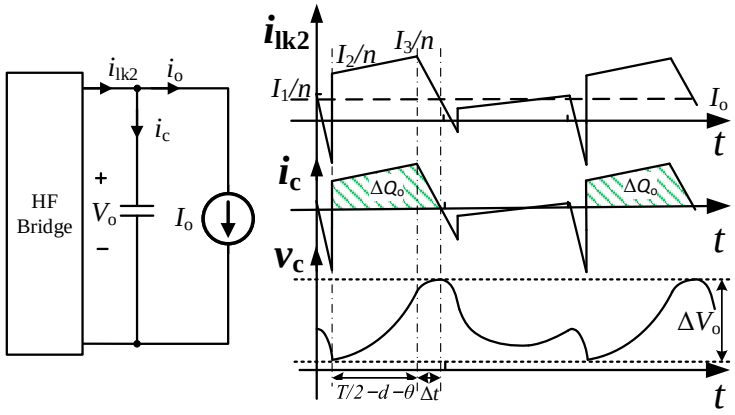



Figure 3.13: Filtering capacitor design, left: equivalent circuit focusing on output, right: output current and voltage waveforms

The charges that elevate the cap voltage is a result of the integrated shaded area of the capacitor current. It can be calculated by integrating the current over the period, resulting in $\Delta Q_o$. Thus, the largest peak-to-peak voltage ripple happens when the $\Delta Q_o$ reaches the maximum. The geometry

analysis can be applied and the expression of $\Delta Q_o$ can be obtained:

$$\Delta Q_o = (\frac{T}{2} - d - \theta + \Delta t)\frac{(I_2 + I_3 - 2nI_o)}{2n} + \frac{\Delta t I_3}{2n} \tag{3.26}$$

$$\text{where } \Delta t = \frac{I_3/n - I_o}{K_3} \tag{3.27}$$

$$I_2 = -I_1 + K_1 d \tag{3.28}$$

$$I_3 = -I_1 + K_1 d + K_2(T/2 - d - \theta) \tag{3.29}$$

It can be seen that the initial inductor current $I_1$ is inversely proportional to the charge $\Delta Q_o$, so that the minimal $I_1$ will result in largest change in capacitor charge regardless of other dependencies. Due to highly coupled dependencies on phase shift $d$, duty cycle compensation $\theta$ and cell voltages $V_{\text{cell1}}$ and $V_{\text{cell2}}$, a parameter sweep is performed to find the optimal capacitance, as shown in Fig. 3.14. The voltage is swept within the following range: $3.5 \leq V_{\text{cell1}} \leq 4.2\ V$, $2.7 \leq V_{\text{cell1}} \leq 3.4\ V$. Phase shift is spanned from 0.1 to $(T/2 - d - \theta)$ while keeping $\theta$ constant based on Eq. (3.18).

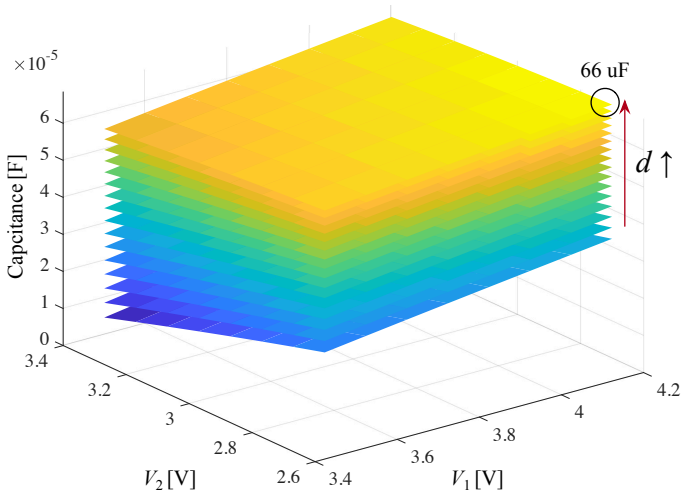



Figure 3.14: Required capacitance with different cell voltages and phase shift

The largest ripple is located when the cell voltage difference and output power are maximized, as the figure suggests 66 uF capacitance is required to remain current nearly constant. However, when cell voltages are similar, the required filtering capacitance to keep $I_o$ constant is reduced

to less than 10 uF. A comparison of filtering performance using different capacitance is given in Fig. 3.15, which is simulated in MATLAB/Simulink with PLECS toolbox. The cell voltages are selected to be [2.7 V, 4.2 V] as the worst case indicated. The simulated capacitances are 10 uF that is adequate for [3.4 V, 3.5 V] combination, and 66 u'//12121"F that can handle worst case scenario. The simulation results indicate that 66 uF is capable of stabilizing the output current reasonably well, whereas 10 uF capacitance will introduce large oscillation on the output current.

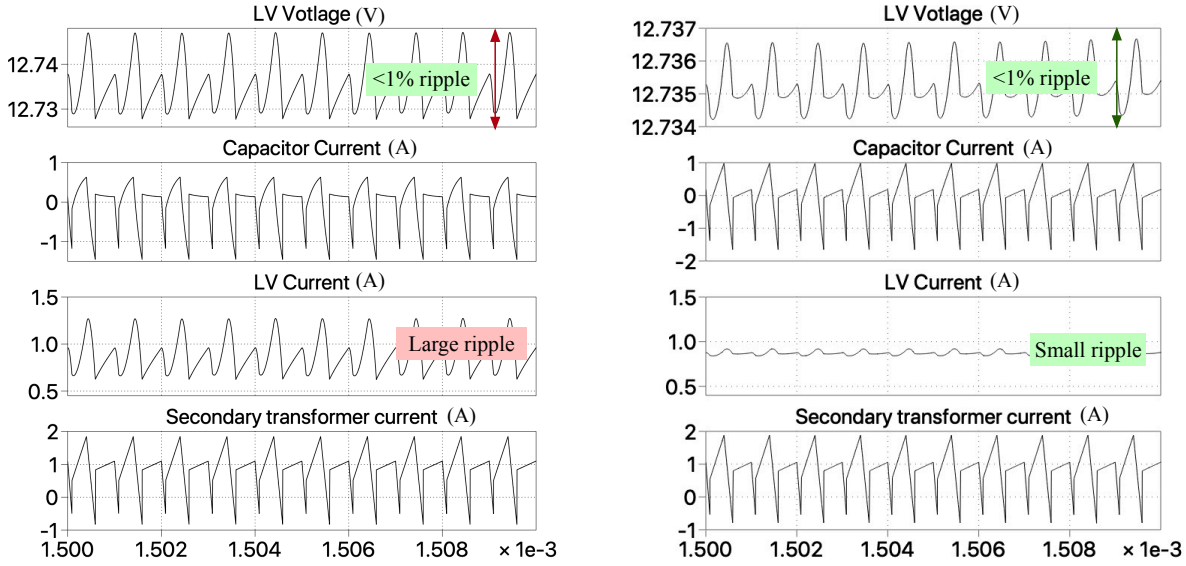



Figure 3.15: Simulation results of output current ripple with 4.2 V and 2.7 V cell voltages: (a) 10 uF filtering capacitance, (b) 66 uF filtering capacitance

### 3.6.2 Power rating and balancing capability

As the output power is limited by the leakage inductance in Eq. (3.20), optimally selecting the leakage inductance will achieve more compact design and reduced cost from over designing. Therefore, the rated operating condition should be defined before proceeding to transformer design.

**APM power rating**

Depending on the identity of the electric vehicle, the rated power for the auxiliary power modules is undetermined. The more luxury the vehicle is, the heavier LV loads could be as more power

is needed for extra LV functionalities, e.g. steering wheel and seat heating. From previous literatures, the rated current for APM is between 100-200 A, which translates to 1.2-2.4 kW power output [47], [61]. Therefore, for a 100-cell/module HV battery system, output power of 12-24 W for each cell/module to LV should be guaranteed. As two cells are managed by one HFB, the HFB should be rated for 24-48 W and can be designed accordingly based on Eq. (3.20). In this thesis, the HFB is designed to deliver a maximum power of 48 W in order for a generalized solution that can be implemented in most classes of EVs.

**HFB balancing capability**

The balancing capability is defined by the net current between two cells in one HFB and the net power between HFB modules. The net current $I_{\mathrm{DC}}$ in one HFB is rated at 5 A in the prototype that is shown in later section. Aside from C2C balancing, C2LV/LV2C will also assist equilibrium of the battery pack. One or more HFBs can operate at reversed power flow with respect to the rest of HFBs in order to balance the cells. A little buffer is given on each HFBs's rated power so that the power needed from the cells under balancing can be compensated by more power from the rest of cells. Therefore, a 2 W-room for each HFB is spared for C2LV/LV2C at maximum load, which yields a total maximum power of 50 W per HFB link. Note that the room for extra power can be tweaked by design easily.

Aforementioned parameters would simply provide a 0.1 C-rate current for balancing a 150 Ah EV battery pack, which is more than enough for "maintenance" balancing and comparable for "gross" balancing current level mentioned in [28], as well as other individual-converter topologies [17], [23].

### 3.6.3 Transformer design considerations

**Output power requirement**

The rated output power per HFB should be considered for transformer design. The conditions that physically/electrically limit the output power are switching period $T$, leakage inductance $L_{\mathrm{lk}}$,

and turns ratio $n$. On the other hand, the range of phase shift $d$ and the duty cycle adjustment $\theta$ are the controllable variables that tune the output power within the physical/electrical range.

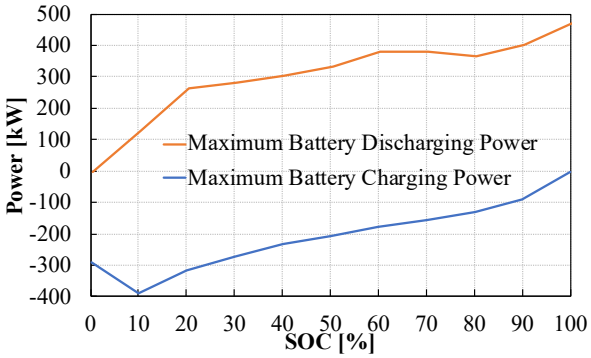



Figure 3.16: Maximum discharging power for Nissan Leaf [62]

Based on Eq. (3.20), the power spectrum can be obtained by sweeping phase shifts $d$ and the leakage inductance levels $L_{\text{lk}}$ under the worst scenario of cell voltages (2.8 V cut-off). However, this condition ($V_1 = V_2 = 2.8$ V) is unrealistic to provide the maximum power as the cells are defined as empty. Also at low SOC, the output power to auxiliary loads should be limited in order to ensure longer range and driving performance. Literature [62] reported a battery output power vs. SOC for Nissan Leaf, as shown in Fig. 3.16. Nissan Leaf is equipped with 80 KW synchronous motor and a 30 kW battery pack. Draining the last portion of battery with rated motor power will be sufficiently fast. In addition, battery SOC is limited to be used below 7.5% according to [62]. The remaining energy is reserved for emergency use. Therefore, it is reasonable to set the voltage range that provide the maximum power of the BB-APM to be greater than 20% SOC where a sharper output power reduction is observed in Fig. 3.16. Then the cell voltages are translated from OCV-SOC map generated from the experiments of the tested NMC cells, as shown in Fig. 3.17. When SOC = 20%, the OCV is measured to be 3.32 V which will be set as the minimum voltage to achieve maximum power of 50 W. Note that the voltage varies with the chemistries.

A sweep is performed to illustrate the determination of leakage inductance and operating frequency, as shown in Fig. 3.18. It shows the power capability of implementing the different transformers with a various of leakage inductance at two polarized conditions, i.e. 20% and 100% SOCs. It can be seen that not every design can guarantee a 48 W output at 20% SOC, e.g. the

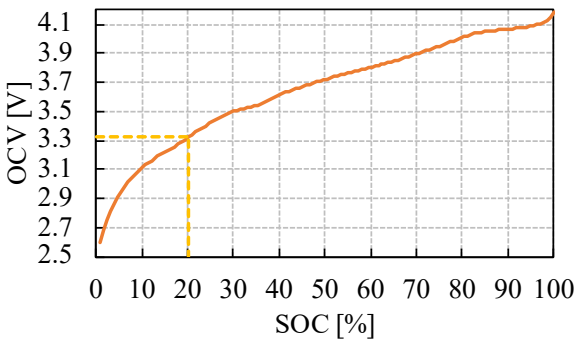



Figure 3.17: The OCV-SOC curve of the NMC cell

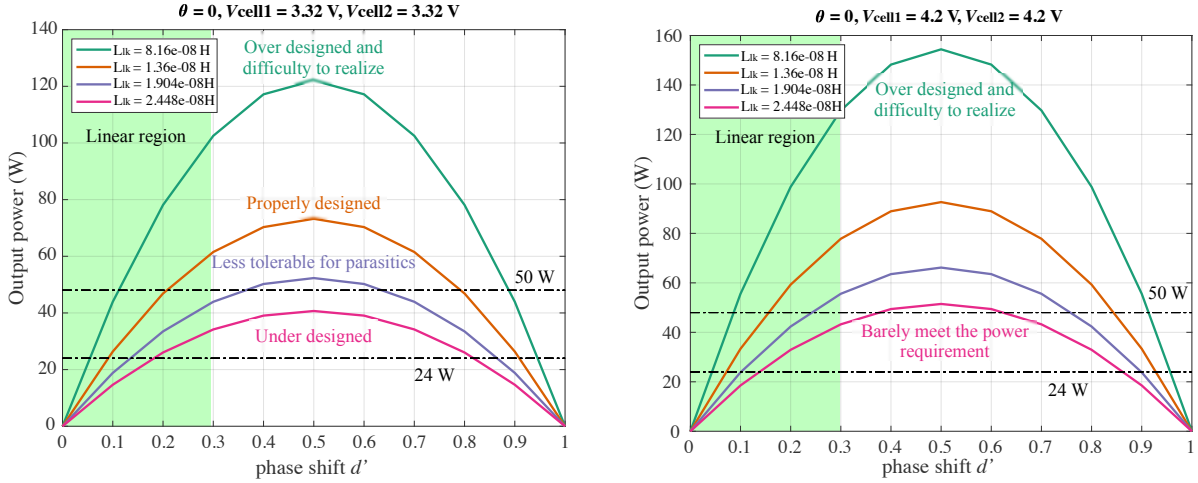



Figure 3.18: The power spectrum with a range of leakage inductance values at 500 kHz when battery cells are (a) at 20% SOC, (b) at 100% SOC

design with 24.48 nH of equivalent leakage inductance. Also, considering the parasitic inductance solely generated by the conduction path between transformer and switches, the design with 19.04 nH equivalent leakage inductance might not be sufficient to provide the output power of 48 W because the total inductance could exceed 20 nH that makes delivering 50 W unachievable. On the other hand, the power requirement can be easily satisfied when batteries are at higher SOCs even with larger inductance. However, in order to provide the maximum power between 20% to 100% SOC as designed, a slightly over designed transformer with 13.6 nH equivalent leakage inductance (6.8 nH primary leakage inductance) is selected in this thesis. The power spectrum helps locate the optimal leakage inductance to achieve rated power in the pre-defined operating range. For a

general design procedure, a flowchart for selecting the leakage inductance is given in Fig.3.19.

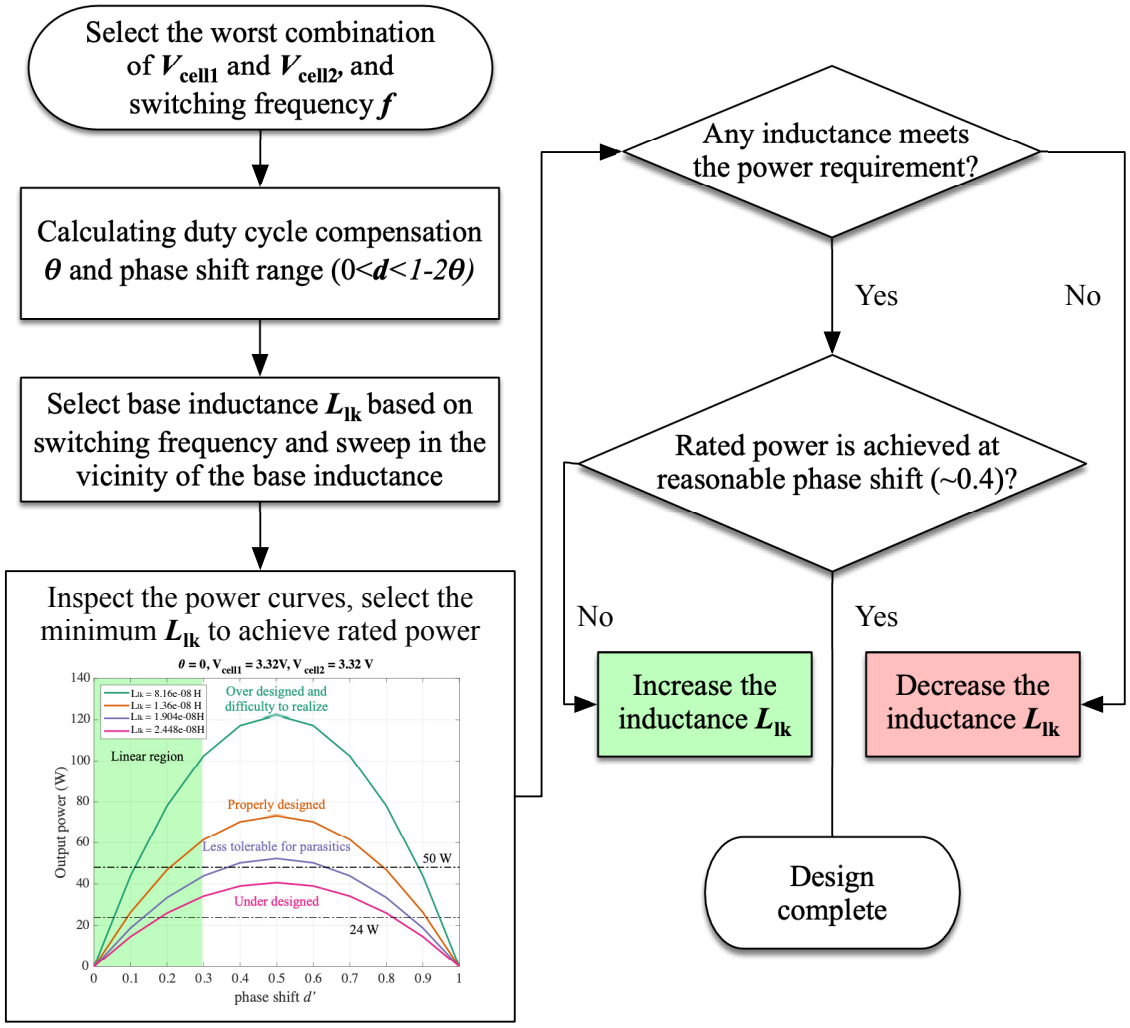



Figure 3.19: Flowchart of selecting leakage inductance to achieve rated power and peak current limitation

### Magnetic design considerations

In contrast with conventional transformer design, due to the presence of DC current in the leakage inductor for C2C operation, the core saturation needs to be carefully checked at rated C2C current level. If the core will be saturated at the rated current bias level, a better (higher saturation flux density) or larger core is needed. The overall design is a combination of designing a transformer and an inductor. The following inequality has to be satisfied to stay away from core

saturation:

$$I_{\mathrm{DC}} < \frac{(B_{\mathrm{sat}} - \Delta B/2) \times MPL}{0.4\pi\mu_{\mathrm{r}}\mu_0 N} \tag{3.30}$$

where $B_{\mathrm{sat}}$ is the maximum flux density that the core can operate without saturation, $\Delta B$ represents the peak-to-peak flux swing induced by periodically alternated square-wave voltage applied to the primary side of the transformer. *MPL* indicates the magnetic path length, which is normally given by the manufacturer. $\mu_{\mathrm{r}}$ and $\mu_0$ are the relative permeability respect to free space and permeability of the free space, respectively. $N$ is the number of turns on primary side.

Even if the transformer for HFB needs to operate at a DC current without saturation, the design barely induces difference compared to conventional transformer design in terms of losses and design complexity, such as the one in [17]. Transformer losses consist of core and copper losses. The winding property contributes to copper loss. The core loss is determined by the hysteresis effect of the core material which hardly relates to where the hysteresis loop starts (DC-operating point), as long as the peak/valley current will not drive the core to saturation. Therefore, the only trade-off when designing the transformer for HFB is the airgap/material as inducing airgap increases the DC current carrying capability for the core, or simply a better material with high saturation flux density.

Even though a precise leakage inductance can be achieved and validated in the computer aided programs like ANSYS/Maxwell or JMAG, the manufacture variation can be introduced to degrade the coupling between primary and secondary, leading to higher/lower leakage inductance than designed. The rated power requirement might not be guaranteed due to the change of leakage inductance. But it should not be worried, the advanced control strategy like variable frequency [63] can be adopted to overcome the short of power and provide other benefits like extended soft-switching range and smaller peak and RMS current.

## 3.7 Transformer design

The transformer parameters play an important role in the entire circuit operation and determine the output power at a given operating frequency. Therefore, a careful design of the transformer is required to have a tight control over the power capability and efficiency. In addition, the leakage inductance should be cautiously modeled since the discrete inductor is integrated in the transformer.

### 3.7.1 Core material selection

The material spectrum in terms of operating frequency and power loss density is normally given by the core manufacturer. The core material supplier in this thesis is chosen to be Ferroxcube as it provides various of Ferrite cores that are suitable for high-frequency switching operations compared to laminated silicon steel or powered metal due to lower losses. The material spectrum provided by Ferroxcube [64] is given in Fig. 3.20 and used to select the proper material model. The higher $f \times B_{\max}$ value is, the higher saturation flux density is at high operating frequency, i.e. the less likely the core will be saturated. The target operating frequency is between 500 kHz and 1 MHz. Therefore, 3F45 is selected to be a sufficient balance between performance and cost whereas cost will be compromised if 3F5 or 4F1 is used. Due to the availability of the 3F45 core material, the variant 3F46 is used and the property is similar compared with 3F45.

### 3.7.2 Core size selection using area product method

One of the challenges designing the transformer starts from proper core sizing. Neither should not the core be excessively bulky as the core loss increases with the volume, nor it should be small because the windings need to fit in. There are different approaches to estimate the core size based on power capability, such as core-geometry method ($K_{\mathrm{g}}$ coefficient) and area product (AP) method [65], [66]. The $K_{\mathrm{g}}$ coefficient determines the regulation ($r$) and energy handling capability, which

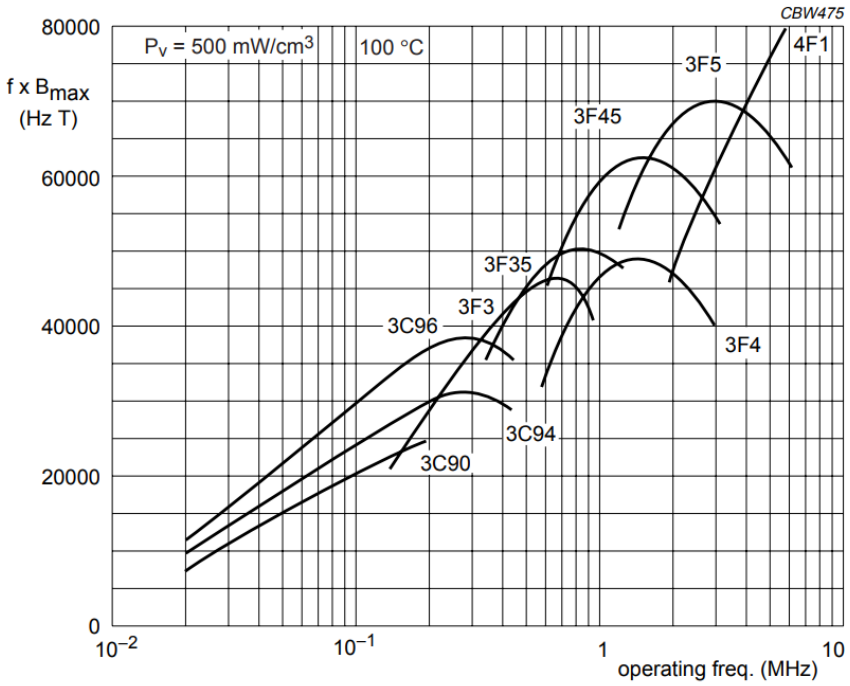



Figure 3.20: The material spectrum used to select core material [64]

is defined in Eq. (3.31).

$$
\begin{aligned}
r &= \frac{P_{\mathrm{t}}}{2K_{\mathrm{g}}K_{\mathrm{e}}} \\
K_{\mathrm{g}} &= \frac{W_{\mathrm{a}}A_{\mathrm{c}}^2K_{\mathrm{u}}}{MLT},\ [cm^5] \\
K_{\mathrm{e}} &= 0.145K_{\mathrm{f}}^2B_{\mathrm{pk}}^2f^2(10^{-4})
\end{aligned}
\tag{3.31}
$$

where $K_{\mathrm{f}}$ is waveform factor which is 4 for square voltage waveform. The apparent power is denoted as $P_{\mathrm{t}}$. $MLT$ represents mean length per turn. $K_{\mathrm{u}}$ is the window utilization factor which is the ratio of effective copper area and window area. The effective cross section area of the core is defined as $A_{\mathrm{c}}$ [cm$^2$] as well as window area of the core $W_{\mathrm{a}}$ [cm$^2$]. The peak flux density swing is $B_{\mathrm{pk}}$. Switching frequency $f$ plays important role in $r$, as it contributes to the factor $K_{\mathrm{e}}$ by a significant amount. The regulation can be configured as copper loss regulation or voltage regulation depending on the definition of regulation. Since $K_{\mathrm{g}}$ coefficient and AP are similar concepts and interchangeable, AP method is adopted to design the transformer in this thesis.

The AP method also correlates the electrical power requirement with the core geometrical power handling capability to help define whether the size of the core can satisfy the power require-

ment of the transformer:

$$A_p|E = \frac{P_t 10^4}{(B_{pk} J_{rms} K_u K_f)}, \ [cm^4] \tag{3.32}$$

$$A_p|G = A_c W_a, \ [cm^4] \tag{3.33}$$

where the subscriptions $E$ and $G$ represent electrically required AP and geometrically provided AP, respectively. $A_p|E$ is related to the circuit parameters: $J_{rms}$ - RMS current density $[A/cm^2]$, On the other hand, the geometrical AP is a function of effective cross section area of the core $A_c$ and window area of the core $W_a$. If $A_p|G \geq A_p|E$, the specific core can be passed to the next-step validation. Otherwise, the core is too small for the required power, and thus a larger core is needed or a paralleled core is required. Paralleling more cores of same size increases the effective area of the core $A_c$ and thus more AP that can be achieved. Some time it is more cost- and size-competitive compared with the larger core.

Table 3.2: Parameters for calculating the $A_p|E$

| **Parameter** | **Value** |
|---|---|
| $P_{VA}$ [W] | 510 |
| $B_{pk}$ [mT] | 50 |
| $J_{rms}$ [A/cm$^2$] | 2000 |
| $K_u$ | 0.2 |
| $K_f$ | 4 |

The parameters that are used to design the transformer are given in Table 3.2. The required AP is 0.1594 cm$^4$ or 1594 mm$^4$, which is then compared with the core geometry AP. Three different sizes of cores are initially selected and summarized in Table 3.3. Datasheet-specified core effective cross section area $A_c$ and window area $A_w$ are multiplied to obtain geometric AP, according to Eq. (3.33). The first core size EE14/3.5/5 is not sufficient to provide required power capability based on its AP. On the other hand, the rest two cores are suitable for further investigation as they are larger than 1594 mm$^4$.

Table 3.3: Geometry parameters of some core candidates

| | $A_c$ [mm$^2$] | Window width [mm] | $A_w$ [mm$^2$] | $A_p = A_e \times A_w$ [mm$^4$] | $V_e$ [mm$^3$] | $l_e$ [mm] |
|---|---|---|---|---|---|---|
| EE14/3.5/5 | 14.5 | 4 | 16 | 232 | 240 | 16.4 |
| EE22/6/16 | 78.5 | 6.45 | 37.76 | 2964.2 | 2100 | 26.1 |
| EP38/8/25 | 194 | 11.7 | 21.85 | 4238.9 | 8460 | 43.7 |

However, the decision cannot be simply made due to smaller size of core EE22/6/16. Another consideration is the winding layout:

**Trace width**

Certain printed circuit board (PCB) trace width is required to guarantee not overheated board.The worst-case primary and secondary RMS currents can be obtained applying design boundaries into Eq. (3.25). Based on previous analysis, the boundaries for locating the worst case scenario is given

$$\min_{-I_{\text{lkx,rms}}} \; -I_{\text{lkx,rms}} \;\; \text{such that} \begin{cases} 3.32\ \text{V} \le V_1 \le 4.2\ \text{V}, \\ 3.32\ \text{V} \le V_2 \le 4.2\ \text{V}, \\ 12\ \text{V} \le V_{LV} \le 14\ \text{V}, \\ 30\ \text{W} \le P_o(d) \le 50\ \text{W} \end{cases} \tag{3.34}$$

Combining the simulated resistances and worst-case primary and secondary RMS currents, the worst AC copper loss is located at operating condition of $V_{\text{cell1}} = V_{\text{cell2}} = 3.32$ V, $V_{\text{LV}} = 12$ V, $P_o = 50$ W.

For primary side carrying maximum RMS current of 52.4 $A_{rms}$ , 9.5 mm trace width for external traces is mandatory with a temperature increase of 40 °C. Internal traces requires wider traces to carry the same amount of current with the same temperature rise – 25 mm trace width. The secondary side needs to carry maximum 10.5 A, which translates to a trace width of 2.88 mm (rounded to 3 mm). So core EE22/6/16 is insufficient to fit a primary winding of 9.5 mm without paralleling traces. Therefore, EP38/8/25 is selected as the final core size.

### Winding structure

Minimal leakage inductance and more uniformly distributed currents in the windings can be achieved through interleaving the primary and secondary windings due to reduced proximity effect [65]–[67]. The core has limited space in the window of the core, by which the trace width of the PCB and total number of layers are constrained.

### Turn calculation

The amount of turns is determined by the maximum flux density swing within one period as well as the voltage amplitude applied on the terminals of the transformer. The simplified circuit of the primary side is illustrated in Fig. 3.21(a). The corresponding flux density variation induced by the applied voltage is drawn in Fig. 3.21(b). The voltage applied is assumed to be constant as the switching period is relatively short compared to the rate of the voltage changing, which is subject to the Faraday's Law:

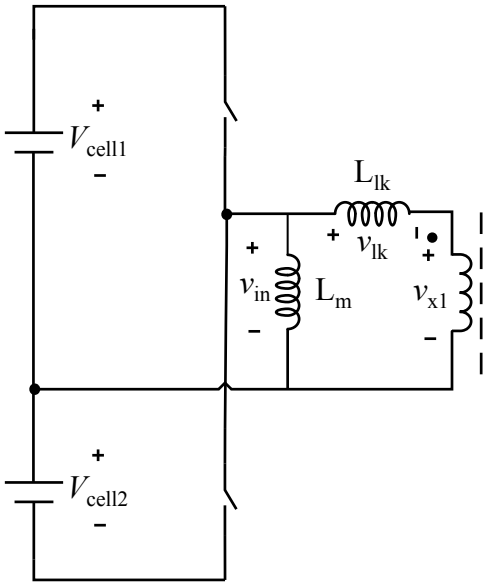
$$V = N_{\mathrm{p}} \frac{d\Phi}{dt} \approx N_{\mathrm{p}} \frac{A_{\mathrm{e}} \Delta B}{\Delta t} \tag{3.35}$$

$$\begin{aligned} N_{\mathrm{p}} &= \frac{V \Delta t}{A_{\mathrm{e}} \Delta B} \\ &\geq \frac{V}{2 f B_{\mathrm{pk}} A_{\mathrm{e}}} \end{aligned} \tag{3.36}$$

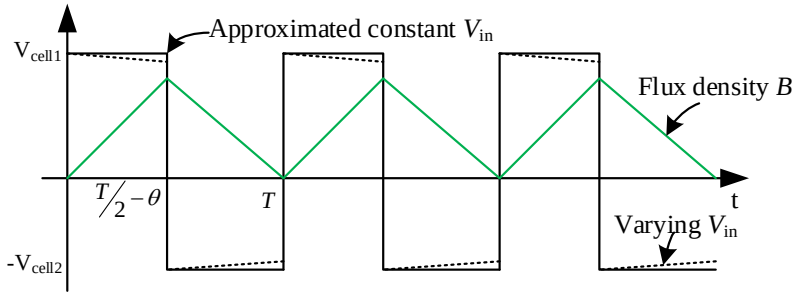
Substituting the operating points of the circuit into Eq. (3.36) yields the minimum number of turns on primary side:

$$N_{\mathrm{p}} \geq \frac{4.2}{2 \times 1\mathrm{MHz} \times 50\mathrm{mT} \times 194\mathrm{mm}^2} \geq 0.21 = 1 \tag{3.37}$$

The number of the secondary windings is then 5 turns. The equivalent maximum flux density swing is 10.8 mT when the number of the turn is selected as one.




(a)




(b)

Figure 3.21: (a) Primary-side simplified circuit, (b) Flux density due to applied voltage

### Leakage inductance approximation

The flux that is not linked between primary and secondary windings is defined as flux leakage, which induces a inductance named as leakage inductance. In other words, the energy that is not completely transferred from primary to secondary or vice versa is stored in the substance of leakage inductor. The diagram of the flux leakage is shown in Fig. 3.22. The leakage inductance can be theoretically calculated based on winding layout: non-interleaved, partially-interleaved and fully-interleaved [47], [68]. For the fully-interleaved planar transformer, the leakage inductance can be

estimated by

$$L_{\mathrm{lk}} = \mu_0 \frac{N_{\mathrm{p}}^2 l_{\mathrm{w}}}{M^2 b_{\mathrm{w}}} \left( \frac{\sum h_i}{3} + \sum h_{\Delta} \right) \tag{3.38}$$

where $M$ is the number of intersections between different windings. $l_{\mathrm{w}}$ is the length per turn of the winding, $b_{\mathrm{w}}$ is the width of the primary winding, $h_i$ is the copper thickness of $i$th layer.

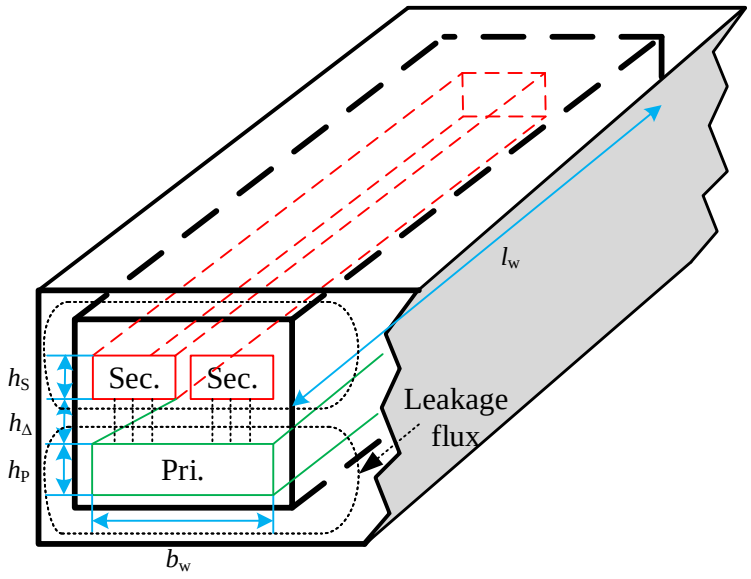



Figure 3.22: The diagram of flux leakage in a simplified 1:2 transformer

An example of the correlation between leakage inductance and the PCB parameters is shown in Fig. 3.23. It can be observed from the Eq. (3.38) and Fig. 3.23 that the leakage inductance can be slightly adapted with the adjustments on

- widths and lengths of traces
- number of the turns on primary side
- distance between windings
- winding structures, e.g. fully-interleaved windings

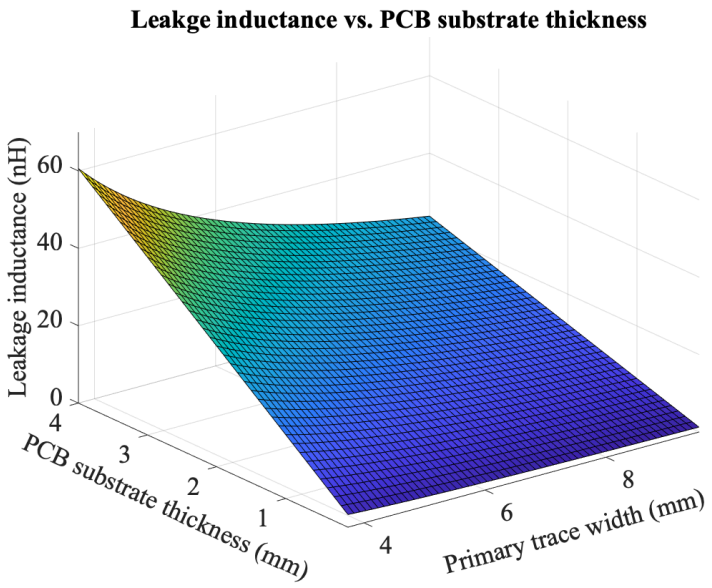



Figure 3.23: The correlation between leakage inductance and other PCB design parameters

### 3.7.3 Winding design and layout

As it is explained previously, the windings are preferred to be sandwiched/interleaved to minimize the leakage inductance and proximity effect. In order to interleave the windings of 1:5 turns ratio, the primary winding consists of two paralleled turns which separately link two layers of 2-turn secondary winding. One turn that is left of the secondary winding is placed in the center of the sandwich structure. The winding layout is illustrated in Fig. 3.24

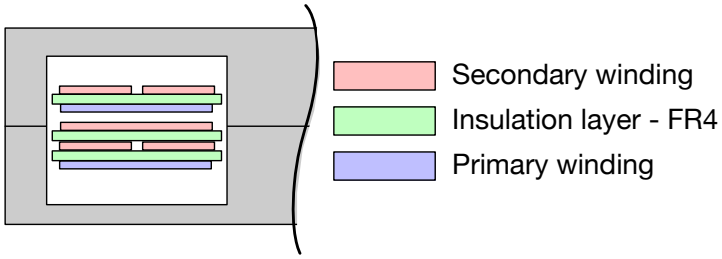



Figure 3.24: Winding layout

Based on the window size of EP38/8/25, the layout of the designed transformer is shown in Fig. 3.25, which will help analyze the copper loss.

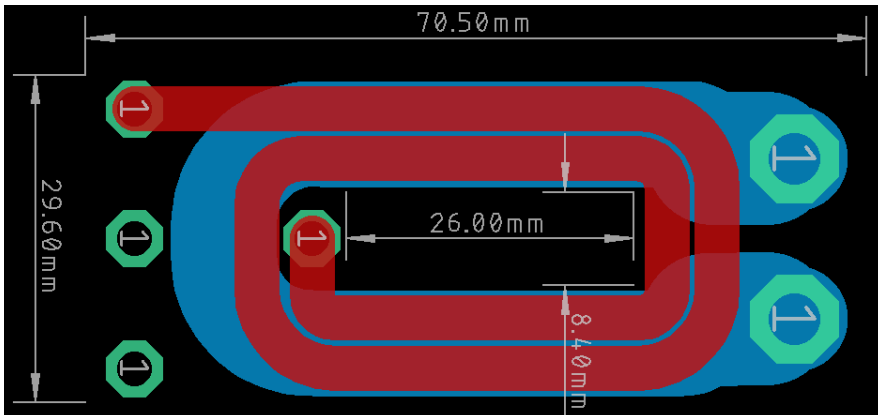



Figure 3.25: The dimensions for calculating the *MLT* for the designed transformer

### 3.7.4 Loss calculation

The losses generated from the transformer are the copper loss and the core loss. Depending on the switching frequency, the copper loss may vary due to the skin and proximity effects.

#### Copper loss

Resistance is inversely proportional to the cross area of the winding conductor. The conductor is normally chosen to be thicker when more current is needed to conduct while keeping the conductor cool. It is valid if the current carrying in the conductor is DC or low-frequency. Due to the Eddy current effect [65], [66], [69], the conducting current starts to concentrate more towards on the surface as the center current is canceled out by the induced eddy current, leading to the decreased effective conductor area and thus, the AC resistance is higher than the DC one.

A factor called Skin depth where the current density decreases to $1/e$ of the one on the surface [66] is given below to help reduce/avoid inconsistently distributed current when designing magnetic devices:

$$\delta = \sqrt{\frac{\rho}{\pi f \mu_0 \mu_r}} \tag{3.39}$$

where, $\rho$ is the resistivity of the copper, $1.7 \times 10^{-8}\Omega$·m. The permeability of free space and relative permeability to free space are denoted as $\mu_0$ and $\mu_r$, $4\pi \times 10^{-7}$ H/m and 1, respectively. The copper thickness is preferred as low as possible, and should not exceed $2\delta$. $2\delta$ for operating frequencies

from 10 kHz to 1 MHz is summarized in Table 3.4.

Table 3.4: Common maximum copper thicknesses for various frequencies

| $f_s$ [kHz] | 10 | 20 | 100 | 250 | 500 | 1000 |
|---|---|---|---|---|---|---|
| $2\delta$ [um] | 1304 | 922 | 412.4 | 260.8 | 184.4 | 130.4 |

As it can be seen from the Table 3.4, to operate at 1 MHz, the PCB thickness should not be larger than 130.4 um which translates to 3 oz copper (104.37 um). Otherwise, the AC resistance will be pronounced.

DC copper loss can be calculated based on the DC resistance and DC current carried by the copper trace, according to Eq. (3.40)

$$\begin{aligned} P_{\text{cu,DC}}^{\text{trans}} &= R_{\text{dc}}^{\text{trans}} I_{\text{DC}}^2 \\ R_{\text{dc}}^{\text{trans}} &= \rho \frac{l}{t_{\text{pcb}} w_{\text{pcb}}} = \rho \frac{MLT \cdot N}{t_{\text{pcb}} w_{\text{pcb}}} \end{aligned} \tag{3.40}$$

where, the thickness and width of the PCB trace are denoted as $t_{\text{pcb}}$ and $w_{\text{pcb}}$ in meter, respectively. The length of the copper trace $l$ can be approximated using the production of the number of turns and mean length per turn (MLT) for a planar PCB transformer with rectangular windings, as shown in Figs. 3.25 and 3.26. The calculation of MLT is then calculated as [65]

$$MLT = 2B + 2C + 2.82A \tag{3.41}$$

$$= 2 \times 8.4 + 2 \times 26 + 2.82 \times 10.6 \tag{3.42}$$

$$= 98.7 \text{ mm} \tag{3.43}$$

where parameters A, B and C are specified in Fig. 3.26. Therefore, the DC resistance of primary and secondary sides can be obtained

$$R_{\mathrm{dc,pri}}^{\mathrm{trans}} = \rho \frac{MLT \cdot N_{\mathrm{p}}}{t_{\mathrm{pcb}} w_{\mathrm{pcb,p}}} = 1.7 \times 10^{-5} \frac{98.7 \times 1}{0.11 \times 2 \times 9.5} = 0.8\ \mathrm{m\Omega} \tag{3.44}$$

$$R_{\mathrm{dc,sec}}^{\mathrm{trans}} = \rho \frac{MLT \cdot N_{\mathrm{s}}}{t_{\mathrm{pcb}} w_{\mathrm{pcb,s}}} = 1.7 \times 10^{-5} \left[ \frac{98.7 \times 4}{0.11 \times 3} + \frac{98.7 \times 1}{0.11 \times 9.5} \right] = 21.94\ \mathrm{m\Omega} \tag{3.45}$$

The DC resistances will only generated corresponding DC losses based on DC components of the currents. As can be seen from previous analysis, the DC component of the primary transformer current only comes from the C2C operation which is up to 5 A in this thesis. Therefore, the DC loss generated by primary winding is maximum 0.02 W. On the other hand, the secondary side does not contain the DC current component. As a result the total DC loss is

$$\begin{aligned} P_{\mathrm{DC}}^{\mathrm{trans}} &= P_{\mathrm{DC,pri}}^{\mathrm{trans}} = \max(I_{\mathrm{DC}})^2 R_{dc,pri}^{\mathrm{trans}} \\ &= 5^2 \times 0.0008 = 0.02W \end{aligned} \tag{3.46}$$

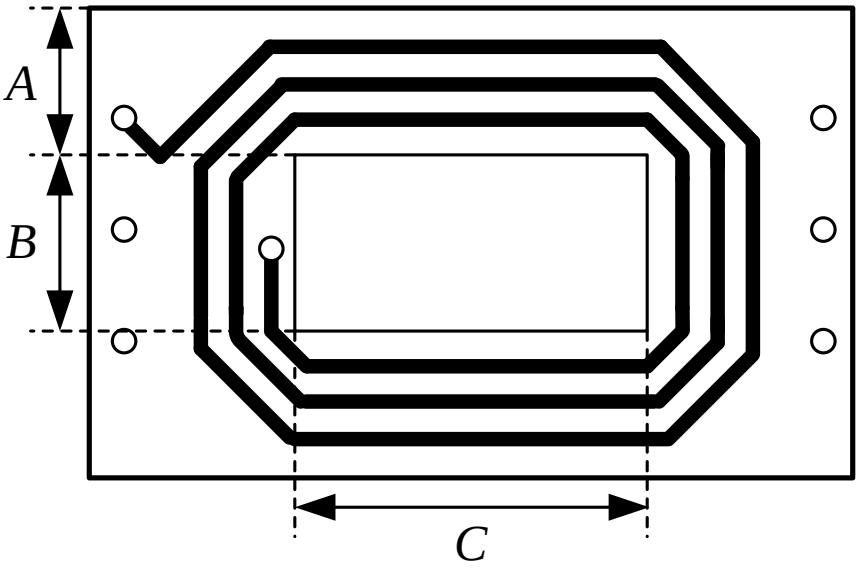



Figure 3.26: The dimensions for calculating the MLT for a rectangular winding

It can be seen that the losses generated by the DC components are roughly negligible. On the contrary, the AC components will dominate the losses since the transformer current contains

mainly AC components. The AC resistance of the windings can be approximated by Dowell's equations assuming an infinitely long current sheet [70], [71]:

$$F_{\mathrm{r}} = \frac{R_{\mathrm{ac}}^{\mathrm{trans}}}{R_{\mathrm{dc}}^{\mathrm{trans}}} = X\left[\frac{\sinh X + \sin X}{\cosh X - \cos X} + (2m-1)^2 \frac{\sinh X - \sin X}{\cosh X + \cos X}\right] \tag{3.47}$$

where $X$ is the ratio of trace thickness and skin depth at given operating frequency, i.e. $X = \frac{t_{\mathrm{pcb}}}{\delta}$. For a 3 oz copper, the factor $F_{\mathrm{r}}$ changes with the frequency for the proposed winding structure. Total number of consecutive layers from the same winding is defined as $m$. A plot illustrating the correlation between frequency and the ratio $\frac{R_{\mathrm{ac}}^{\mathrm{trans}}}{R_{\mathrm{dc}}^{\mathrm{trans}}}$ for a 3 oz copper design with a various number of layers is shown in Fig. 3.27. For a fully-interleaved design, i.e. $m = 1$, the AC resistance is not pronounced until hundreds of kHz range. Even at MHz, with the interleaving, the AC resistance is still low compared to the winding layout with more than 2 layers of same winding consecutively. However, this method will not be accurate if interleaving and paralleled windings are involved. In

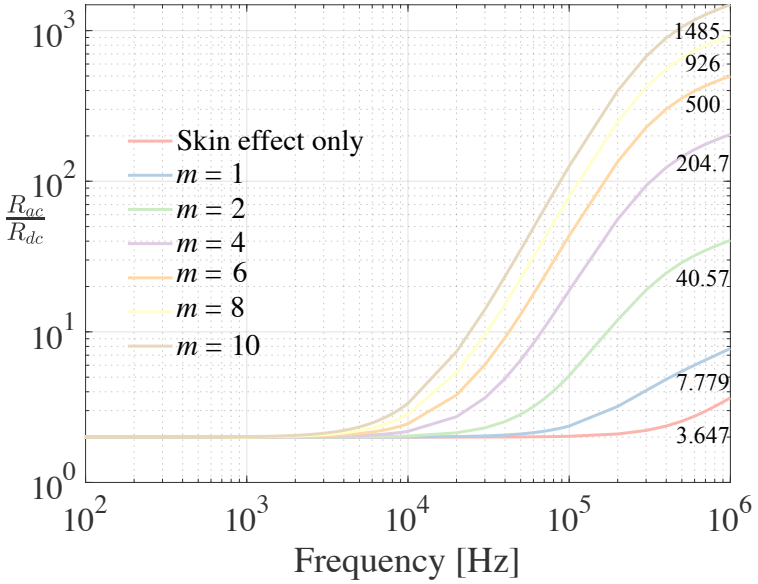



Figure 3.27: The distribution of $F_{\mathrm{r}}$ across a wide range of frequencies and different number of layers

order for accurate modeling of power loss for AC components, the AC resistances of both windings will be extracted from high-fidelity FEA simulations, which will be explained in a later section.

**Core loss**

The core loss is highly dependent on the core material and size, which is normally specified by the manufacturer as a plot of power loss density vs. flux density swing $\Delta B$ at different operating frequencies, as shown in Fig. 3.28. The Steinmetz core loss density equation is [47], [72], [73]

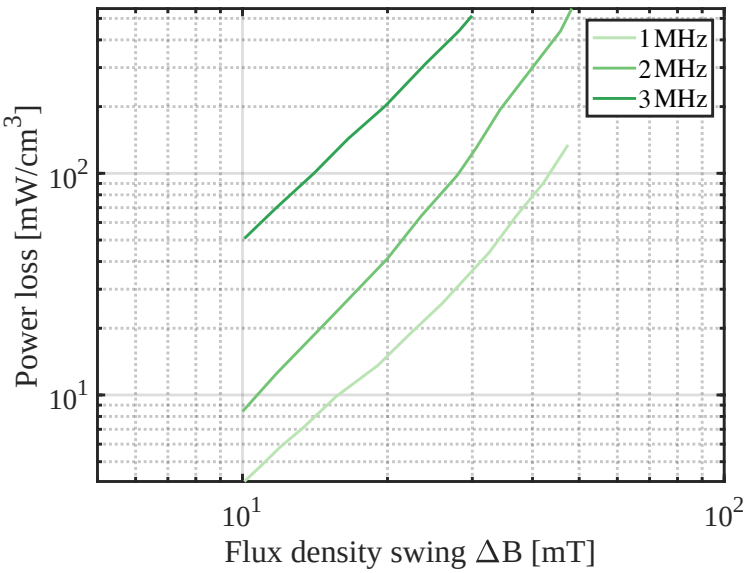



Figure 3.28: The core loss density vs. flux density swing at 1, 2, and 3 MHz switching frequency

$$P_{\text{fe}} = k f^{\alpha} \Delta B^{\beta} \tag{3.48}$$

Normally the Steinmetz Coefficients are not provided by the manufacturers directly,therefore some fitting techniques need to be applied to obtain them. In this thesis, the least square (LS) curve fitting technique is used to extract the coefficients of the core loss curve. As the transformer is designed for operating frequency around/below 1 MHz, only 1 MHz curve is fitted to increase the fitting accuracy instead of trying to fit the entire frequency range. The fitting result is shown in Fig. 3.29. The fitted coefficients are given in Table 3.5. Therefore, the core loss can be calculated by the maximum flux density swing and the switching frequency.

$$P_{\text{fe,max}} = 3.5 \times 10^{-3} \times 1^{3} \times 10.8^{2.7245} = 19.36 \text{ mW} \tag{3.49}$$

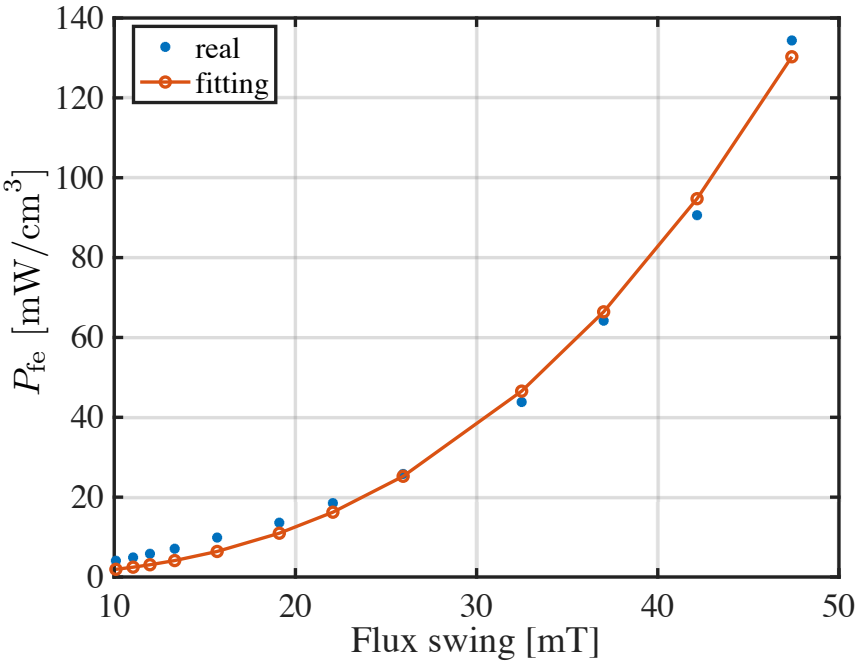



Figure 3.29: Core loss curve fitted at 1 MHz

Table 3.5: The extracted Steinmetz coefficients at 1 MHz

| Parameter | k | $\alpha$ | $\beta$ |
|---|---|---|---|
| Value | $3.5 \times 10^{-3}$ | 3 | 2.7245 |

### 3.7.5 Magnetization and leakage inductances

**Magnetization inductance**

The magnetization inductance is mainly determined by the core property and the winding lay out when the flux is well regulated in the core, which can be calculated through the following equation:

$$L_m = \frac{\mu_0 \mu_r N_p^2 A_c}{l_m} \tag{3.50}$$

where $l_m$ is the magnetic path length of the core which is specified by data sheet. It is considered significantly larger than the leakage inductance and thus, its effect on the circuit is negligible. For the chosen core and primary winding, the magnetization inductance is calculated as 5.05 uH.

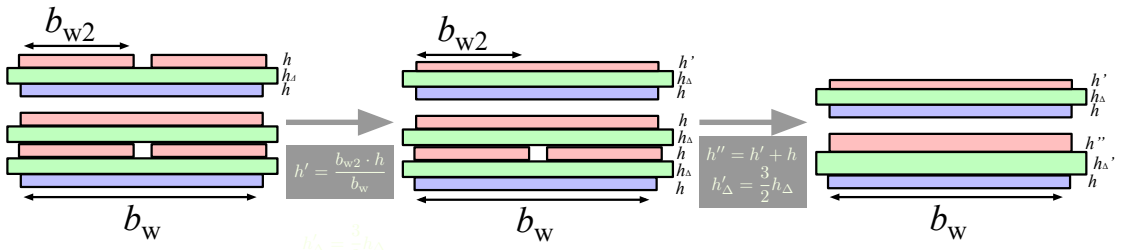



Figure 3.30: The steps to convert asymmetrical fully-interleaved structure to symmetrical fully-interleaved one

**Leakage inductance approximation based on partially-interleaved windings**

For asymmetrical fully-interleaved structure in this thesis as shown in Fig. 3.24, the parameters in Eq. (3.38) need to be adjusted. The assumption in deriving the leakage inductance for in [68] is the windings have the same trace width. On the contrary, in the proposed transformer layout, the widths of both windings are not identical.

If the volume of the conductor is maintained the same, the energy stored in the leakage will be identical. Therefore, the equivalent thickness for secondary windings to keep the width the same as primary one can be calculated as

$$h'_s = \frac{h_s \cdot b_{w2}}{b_w}, \tag{3.51}$$

where $b_{w2}$ is the trace width of the secondary winding. In addition, the layer 2 and 3 of the secondary windings are placed consecutively. They should lump into a structure of single layer of secondary with one layer of insulation in order to apply the Eq. (3.38). The process of translating the structure in Fig. 3.24 to a symmetrical fully-interleaved structure is shown in Fig. 3.30. Then, the Eq. (3.38) can be applied to the equivalent transformer layout in Fig. 3.30:

$$L_{lk} = 4\pi \times 10^{-7} \times \frac{1^2 \times 98.7}{3^2 \times 9.5} \left( \frac{3 \times 0.11 + 2 \times \frac{6}{9} \times 0.11}{3} + \frac{5}{2} \times 0.61 \right) = 7.3 \text{ nH} \tag{3.52}$$

### 3.7.6 Maxwell simulation

The designed transformer is precisely modeled in Ansys/Maxwell to conduct the simulation for characterization, as shown in Fig. 3.31. The correlation between magnetization/leakage inductance and FR4 thickness (winding distance) has been illustrated in Fig. 3.32 using Magnetostatic and Eddy current solvers. The magnetization inductance on primary and secondary sides is constantly distributed as the FR4 increases as it is directly related to the core properties and winding structure as shown in Eq. (3.50). On the other hand, the leakage inductance is highly dependent on the distance between the windings. To minimize the leakage inductance and increase the coupling, the windings should be placed as close as possible. However, a survey of PCB manufacturing capability for a 3 oz two-layer board shows the minimum thickness of 0.6 mm board, which yields a simulated leakage inductance of 6.7 nH.

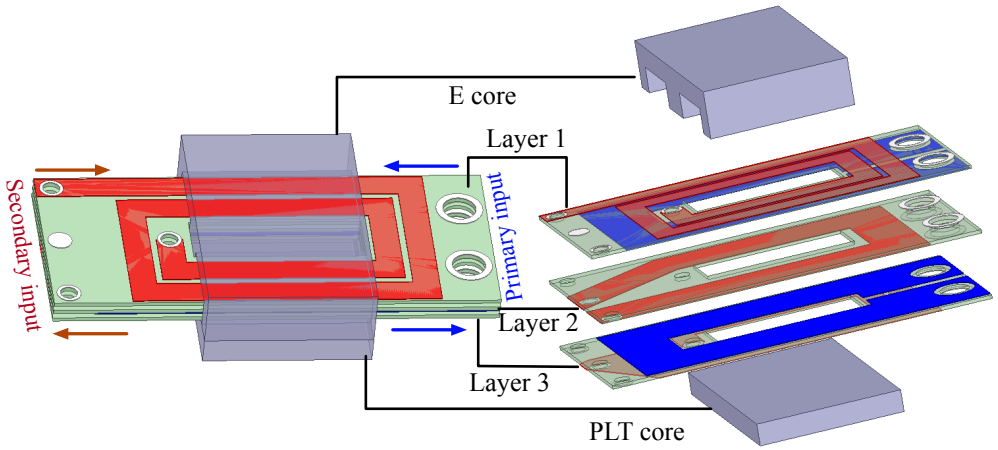
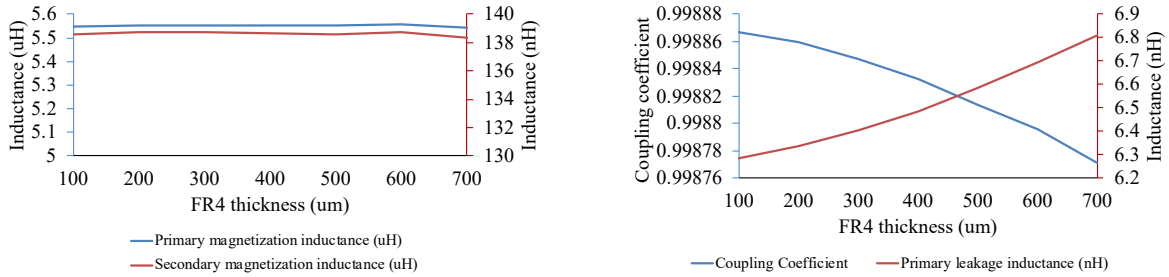


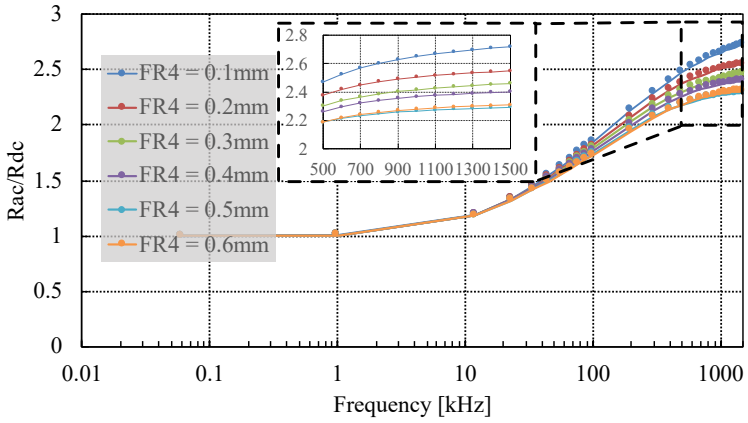

Figure 3.31: Maxwell simulation 3D model

The AC resistances are also extracted from Eddy Current solver, as shown in Fig. 3.33. It shows that the calculated DC resistances show the high agreement with the simulated results. In addition, it can be seen that the simulated AC resistances are roughly halved compared with the calculation using Dowell's Equations (3.47). The offset can be resulted from the non-idealities, such as the finite trace width, and paralleled primary winding. The results also show that the further apart windings are the less proximity effect is generated and thus lower AC resistance. Operating at typical 500 kHz and 1 MHz, the primary-side and secondary-side winding AC resistances are

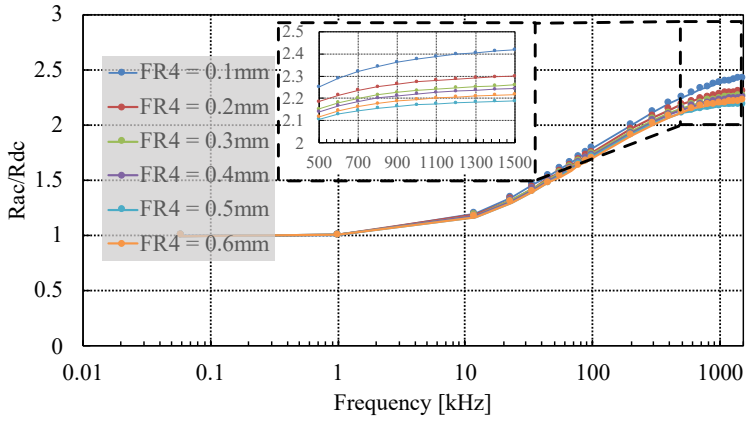



(a) (b)

Figure 3.32: The correlation between FR4 and (a) magnetization inductances, and (b) leakage inductance




(a)




(b)

Figure 3.33: The simulated $F_r$ at different frequency with multiple FR4 thicknesses on (a) primary side and (b) secondary side

given with simulated DC counterparts in Table 3.6. Based on previously calculated primary- and

Table 3.6: The simulated DC and AC resistances for primary and secondary windings with FR4 = 0.6 mm

| | Frequency [Hz] | Resistance [mΩ] |
|---|---|---|
| Primary winding | DC | 0.808 |
| | 500 k | 1.768 |
| | 1 M | 1.843 |
| Secondary winding | DC | 17.824 |
| | 500 k | 37.728 |
| | 1 M | 39.131 |

secondary-side RMS currents, the conduction losses can be calculated as

$$P_{\text{AC,pri}}^{\text{trans}} = R_{AC,pri}^{\text{trans}} \cdot I_{lk1,rms}^2 = 1.768\ \text{m}\Omega \times 52.38^2 = 4.85\ \text{W}, \tag{3.53}$$

$$P_{\text{AC,sec}}^{\text{trans}} = R_{AC,sec}^{\text{trans}} \cdot I_{lk2,rms}^2 = 37.728\ \text{m}\Omega \times 10.47^2 = 4.13\ \text{W}. \tag{3.54}$$

So the total copper loss generated from the transformer is

$$P_{\text{trans,cu}}^{\text{trans}} = P_{\text{DC}}^{\text{trans}} + P_{\text{AC,pri}}^{\text{trans}} + P_{\text{AC,sec}}^{\text{trans}} = 0.02 + 4.85 + 4.13 = 9.02\ \text{W}. \tag{3.55}$$

Note that this is the worst condition estimation. The power losses at rated or low load conditions are expected to be significantly less.

### 3.7.7 Experimental measurements

The assembled transformer is shown in Fig. 3.34. The open-circuit (OC) and short-circuit (SC) tests have been performed on it by a precision RLC meter to obtain the measurements of the resistance, magnetization inductance and leakage inductance along many frequency points, as shown in Fig. 3.35. The comparison of the calculation, simulation and measurements is summarized in Table 3.7. The result shows high consistency between calculation/simulation and experimental measurements.

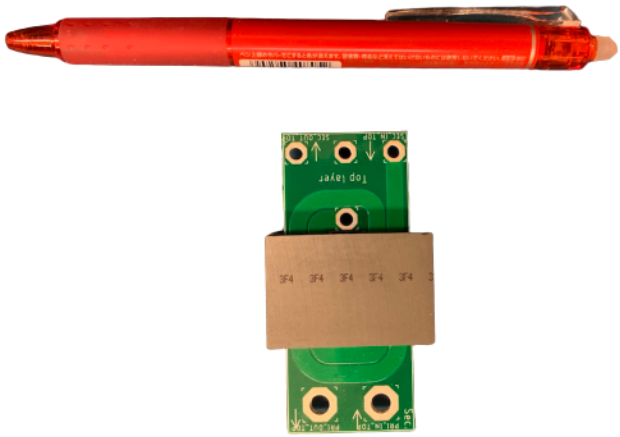
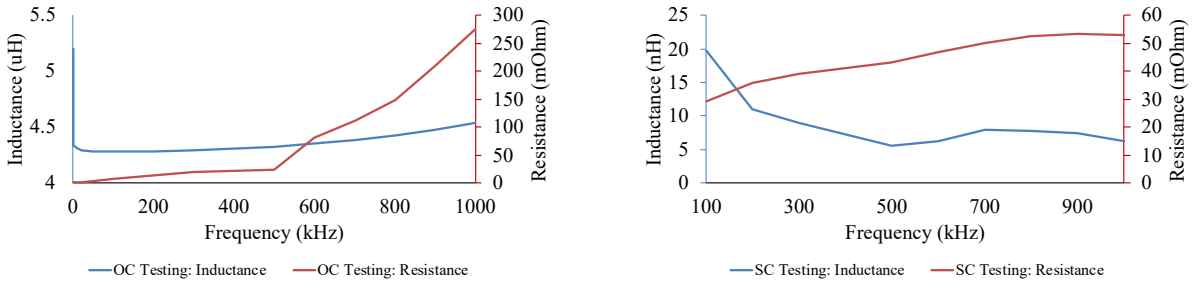


Figure 3.34: The assembled transformer for HFB

Table 3.7: Comparison of calculation, simulation and measurements of the transformer

| Parameters | Calculation | Simulation | Experiment |
|---|---|---|---|
| Magnetization inductance @ DC | 5.05 uH | 5.56 uH | 5.2 uH |
| Primary leakage inductance | 7.3 nH | 6.7 nH | 6.84 nH (averaged between 500 kHz -1 MHz) |




(a) (b)

Figure 3.35: Measurements of inductance and resistance (a) OC measurements, (b) SC measurements

## 3.8 Lower-level controller design

In order to guarantee the LV loads are powered properly, each HFB module should output any arbitrary power within the design limits depending on each cell's condition. Therefore, the feedback controllers should be installed on each HFB module to regulate the output power and the balancing process.

### 3.8.1 Higher-level controller with LV load regulation

The controller on each HFB, however, has limited vision on the information of LV battery and load. It might lead to over-stressing LV battery without a systematic control strategy on when and how much to charge/discharge the LV or power the LV loads. Therefore, a higher-level controller

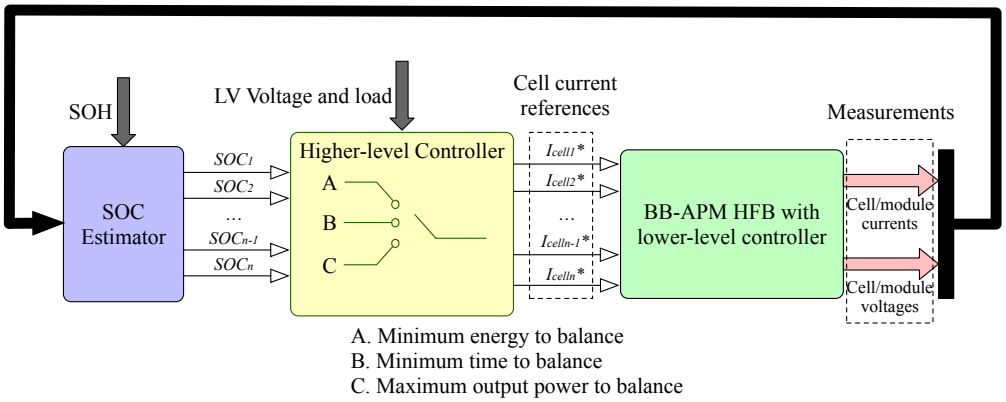



Figure 3.36: Higher-level controller distributing power demands to each local controller

shown in Fig. 3.36 that oversees and distributes the power needed and balancing actions for each HFB module is installed before each HFB with its own local controller. The center controller receives SOC and state of health (SOH) statuses from the state estimators that could be embedded in the HFB modules, as well as the LV battery status and load condition. Based on the feedbacks, the higher-level controller determines the current references for each cell and update them with the local controller to actuate the control. During the current determination process, intelligent optimization techniques (e.g. model predictive control) can be applied to achieve the SOC equilibrium with various objectives. Three commonly referred balancing cost functions are listed in the Fig. 3.36. It is assumed in this thesis the higher-level balancing control algorithm in [74] is used and the current references generated from the algorithm are passed to the lower-level controller. Therefore, in this thesis, only the detailed design process for lower-level controller is given. Each lower-level controller shown in Fig. 3.37 is responsible for regulating the current demand between two cells in one HFB.

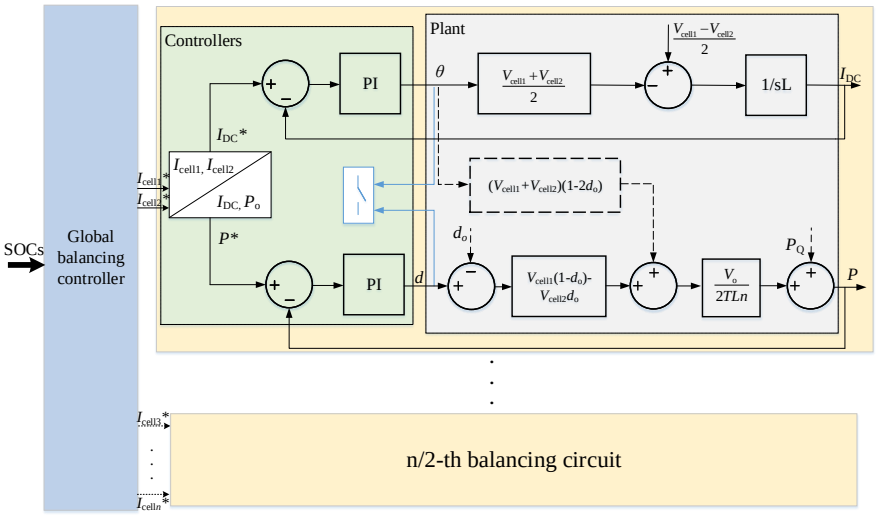



Figure 3.37: Diagram of lower-level controller

### 3.8.2 Lower-level controller reference translation

The cell currents $I_{\text{cell1}}$ and $I_{\text{cell2}}$, however, cannot be directly controlled since they do not have a direct relationship with the controllable variables $\theta$ and $d$. It is observed that DC offset current $I_{\text{DC}}$ and output power $P_{\text{o}}$ are linked with $\theta$ and $d$ in Eqs. (3.14) and (3.20). An intermediate transformation is needed from cell currents to the controllable variables. In the lossless case, input power is 100% transferred to output or the cells to be charging, which yields $P_{\text{o}} = P_{\text{in}} = V_{\text{cell1}} I_{\text{cell1}} + V_{\text{cell2}} I_{\text{cell2}}$. Therefore, given $I_{\text{DC}} = I_{\text{cell1}} - I_{\text{cell2}}$, the intermediate transformation matrix is derived as $\mathbf{T}$:

$$\begin{bmatrix} I_{\text{DC}} \\ P_{\text{o}} \end{bmatrix} = \mathbf{T} \begin{bmatrix} I_{\text{cell1}} \\ I_{\text{cell2}} \end{bmatrix} = \begin{bmatrix} 1 & -1 \\ V_{\text{cell1}} & V_{\text{cell2}} \end{bmatrix} \begin{bmatrix} I_{\text{cell1}} \\ I_{\text{cell2}} \end{bmatrix} \tag{3.56}$$

Consequently, in the lower-level controller, the reference of current distribution generated by the global controller is translated to the reference of $I_{\text{DC}}$ and $P_{\text{o}}$ by the transformation matrix $\mathbf{T}$ so that each cell's current can be controlled by regulating $I_{\text{DC}}$ and $P_{\text{o}}$.

### 3.8.3 Linearized power characteristics

It is observed that Eq. (3.20) has two controllable variables coupling together, which makes controllers hard to be designed and implemented. A reasonable method to decouple the nonlinear relationship is Taylor series expansion, which is used to linearize the expression in Eq. (3.20) around a quiescent point Q:

$$\begin{aligned} P_{\mathrm{o}} =& P_{\mathrm{o}}|_{\theta'_{\mathrm{Q}},d'_{\mathrm{Q}}} + \frac{V_{\mathrm{o}}T}{2L_{\mathrm{lk}}n}[(V_{\mathrm{cell1}} + V_{\mathrm{cell2}})(1-2d'_{\mathrm{Q}})\theta' \\ &+ (V_{\mathrm{cell1}}(1-d'_{\mathrm{Q}}) - V_{\mathrm{cell2}}d'_{\mathrm{Q}})(d'-d'_{\mathrm{Q}})] \end{aligned} \tag{3.57}$$

where $\theta'_{\mathrm{Q}}$ and $d'_{\mathrm{Q}}$ are the quiescent operation points for the control variables. They are normally set to be the steady-state conditions. $\theta$ is given by Eq. (3.18) which leads to a balanced leakage inductor current, and $d'_{\mathrm{Q}}$ is determined to deliver a certain level output power based on Eq. (3.20). A linearized power curve is compared with the original power curve in Fig. 3.38 for a specific circuit design, cell voltage and power levels, but it is general for other conditions.

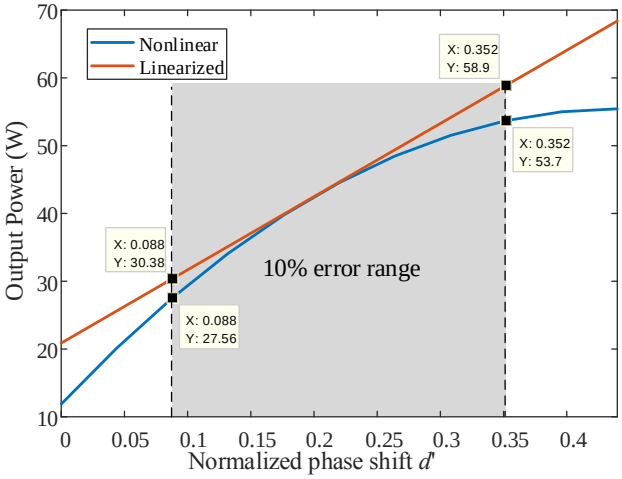



Figure 3.38: Comparison between linearized and original power curves

The plot shows the linearized power at $d'_{\mathrm{Q}} = 0.2$ has less than 10% error in a large phase shift range, varying from 0.09 to 0.352. It covers the majority of area if 40 W output power is required. Obviously, $d'_{\mathrm{Q}}$ can be selected accordingly if the power range is required narrower. This result will give enough information for intelligent controllers to react accurately.

### 3.8.4 Overall control strategy

Based on Eqs. (3.14) and (3.57), the diagram of lower-level controller is depicted by the green block in Fig. 3.37. Two reference currents for the corresponding cells in one HFB device are fed into the lower-level controller. After translating them into reference DC offset current and output power, the measurements are compared and their error signals are transmitted to two PI controllers. The two control variables from PI controllers are driving the gates of the switches to realize the control process.

The dashed block between duty cycle adjustment and phase shift PI controllers is cross-coupling term from $\theta$. One can design a PI controller to compensate those terms; however, in this thesis, those terms are treated purely as disturbances and the PI controller is considered robust to eliminate the disturbances in closed-loop control. Therefore, only forward path is concerned when designing the PI controllers.

Bode plots are applied to sketch the design of two PI controllers. It is noted that if the compensator gain at the switching frequency is too high, then these switching harmonics are amplified by the compensator, and can disrupt the operation of the PWM [75]. Normally, the cut off frequency requires at least less than 10 % of switching frequency, e.g. cutoff frequency at least less than 50 kHz if switching at 500 kHz. For the PI controller regulating $\theta$, it can be obtained from the block diagram in Fig. 3.37 that the transfer function of the open-loop system is:

$$G_1 = G_{\mathrm{PI}_1} G_{\mathrm{theta}} = -\frac{K_{\mathrm{P}} s + K_{\mathrm{I}}}{s} \frac{V_{\mathrm{cell1}} + V_{\mathrm{cell2}}}{2 L_{\mathrm{lk}} s} \tag{3.58}$$

The Bode plot of $G_1$ with gain and phase margins is shown in Fig. 3.39, where $K_{\mathrm{P}}$ and $K_{\mathrm{I}}$ are given in Table 3.8. The two extreme conditions are included: $\max(V_{\mathrm{cell1}} + V_{\mathrm{cell2}})$ and $\min(V_{\mathrm{cell1}} + V_{\mathrm{cell2}})$. It can be seen from the Fig. 3.39 that gain and phase margins deviate insignificantly for two extreme conditions; so that the open-loop system has a nearly constant cutoff frequency at 33 kHz while the system is switching at 500 kHz, which satisfies the criteria of cut-off frequency locating at least less than 10% switching frequency. The step response to the closed-loop system is also given to

show the performance of the controller. It can be seen that the controller follows the step response quickly and accurately without any overshoot. The same analysis can be also applied to the PI controller that regulates phase shift; the PI gains for two PI controllers are given in Table 3.8.

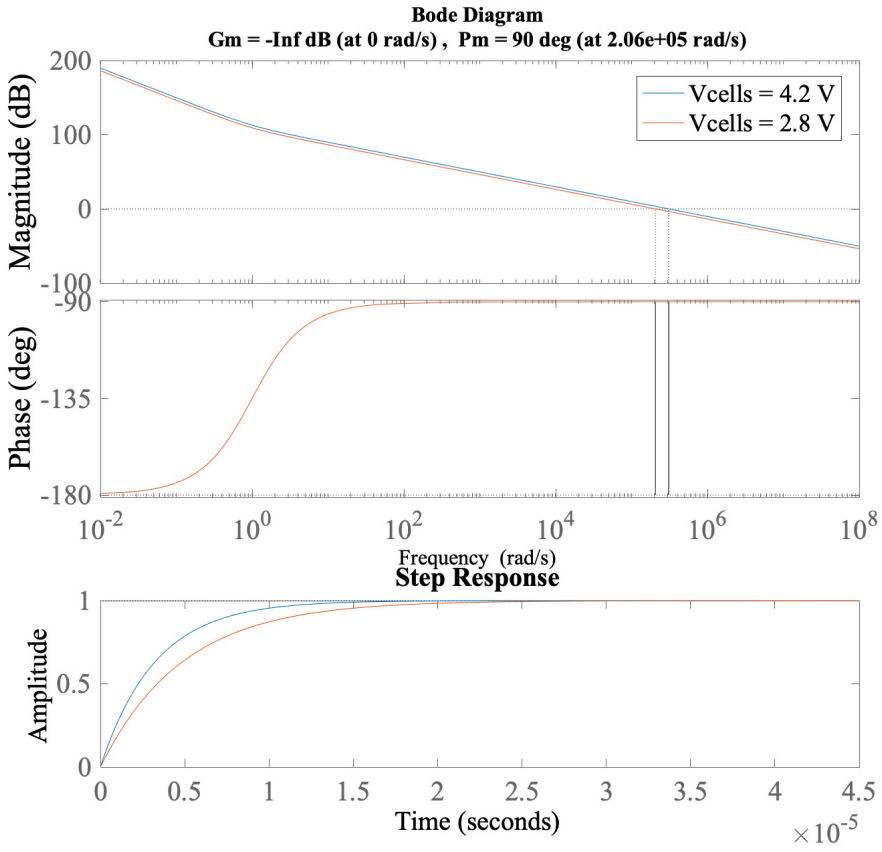



Figure 3.39: The Bode plot for the PI controller of $\theta$ and its step response

Table 3.8: PI controller gains

| | |
|---|---|
| Gains of $\theta$ controller | $K_P = 0.001$<br>$K_I = 0.001$ |
| Gains of $d$ controller | $K_P = 0.005$<br>$K_I = 0.01$ |

### 3.8.5 Simulation

The controllers are firstly tested and validated on a detailed circuit model, which is translated from the topology in Fig. 3.2 based on MATLAB/Simulink with PLECS electronic toolbox. This is aiming at testing all possible operating conditions and their transient responses from one to another before implementing on a real hardware test bench. Any unexpected faults or design errors should be captured and corrected to avoid the catastrophic failures on the real hardware.

As the cells balance/deviate, the reference current distribution is adjusted by the central controllers frequently to either deliver the desired output power or speed up balancing process. The possible current distribution should include the modes listed in Section 3.5. They are specified in Table 3.9.

Table 3.9: References for test conditions

| Condition # | 1 | 2 | 3 | 4 |
|---|---|---|---|---|
| Cell Currents (A) | 5 and 3 | 5 and −2 | −2 and −6 | 5 and −5 |
| Voltages (V) | | Cell 1: 4.2<br>Cell 2: 3.3 | | |
| Output Power (W) | 30.9 | 14.4 | −28.2 | 0 |
| Simulated mode | C2LV + C2C (+) | C2LV + C2C(−) | LV2C | C2C |

The listed four operation modes are verified in Fig. 3.40. At first, the balancing system is given with current references 5 A and 3 A from cell 1 and cell 2, respectively, which yields 30.9 W output power to LV. Adjusting $d'$ and $\theta'$, the controllers converge to the correct references swiftly and accurately, as shown in Fig. 3.40.

Once the system operates in steady state, the current references step change to 5 A and −2 A at approximately 250 us. Output power of 14 W is generated with the new current demand. Positive power flow leads to positive phase shift. Therefore, $d'$ decreases to a smaller value than previous $d'$ . On the other hand, $\theta'$ just subtly fluctuates around previous steady-state condition to reach the new level of leakage inductor current, i.e. $I_{\mathrm{DC}} = I_{\mathrm{cell1}} - I_{\mathrm{cell2}} = 5 - 3 = 2A \rightarrow 5 - (-2) = 7A$. Since two cells' voltages did not change, the duty cycle adjustment in a balanced system would not

change based on Eq. (3.18). In the simulation, $\theta'$ remains the same value compared with previous condition in steady state, as shown by black line in the bottom plot of Fig. 3.40, which is consistent with the previous theoretical analysis.

Switching to condition 3, due to the inversed power requirement, the phase shift is controlled to be negative to introduce a negative phase shift. Averaged leakage inductor current is decreased since $I_{\text{cell1}} - I_{\text{cell2}}$ is dropped from 7 A in condition 2 to 4 A in condition 3. The last condition verifies the C2C mode without power transferred to auxiliary power. It is a constant 5 A discharging from cell 1 and charging for cell 2. It is extremely beneficial if two cells in one HFB are of significant unbalance. The current references are followed properly and promptly. Therefore, the designed controllers are proved to be robust to regulate the control variables to achieve current and power requirements from the global controller.

## 3.9 Experimental results

### 3.9.1 Experimental setup

The circuit-functional tests are performed on two DC power supplies that reacts as the battery cells/modules to simplify the validation process of requiring battery cells that are at different aging statuses. In addition, real battery cells are used to validate the long-term balancing operation. The HFB is constructed by three off-the-shelf half-bridge GaN modules EPC9201 and EPC9203 with integrated gate drivers and the self-designed planar PCB transformer in Section 3.7. The goal of the tests is to experimentally verify all the feasible operation modes described in Section 3.5 via a real-time microcontroller, TI 28377s. The testing conditions and hardware parameters are listed in Table 3.10. The continuous-time PI controller equation is approximated by Forward Euler method in order to implement the control algorithm in digital signal processors. The corresponding outputs (phase shift $d$ and duty cycle adjustment $\theta$) from the discrete-time PI controller are input to the high-res PWM module in TI 28377s to regulate the energy transfer between cells and LV system. The prototype setup is shown in Fig. 3.41.

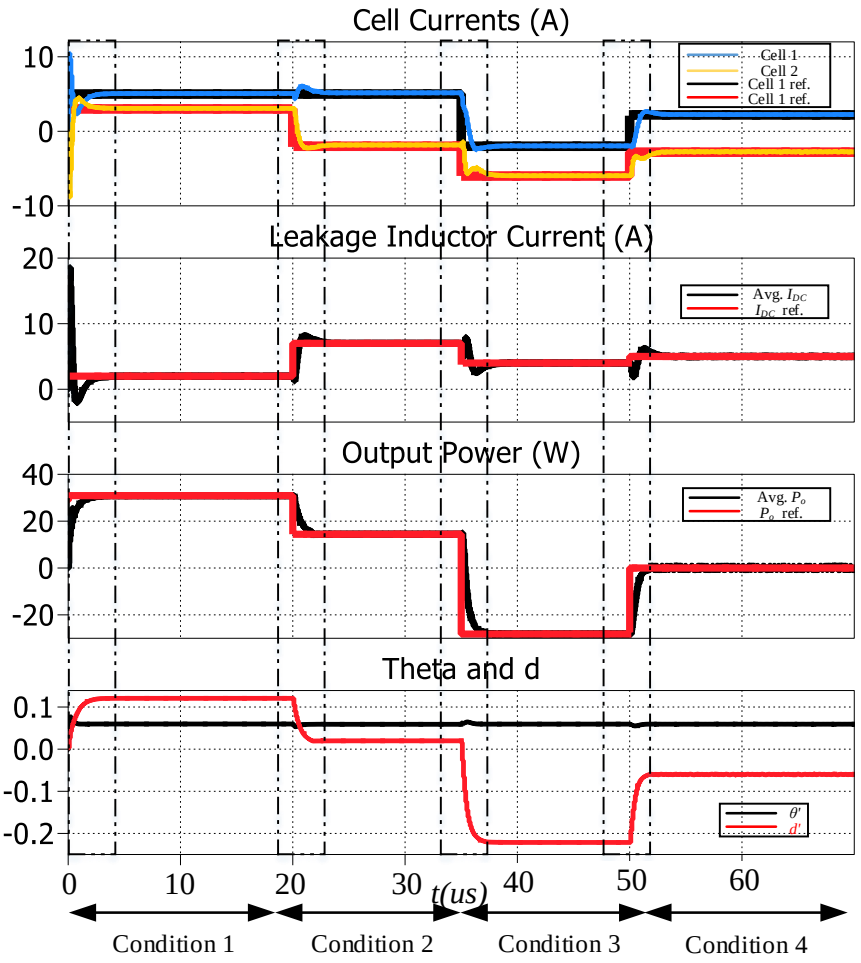



Figure 3.40: Simulated controller reactions to step reference changes

Table 3.10: Experimental parameters of the proposed HFB topology

| | |
|---|---|
| Switching frequency (kHz) | 300 - 500 |
| Sampling frequency (kHz) | 0.2 |
| Transformer turns ratio | 1:5 |
| Transformer primary leakage inductance (nH) | 6.8 |
| Output filtering capacitor (uF) | 66 |
| HV cell voltages (V) for Mode A, B, and D | $Cell_1$ = 3.5, $Cell_2$= 4 |
| HV cell voltages (V) for Mode C | $Cell_1$ = $Cell_2$= 4 |
| LV battery voltage (V) | 12 |

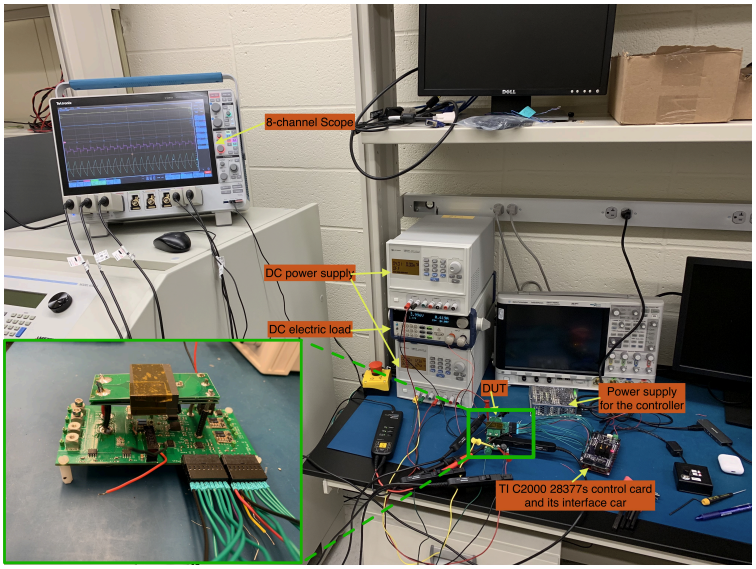



Figure 3.41: Test bench setup

### 3.9.2 Asymmetric control

As explained in previous sections, the asymmetric control logic permits two unbalanced cells (normally at different voltage levels) operating in this topology without causing the VA imbalance and further core saturation or even circuit damage due to infinitely increasing current.

Due to the unbalanced voltages on the two cells, the current will drift without duty cycle compensation as explained in Section 3.4. In order to experimentally validate the asymmetric control, the cell 1 and cell 2 voltages are selected to be 3.5 V and 4 V, respectively. The circuit operation is captured in Fig. 3.42. The conducting time for high voltage cell 1 needs to be decreased to maintain the net change of the leakage inductor current to be zero so that the current is stable. A 3.33% duty cycle reduction on cell 1 can be calculated according to the Eq. (3.18), which leads to 46.67% and 53.33% theoretical conducting duty cycles for cell 1 and cell 2, respectively. In the experimental results, 46.6% and 53.4% duty cycles are observed on the PWM signals. The theoretical and experimental results are consistent considering the switch transition from one state to another and measurement inaccuracy.

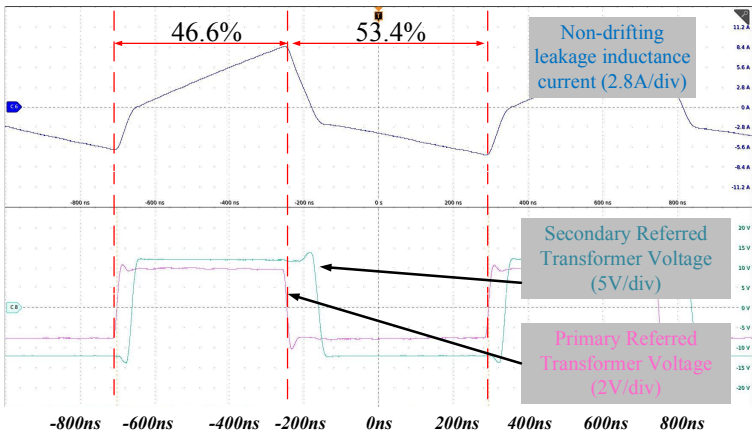



Figure 3.42: Leakage inductor current measurement: asymmetric control regulating unbalanced cells non-drifting

### 3.9.3 Balancing mode validation

The four balancing modes listed in Table 3.1 are also validated in the prototype test bench with real-time controller. The measured currents $I_{\text{cell1}}$, $I_{\text{cell2}}$ and $I_{\text{LV}}$ are given to show the power flow and C2C energy transfer. Again, the positive current convention is defined as follows: the currents discharging the cell 1 and cell 2, and the current charging the LV system.

When the neighboring cells are slightly unbalanced and LV system has to be supplied, the Mode A activates both cells to transfer energy to the LV side while demanding more current on the stronger cell, as shown in Fig. 3.43. So the unbalanced cells should be eventually converging to the same SOC level after certain amount of time depending on the balancing current level, then the Mode C will be initiated to drain the cells equally afterwards. During the validation of Mode A, cell 1 is set to be 0.5 V higher than cell 2 for demonstration of imbalance. The averaged leakage inductor current is controlled to be 1.1 A to drain 1.1 A more for cell 1 than cell 2, as it can be seen from the Fig. 3.43. Positive phase shift also enables the power transfer from HV cells to LV system.

If the two cells in one link are of significant imbalance and the LV system is at no/low-load condition, the faster balancing speed can be achieved by utilizing C2C + LV2C. The negative phase shift and DC current that is higher than $I_{\text{cell1}}$ result in charging the weak cell 1 at 0.7 A while

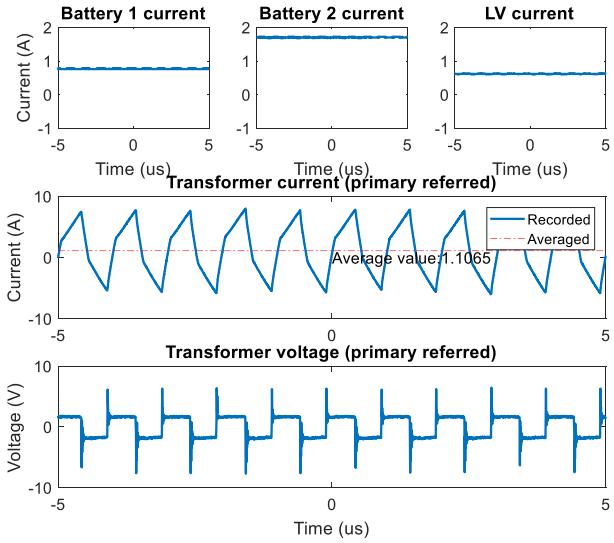



Figure 3.43: Experimental validation of Mode A C2LV + C2C with unequal cell currents

discharging the cell 2 and LV battery at 1.05 A and 0.3 A, respectively, as shown in Fig. 3.44.

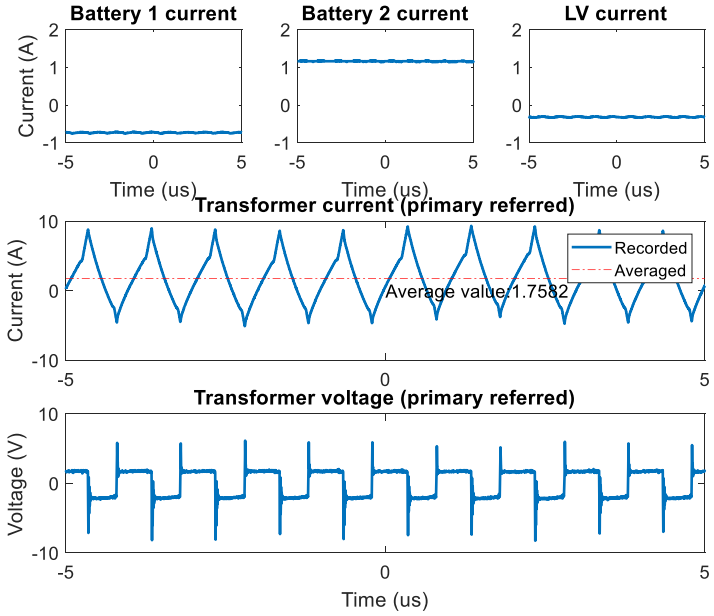



Figure 3.44: Experimental validation of Mode B LV2C + C2C

For the third operating mode as shown in Fig. 3.45, no relative current between the two cells is required, therefore $I_{DC} = 0$. That is, the two cells are supplying/charging LV loads/battery at

the same current level 1.3 A. The positive phase shift between primary switches and secondary switches is applied in order to realize the power transfer from primary to secondary. This mode is designed for the two well-balanced neighboring cells that are demanded to provide power to LV battery/loads.

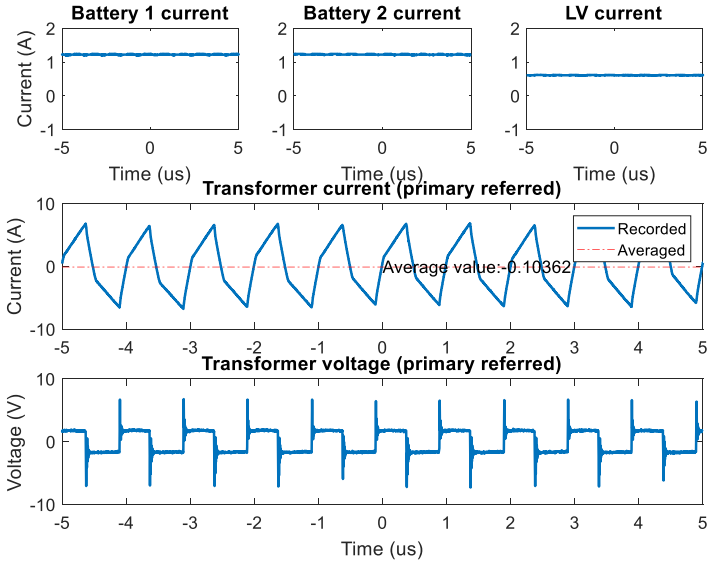



Figure 3.45: Experimental validation of Mode C C2LV only with equal cell currents

Lastly, the unique C2C energy path is verified. The phase shift control is disabled to only activate the C2C path. By controlling the $I_{DC}$ = 1.8 A, the stronger cell 2 is discharging at 1.3 A, as shown in Fig. 3.43. Meanwhile, the cell 1 is being charged at roughly 0.5 A. After all, four individual balancing modes are presented and validated in experiments. A higher-level controller can be installed to simultaneously operate multiple HFB links.

### 3.9.4 Functionality verification

Two 3000 mAh Li-ion NMC cells are installed on the HFB module as cell 1 and 2 to verify balancing operation and performance. The battery balancing is performed based on the SOC feedbacks. Voltage-based feedbacks can also be used as the inputs of the HFB balancing algorithm with possible sacrifices on the balancing performance. Given the parasitic resistance/impedance of

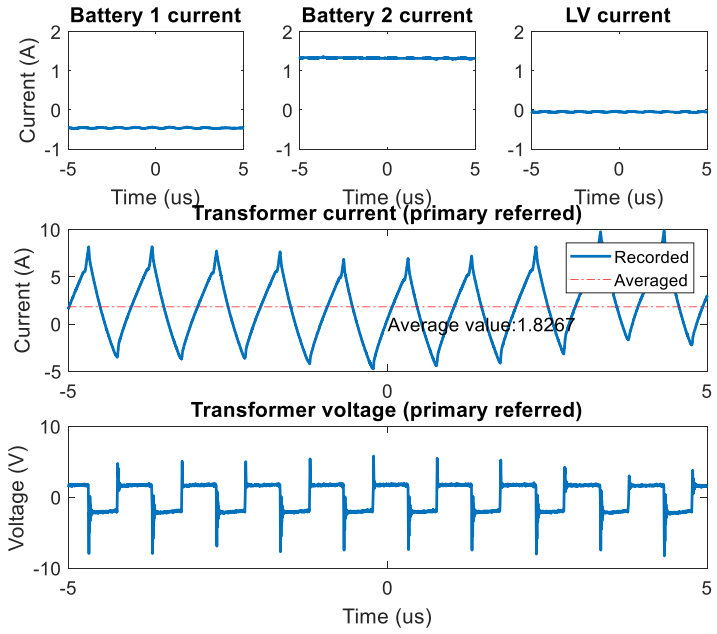



Figure 3.46: Experimental validation of Mode D C2C only

the circuit might present and voltage sensors vary in addition to cell internal resistance, the cell-to-cell voltage difference can be negligible in some cases while cells are out of balance. Therefore, balancing the cells based on the voltage difference is inaccurate in those mentioned cases.

An OCV-SOC for the cell is experimentally extracted to translate the OCV to an static SOC. The continuous SOCs are firstly obtained from fully rested cells' voltages and then updated by coulomb counting when cells are testing. The periodic OCV-SOC check is performed to prevent predicted SOCs drifting away due to current sensor inaccuracy.

### C2LV balancing

A balancing strategy that is usually found in active balancing circuit is validated first. By asking more power from the strong cell and relatively less from the weak cell, the SOC difference is gradually eliminated. The experimental measurements are shown in Fig. 3.47. A 10% initial SOC difference is introduced first and compensated by 1 A current difference between cell 1 and cell 2 within 18 minutes, while keeping output power constant 20 W.

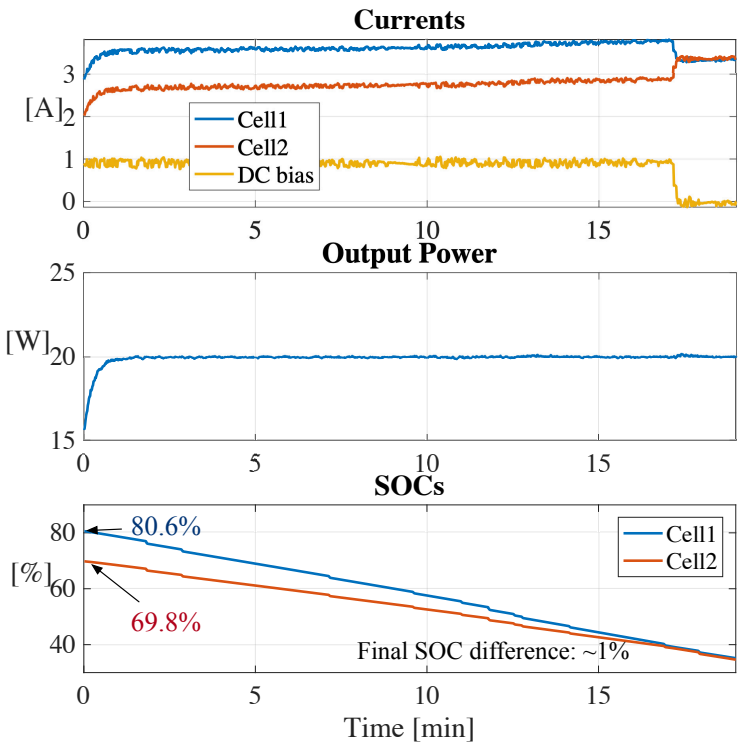



Figure 3.47: Experimental balancing functionality tests on two 3000 mAh NMC cells with 1 A C2C current with 20 W LV load

### C2LV + C2C balancing

Should the faster balancing speed be desired, the unique C2C energy path is utilized when LV load is light. In Fig. 3.48, during the C2C fast balance phase, cell 1 is providing the power to the LV as well as shuttling excessive energy to neighboring cell 2. It can be seen that 10% SOC difference is eliminated within 4 minutes, which is roughly 1/4 of what it takes for the previous case.

### LV2C + C2C balancing

During charging phase, the balancing algorithm can also be activated. Two modes are shown in Fig. 3.49. Within first 15 minutes, the circuit intentionally enlarges the SOC difference between cell 1 and 2 by introducing a positive 1 A DC bias. This period is shown to prove that the HFB module is flexible to compensate the large impedance mismatch among cells, if there is any. The

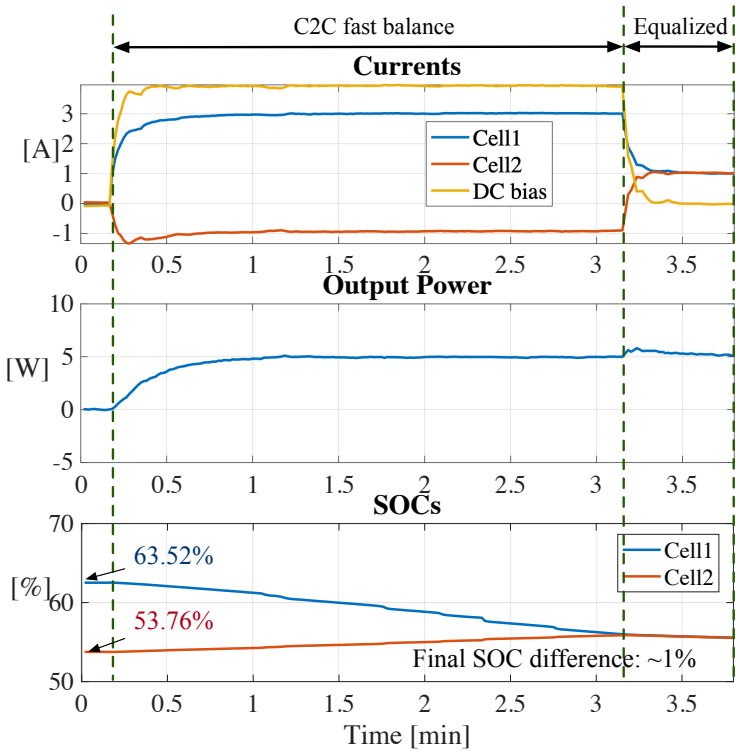



Figure 3.48: Experimental balancing functionality tests on two 3000 mAh NMC cells with 4 A C2C with 5 W load when balancing

rest of test is illustrating the balancing performance while charging.

It should be noted that the absolute balancing speed relies heavily on the balancing C-rate that is determined by the size of the battery pack. However, the two discussed cases clearly show the relative speed benefit gained by using C2C in the neighboring cells.

The measured efficiencies at nominal cell voltages (4 V) and LV voltage (12 V) is given in Fig. 3.50. The peak efficiency (85%) is higher than other non-isolated converters [76] with GaN devices at similar power level in high-frequency conditions. It also can be seen that the achieved power at 500 kHz is lower than calculated, which is due to the additional parasitic inductance in the connectors between transformer and the MOSFETs. However, this power shortage can be compensated by reducing the operating frequency, as shown in Fig. 3.50. Or less inductive connectors can be used.

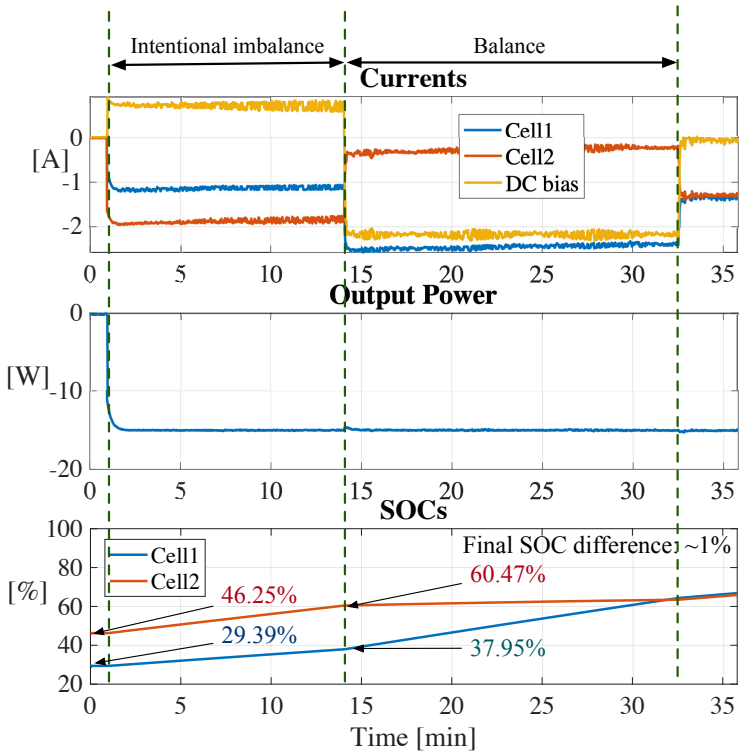



Figure 3.49: Experimental balancing functionality tests on two 3000 mAh NMC cells with intentional imbalance and balance for charging

### 3.9.5 Current ripple on battery cells

It is worth to point out the amplitude of current ripple on the battery cells, even though the battery cells are not very sensitive to high current ripple. However, to keep the operating voltage away from the max/min boundaries to which an unfiltered peak transformer current might drive due to the internal cell resistance, parallel capacitive filtering would help battery filter out high-frequency current ripples to a reasonable degree. In the experiments, two filtering capacitors with 100 uF are paralleled with each battery cell. The current going to the battery is smoother and considered to be constant compared with transformer current, as shown in Fig. 3.51.

### 3.9.6 Advantages of the proposed topology

The existing APM-based balancing strategies balance the cells in two modes, i.e. C2LV and LV2C. The additional mode C2C available in the proposed topology can be achieved indirectly

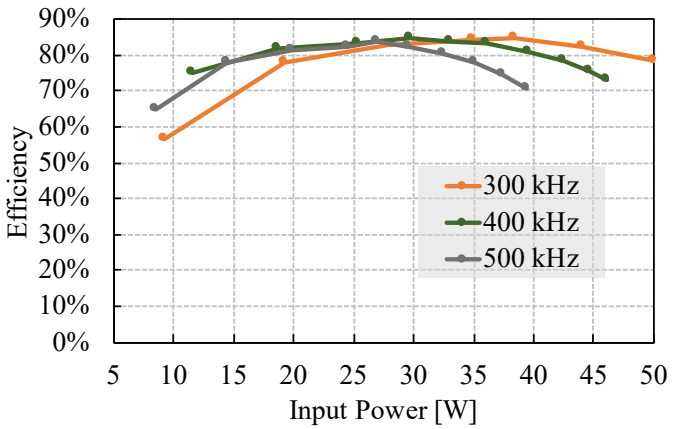



Figure 3.50: The efficiency measurements of the proposed HFB

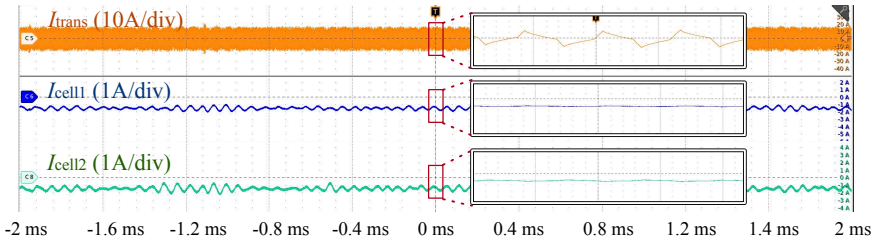



Figure 3.51: Comparison between the measured cell currents and transformer current

in the existing methodologies with paths of C2LV then LV2C. The additional power flows from cell to LV and LV to cell involve extra losses. So generally speaking, it is not efficient to apply the indirect C2C path in existing topologies. Instead, the central controller normally commands a higher current from stronger cells to compensate the total LV loads and weak cells will be left with minimal/no interfacing with LV bus. Two equivalent circuits for proposed and existing topologies are drawn in Fig. 3.52 to explain aforementioned situation. The proposed topology provides an extra freedom of balancing the whole EV pack in APM-based topologies. Especially when the LV loads are fixed and cannot overload, the additional freedom of $I_{DC}$ can be utilized to boost the balancing speed without interfering LV loads. The simulation of this case is shown in Fig. 3.53. Two UDDS driving cycles with a US06 driving cycle in between are injected to two cells composed by high-fidelity NMC battery models. The plots show that the proposed topology can provide a balancing current $I_{DC}$ while the existing topologies are clamped by the LV loads $I_{LV}$. And $I_{DC}$ can be sufficiently high to start actually charging cell 2 instead of bypassing it in the existing

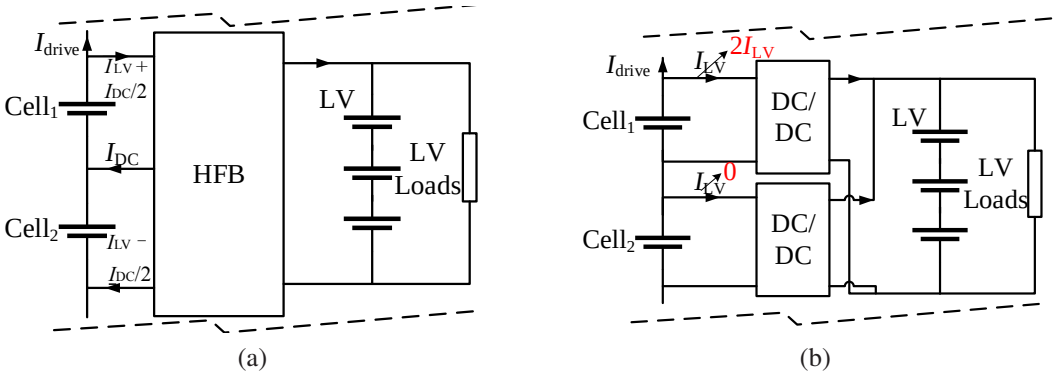



Figure 3.52: Equivalent circuits for simulation using driving cycles: (a) proposed topology, (b) existing topology

topologies without direct C2C path. Therefore, the time to balance can be significantly reduced. In this simulation, the cells are initially unbalanced with a 20% SOC difference and balanced by proposed topology and existing ones. $I_{\mathrm{DC}}$ is set to 2 A and $I_{\mathrm{LV}}$ is set to 0.5 A. In this case, the time to balance is reduced by 50%., as shown in Fig. 3.53. In general, the improved time can be quantified by the following equation for imbalance of neighboring cells:

$$t_{\mathrm{imp}} = \frac{\Delta SOC \times Cap}{I_{\mathrm{DC}} - I_{\mathrm{LV}}}, [\mathrm{min}] \tag{3.59}$$

where the initial SOC difference is denoted as $\Delta SOC$, average capacity of two neighboring cells is $Cap$ in A·min. $I_{\mathrm{DC}}$ and $I_{\mathrm{LV}}$ are the applied DC bias current and LV load referred to the input of the converter. Higher improvement should be observed when the LV bus is at light load, i.e. $I_{\mathrm{LV}}$ is small.

## 3.10 Conclusion

A HFB converter is applied in APM based balancing circuit, which allows the isolated power transfer from HV to LV as well as balancing two cell in one half bridge. The phase shift and duty cycle control are introduced to enable bi-direction power flow and controllable C2C balancing path. The circuit operation and balancing mode realizations are explained. The design guidelines for the filtering capacitor and transformer in this topology are given to convenience the future

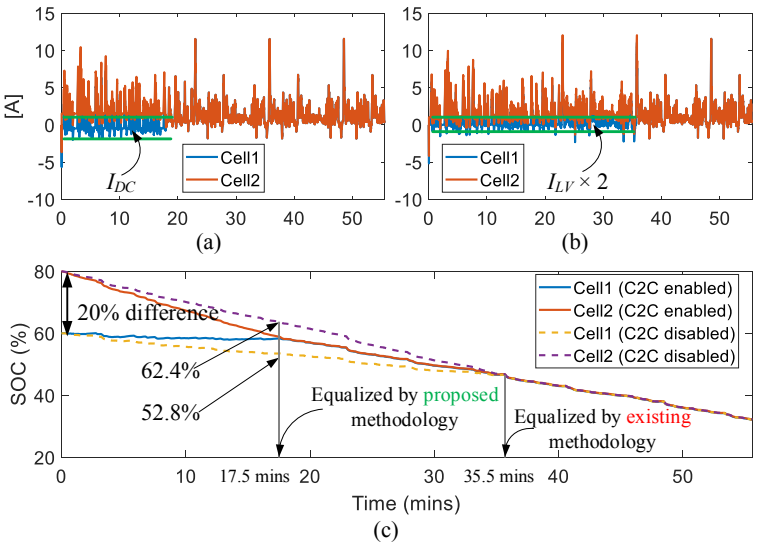



Figure 3.53: Simulation results leveraging non-C2C APM and proposed methodology with combination of UDDS and US06 driving cycles: (a) cell currents with C2C enabled, (b) cell currents without C2C, (c) comparison of balancing performance in terms of SOC

developments. The power and current controllers are properly designed based on the average and small-signal models, showing fast and robust responses. The experimental prototype is presented with self-designed converter and magnetics. The balancing performance is shown by two NMC battery cells. The unique C2C path provides significant balancing speed boost compared with the conventional cell-to-stack balancing direction at which universal isolated DC/DC converters (e.g. DAB and resonant converter) normally operate. The feasible balancing modes are validated in the prototype. A long-term simulation under the excitation of the driving cycles is presented, which compares the proposed topology with the conventional DAB topology, showing a 50% reduction of the balancing time thanks to the extra C2C balancing mode.

# Chapter 4: Coreless Dual-Active Half Bridge for BB-APM

## 4.1 Introduction

It has been demonstrated that the proposed HFB BB-APM can successfully achieve the various of balancing modes while lowering the number of power switches and magnetic components. To further reduce the cost of the system and make it more practical, this chapter proposes the significant minimization on the BB-APM topology in previous chapter by adopting DAHB [46] and integrating the discrete inductor into a coreless transformer. The number of active switch per cell can be reduced to 2 compared with 3 from HFB configuration and 8 from DAB [77]. The ferromagnetic core material that is the major source of cost is also eliminated.

The ferromagnetic materials like steel and ferrite suffers from hysteresis loss and eddy current losses. As the technology of the power MOSFETs evolves, the increasingly higher switching frequency can be achieved. The core loss will dominate the system loss, and thus, the coreless transformer is desired [78]. Also, it is easy faces the saturation problems after certain level of magnetization. In order to avoid the losses and saturation problems, advanced materials need to be used like ferrite. The advantage of the air core is that the transformer will never be saturated as the cored one. Therefore, the saturation check is not required anymore, which simplifies the search of core materials. The coreless transformers also enable light-weighted designs and possibility of PCB integration.

### 4.1.1 EMI due to the absence of the magnetic material

As the flux-regulating core is removed, the flux generated from the windings is randomly distributed in the near field of the transformer. Two simple Maxwell simulations with core and without core are performed to show how the magnetic material regulates the magnetic filed, as shown in

Fig. 4.1 and Fig. 4.2. The core is given 1000 $\mu_r$ to represent any ferrite or other high-permeability material, where again $\mu_r$ is the relative permeability respective to vacuum. On the contrary, the shape of the core is outlined in the coreless simulation (Fig. 4.2) but the material is actually air/vacuum. The flux lines around the windings are plotted to highlight the difference of absence of the magnetic core. The flux is well regulated with the presence of the magnetic core, i.e. minimal flux leakage. Without the core, the flux starts to disperse and distribute in the near field of the windings.

The phenomena explained above might contribute to low coupling and some unwanted electromagnetic interference (EMI) problem which can interfere with the sensing/communication signals that are placed close to the transformer. The integrity of the signals will be compromised if not closely investigated. However, it has been discussed and concluded that the EMI problem generated due to the coreless transformer can be neglected at the frequency where common power electronics operate (kHz to MHz) [79]. Even though the literature suggests that, the results some time vary case by case. Without proper analysis, a solid conclusion cannot be simply drawn. In this study, the extra care is taken to guarantee that the unregulated flux has minimal impact on other power electronics. The simulations shown in the Appendix also proves that the PCB design has controlled the undesired interference to be negligible.

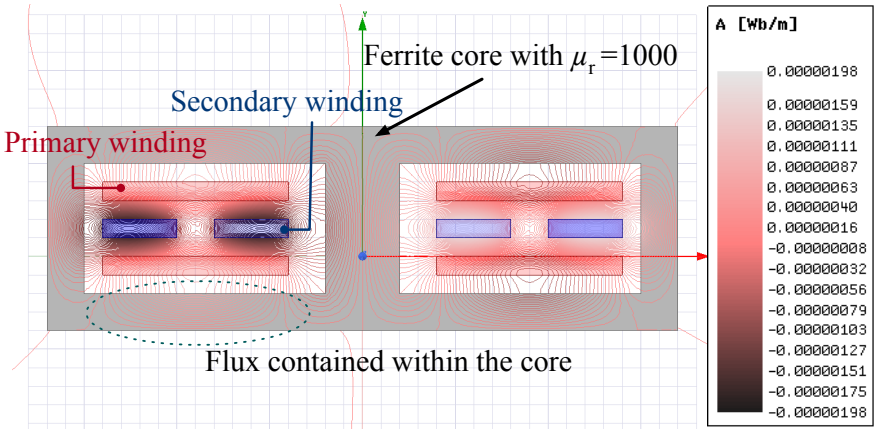



Figure 4.1: Distribution of flux lines for a transformer with core

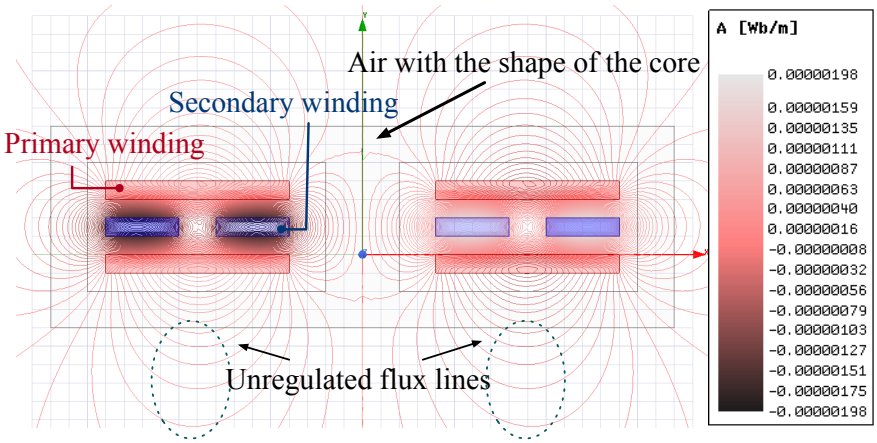



Figure 4.2: Distribution of flux lines for a transformer without core

### 4.1.2 Available topologies for coreless transformer

Due to the unregulated flux behavior, the coreless transformer has significantly worse coupling between windings and therefore generates higher conduction loss. There has been significant amount of the attention being brought on integrating redundant/discrete inductors or getting rid of the magnetic core to minimize the loss generated by the loose coupling, especially in wireless charging, server and consumer electronics [76], [80]–[84]. For the wireless charging application, the resonant converter [82], [83] is widely used since the coupling of coreless transformer is significantly compensated by the resonant capacitor. Even though the LLC-equivalent configurations can be adopted on the HFB topology with the topological modifications, as shown in Fig. 4.3, the C2C balancing between neighboring cells is eliminated as the DC current is intrinsically blocked by the resonant capacitors $C_{r1}$. Therefore, the cells in the same converter might suffer from imbalance as their currents cannot be controlled independently. Some feasible alternatives could be

- configuring the primary topology to be full bridge instead of half bridge: each cell is monitored and regulated by a dedicated converter
- adding extra switches to form a multi-level converter

Therefore, the traditional resonant converter is not suitable for the proposed topology unless the converter is configured as mentioned above. However, these options contradict with the idea of

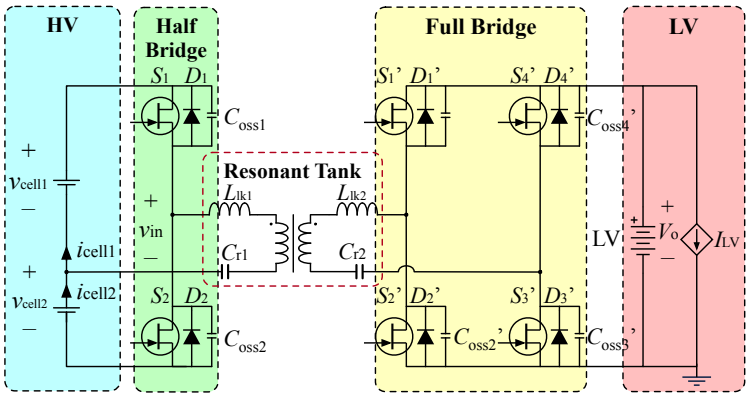



Figure 4.3: The potentially feasible CLLLC converter, modified based on proposed HFB converter

lowering the cost of the redistributive balancing since they add extra components that contribute to the total cost at least by 10% according to the cost analysis conducted in Chapter 6. In that case, the advantage from the proposed topology in terms of the component count/cost is compromised though the magnetic component is minimized. Instead, a different approach is needed to maintain the proposed balancing modes while minimize the magnetic design.

### 4.1.3 DAHB with coreless transformer

The HFB topology can be simplified to a DAHB topology that achieves the identical functionalities but with less power switches, as illustrated in Fig. 4.4. Compared with the HFB, the DAHB removes one of the half bridge from original full-bridge configuration on the secondary side. This modification requires two stabilizing/filtering capacitors to be placed in parallel with the half-bridge MOSFETs. In order to take cared of unbalanced device stresses, the bleeding resistors are paralleled with the output capacitors to balance their voltages.

The transformer is always assumed tightly coupled when deriving the circuit model [46], [85], i.e. magnetization inductance is significantly larger than the external or leakage inductance. This assumption noticeably simplifies the design and modeling of the topology. However, the effect of the magnetization inductance cannot be neglected in coreless transformer, leading to a more complex modeling process. In this chapter, the generalized system model is derived for both cored and coreless systems considering the coupling factor and effective turns ratio. Based on the system

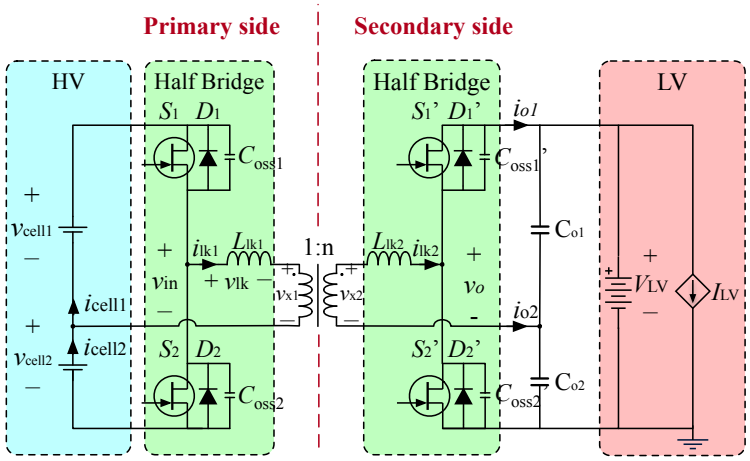



Figure 4.4: DAHB topology with coreless transformer

model, the coreless transformer is correspondingly designed.

## 4.2 System model

The conventional DAB and DAHB designs utilize either discrete inductor or the leakage inductor introduced by the transformers [46], [56], [77], [86]. Integrating the discrete inductor in the transformer, the current flowing through the magnetization inductor can be ignored since it is significantly larger than leakage inductance. Therefore, the system model is normally derived assuming that the magnetization inductor is open-circuited [56], [87], which makes the derivations relatively uncomplicated. However, for coreless transformers, the absence of the core leads to a higher leakage inductance even when primary and secondary windings are placed sufficiently close to each other [79], [88], which makes the leakage inductance comparable with the magnetization inductance. So the current flowing through the magnetization inductance is not negligible in this case. The expressions of currents and power thus deviate from all the existing literatures on DAB or DAHB designs, including the ones in Chapter 3. The simplified ECM of the transformer is illustrated in Fig. 4.5 considering magnetization inductor in the transformer. The switching node voltages are simplified to square wave voltage sources $v_{\text{in}}$ and $v_{\text{o}}$ assuming the voltage is constant during one switching action, where the prime represents the primary-referred secondary values,

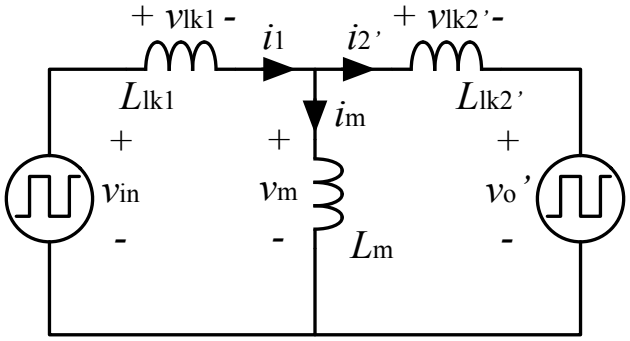



Figure 4.5: The equivalent circuit model of the transformer with the square-wave input voltage sources

such as the leakage inductance $L'_{\text{lk2}}$ and voltage $v'_{\text{o}}$. Applying KCL and KVL on the ECM leads to:

$$i_1 = i_{\text{m}} + i'_2 \tag{4.1}$$

$$V_{\text{in}} - V_{\text{m}}(t) = L_{\text{lk1}} \frac{di_1(t)}{dt} \tag{4.2}$$

$$V_{\text{m}}(t) - V'_{\text{o}} = L'_{\text{lk2}} \frac{di'_2(t)}{dt} \tag{4.3}$$

$$V_{\text{m}}(t) = L_{\text{m}} \frac{di_{\text{m}}(t)}{dt} \tag{4.4}$$

where the currents $i_1(t)$, $i'_2(t)$, and $i_{\text{m}}$ are the primary-side leakage inductor current, primary-referred secondary-side leakage inductor current and magnetization current. Voltage across the magnetization inductor is denoted as $V_{\text{m}}(t)$. The equations above can be simplified to:

$$\begin{aligned} V_{\text{m}}(t) &= L_{\text{m}} \left( \frac{di_1(t)}{dt} - \frac{di'_2(t)}{dt} \right) \\ &= L_{\text{m}} \left[ \frac{v_{\text{in}}(t) - V_{\text{m}}(t)}{L_{\text{lk1}}} - \frac{V_{\text{m}}(t) - v'_{\text{o}}(t)}{L'_{\text{lk2}}} \right] \\ &= \frac{L_{\text{lk1}} v'_{\text{o}}(t) + L'_{\text{lk2}} v_{\text{in}}(t)}{\frac{L_{\text{lk1}} L'_{\text{lk2}}}{L_{\text{m}}} + L_{\text{lk1}} + L'_{\text{lk2}}}. \end{aligned} \tag{4.5}$$

It can be seen that the magnetization voltage replies on the leakage inductances and the ratio of $L_{\text{lk1}}$ and $L_{\text{m}}$, which is in turn, dependent on the coupling of the transformer. The main difference of the cored transformers and coreless transformers is the coupling between windings. A tightly coupled

transformer using magnetic material has most of its flux coupled between windings, leading to a significantly small leakage inductance compared to magnetization inductance. On the other hand, the flux that traverses through the same winding is comparable with the one linking with the other winding if the windings are not placed sufficiently closed or the magnetic material is removed. In order to quantify the extent of coupling, the coupling coefficient is commonly used and defined as

$$k = \frac{L_{\mathrm{m}}}{L_{\mathrm{self}}} = \frac{L_{\mathrm{m}}}{L_{\mathrm{m}} + L_{\mathrm{lk}}} \tag{4.6}$$

where $L_{\mathrm{self}}$ is the self inductance, a sum of magnetization inductance $L_{\mathrm{m}}$ and leakage inductance $L_{\mathrm{lk}}$ referred to any side. The higher the coupling achieves, the smaller magnetizing currents can be induced, resulting in less losses. Given the different transformer parameters, the switch node voltage varies based on Eq. (4.6), which further determines the leakage current that governs the circuit operation. Therefore, the voltages across leakage inductors will be analyzed firstly based on the transformer configurations.

### 4.2.1 Expressions of tightly coupled transformers

In the design of the cored transformer, the coupling factor is as high as 0.99 [89], which translates to the ratio of leakage and magnetization inductance is at least a factor of 100. Therefore, the term $\frac{L_{\mathrm{lk1}} L_{\mathrm{lk2}}}{L_{\mathrm{m}}}$ in Eq. (4.5) can be neglected without noticeable errors. The voltage across the magnetization inductor then can be simplified with the knowledge of $L_{\mathrm{lk1}} = L'_{\mathrm{lk2}}$ in transformers:

$$V_{\mathrm{m}} = \frac{V_{\mathrm{in}} + V'_{\mathrm{o}}}{2}, \tag{4.7}$$

which further determines the voltage across the primary leakage inductor

$$v_{\mathrm{lk1}} = V_{\mathrm{in}} - V_{\mathrm{m}} = \frac{V_{\mathrm{in}} - V'_{\mathrm{o}}}{2}. \tag{4.8}$$

This equation shows that the voltage across the primary leakage inductor is not $V_{\text{in}} - V'_{\text{o}}$ which applies in the designs with discrete transformers and inductors, whereas the half of the difference is applied on the leakage inductor due to the symmetrical leakage inductance on both windings. As a result, the rate of current change is halved, which further leads to halved output power capability if switching frequency is maintained the same.

### 4.2.2 Expressions of loosely coupled transformers

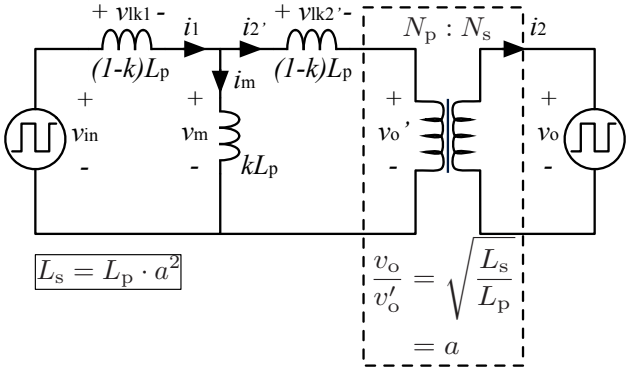



Figure 4.6: The equivalent transformer model considering the coupling factor and nonideality

On the other hand, the term $\frac{L_{\text{lk1}}L'_{\text{lk2}}}{L_{\text{m}}}$ in Eq. (4.5) cannot be ignored anymore when the core is removed as the flux regulation is significantly worse and it leads to leakage inductance that is comparable and even larger compared with magnetization inductance [90]. Consequently, $V_{\text{m}}$ will be related to the coupling factor. To better illustrate the change, the equivalent transformer model considering coupling factor $k$ is given in Fig. 4.6. It shows a transformer with a physical turns ratio of $N_{\text{p}} : N_{\text{s}} = 1 : n$ and coupling factor $k \subset [0, 1]$. However, the relationship mapping the secondary value to primary side is not necessarily equal to physical turns ratio [91]. For a coreless transformer, It is equivalent to have an ideal transformer with a turns ratio of

$$N_{\text{p}} : N_{\text{s}} = 1 : \sqrt{L_{\text{s}}/L_{\text{p}}} = 1 : \sqrt{L_{\text{lk2}}/L_{\text{lk1}}} = 1 : a. \tag{4.9}$$

The primary self inductance and secondary self inductance are denoted as $L_{\text{p}}$ and $L_{\text{s}}$, respectively. All primary-referred secondary parameters with the effective turns ratio are summarized in Table

4.1. These notations will be used in this section unless explicitly stated. For a cored transformer, effective turns ratio is equal to the physical turns ratio.

Table 4.1: The translation from secondary parameters to primary-referred secondary parameters

| **Secondary** | **Primary-referred** |
|---|---|
| ***x*** | ***x'*** |
| $V_s$ | $V_s/a$ |
| $I_s$ | $aI_s$ |
| $L_{lk2}$ | $L_{lk2}/a^2 = L_{lk1}$ |

The magnetization inductance is represented by $L_m = kL_p$. Due to the imperfect coupling, the flux not linked with the other winding forms the leakage inductance that is related to $k$, as shown in Eq. (4.6). The leakage inductances $L_{lk1}$ and $L_{lk2}$ can be expressed as $(1-k)L_p$ and $(1-k)L_s$, respectively. Referred to the primary, the leakage inductance $L'_{lk2}$ equals to $L_{lk1}$. The term $\frac{L_{lk1}L'_{lk2}}{L_m}$ can be therefore simplified to $\frac{1-k}{k}L_{lk1}$ and the Eqs. (4.1) - (4.4) can be represented by the following:

$$V_m = \frac{V'_o + V_{in}}{\frac{1-k}{k}+2} \overset{K=\frac{1-k}{k}}{=} \frac{V'_o + V_{in}}{K+2} \tag{4.10}$$

$$v_{lk1} = \frac{(K+1)V_{in} - V'_o}{K+2} = \frac{V_{in} - \frac{V'_o}{K+1}}{1+\frac{1}{K+1}} \tag{4.11}$$

$$v'_{lk2} = V_m - V'_o = \frac{V_{in} - (K+1)V'_o}{K+2} = \frac{\frac{V_{in}}{K+1} - V'_o}{1+\frac{1}{K+1}} \tag{4.12}$$

The Eqs. (4.10) - (4.12) are the important equations that determine the current waveforms of the magnetization inductor, primary-side and primary-referred secondary-side leakage inductors. Fig. 4.7 shows the key waveforms of the inductor currents when $V_{in} - \frac{V'_o}{K+1} > 0$. In order to derive the piece-wise expressions, the switching sequence during one period is summarized in Table 4.2, where phase shift and duty cycle compensation are applied, which is explained in the previous chapter. The following shows the voltage expressions for each segment during one period, which is essential for deriving the expressions of RMS and ripple current for each inductor element as

Table 4.2: Switching sequence with phase shift and duty cycle adjustment during a switching period $T$

| **Time slot** | Switch | | | | $v_{\text{in}}(t)$ | $v_{\text{o}}(t)$ |
|---|---|---|---|---|---|---|
| | $S_1$ | $S_2$ | $S_1'$ | $S_2'$ | | |
| $0-d$ | On | Off | Off | On | $v_{\text{cell1}}$ | $v_{\text{co2}}$ |
| $d-0.5T-\theta$ | On | Off | On | Off | $v_{\text{cell1}}$ | $v_{\text{co1}}$ |
| $0.5T-\theta-d+0.5T$ | Off | On | On | Off | $v_{\text{cell2}}$ | $v_{\text{co1}}$ |
| $d+0.5T-T$ | Off | On | Off | On | $v_{\text{cell2}}$ | $v_{\text{co2}}$ |

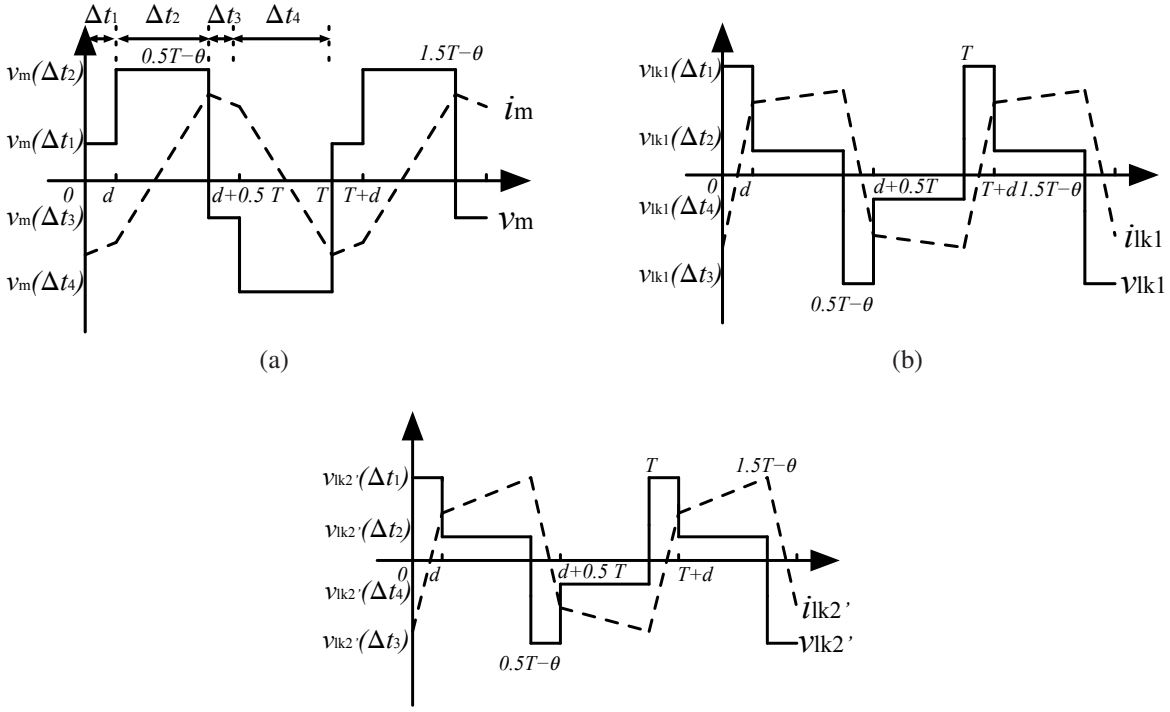



Figure 4.7: The waveforms of (a) magnetizing inductor, (b) primary leakage inductor, (c) primary-referred secondary leakage inductor

well as the output power:

$$v_{\text{m}}(t)=\begin{cases}\dfrac{-V_{\text{o}}'+V_1}{K+2}, & 0\le t<d\\ \dfrac{V_{\text{o}}'+V_1}{K+2}, & d\le t<\dfrac{T}{2}-\theta\\ \dfrac{V_{\text{o}}'-V_2}{K+2}, & \dfrac{T}{2}-\theta\le t<\dfrac{T}{2}+\theta\\ \dfrac{-V_{\text{o}}'-V_2}{K+2}, & \dfrac{T}{2}+\theta\le t<T\end{cases} \tag{4.13}$$

$$v_{\mathrm{lk1}}(t) = \begin{cases} \dfrac{V_1 + \frac{V'_{\mathrm{o}}}{K+1}}{1 + \frac{1}{K+1}}, & 0 \le t < d \\ \dfrac{V_1 - \frac{V'_{\mathrm{o}}}{K+1}}{1 + \frac{1}{K+1}}, & d \le t < \dfrac{T}{2} - \theta \\ \dfrac{-V_2 - \frac{V'_{\mathrm{o}}}{K+1}}{1 + \frac{1}{K+1}}, & \dfrac{T}{2} - \theta \le t < \dfrac{T}{2} + \theta \\ \dfrac{-V_2 + \frac{V'_{\mathrm{o}}}{K+1}}{1 + \frac{1}{K+1}}, & \dfrac{T}{2} + \theta \le t < T \end{cases} \tag{4.14}$$

$$v'_{\mathrm{lk2}}(t) = \begin{cases} \dfrac{\frac{V_1}{K+1} + V'_{\mathrm{o}}}{1 + \frac{1}{K+1}}, & 0 \le t < d \\ \dfrac{\frac{V_1}{K+1} - V'_{\mathrm{o}}}{1 + \frac{1}{K+1}}, & d \le t < \dfrac{T}{2} - \theta \\ \dfrac{\frac{-V_2}{K+1} - V'_{\mathrm{o}}}{1 + \frac{1}{K+1}}, & \dfrac{T}{2} - \theta \le t < \dfrac{T}{2} + \theta \\ \dfrac{\frac{-V_2}{K+1} + V'_{\mathrm{o}}}{1 + \frac{1}{K+1}}, & \dfrac{T}{2} + \theta \le t < T \end{cases} \tag{4.15}$$

### 4.2.3 Turns ratio

When the turns ratio of the transformer is designed to be $\dfrac{V_x}{K+1} > V'_{\mathrm{o}}\,(x \in (1,2))$, $V_{\mathrm{m}}$, $v_{\mathrm{lk1}}$ and $v_{\mathrm{lk2}}$ are positive during $[d, T/2-\theta)$ and negative during $[T/2+\theta, T)$, which leads to increasing and decreasing of the inductor current during those two time windows,as shown in Fig. 4.7. The turns ratio enabling requires

$$\begin{aligned} a &> \frac{V_{\mathrm{LV}}}{V_x} \cdot \frac{K+1}{2} \\ &= \frac{V_{\mathrm{LV}}}{V_x} \cdot \frac{1}{2k},\ x \in\ (1,2) \end{aligned} \tag{4.16}$$

Considering the cell voltage range and coupling factor are always positive, above equation can

be simplified to

$$\begin{aligned} a &> \max\left(\frac{V_{\mathrm{LV}}}{V_x}\right) \cdot \max\left(\frac{1}{2k}\right) \\ &> \frac{\max(V_{\mathrm{LV}})}{\min(V_x)} \cdot \frac{1}{2 \cdot k} \\ &> \frac{14}{2.8} \times \frac{1}{2 \cdot k} \\ &> \frac{2.5}{k} \end{aligned} \tag{4.17}$$

Therefore, the waveform will change if designed effective turns ratio fails to meet the equations below:

$$a > \begin{cases} 4, \ k \leq 0.625 \\ 3, \ 0.625 < k \leq 0.83 \\ 2.5, \ k > 0.83 \end{cases} \tag{4.18}$$

If the Eq. 4.18 is not met, then the currents of $i_{\mathrm{lk1}}$ and $i_{\mathrm{lk2}}$ start to decrease $[d, T/2 - \theta)$ and increase during $[T/2 + \theta, T)$. This difference will not affect the operation of the circuit, or the peak-to-peak (P2P) current range where ZVS operation should comply with. The ZVS operation will be introduced and discussed in next chapter. The corresponding waveforms derived from the aforementioned voltage expressions are drawn in Fig. 4.7 with the condition where Eq. (4.18) is satisfied. Fig 4.8 shows the primary leakage inductor current waveform when the Eq. 4.18 is not satisfied compared with the one in Fig. 4.7b.

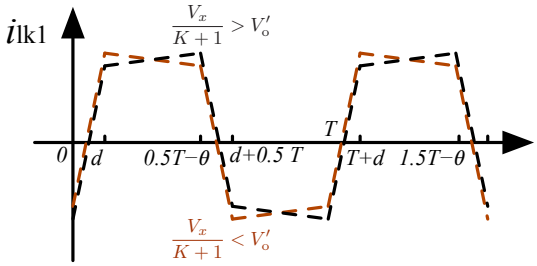



Figure 4.8: The waveforms of the primary leakage inductor current when Eq. (4.18) is satisfied and unsatisfied

Then the turns ratio $n$ is selected to be 4 to fit the worst coupling factor. To reduce the turns

ratio to 3, the coupling factor $k$ needs to be better than 0.83. However, due to the imperfect coupling, the effective turns ratio would be less than 3 if turns ratio is 3. So in order to eliminate any uncertainties and simplify the design process. The physical transformer turns ratio is chosen to be 4, which definitely satisfy the inequality in Eq. (4.18) without introducing significant loss. However, the turns ratio can be reduced if coupling can be improved.

## 4.3 Modeling of the transformer currents

The current of each inductor component then is piece-wisely obtained by $\Delta i = \frac{V}{L}\Delta t$ assuming the voltage remains constant during one switching event. The current and voltage waveforms of magnetizing, primary leakage, and primary-referred leakage inductors are shown in Fig. 4.7. The peak and RMS values for the aforementioned currents need to be quantified in order to select the proper MOSFETs and design the transformer to tolerate the current without introducing too much losses.

### 4.3.1 Peak-to-peak currents

The peak-to-peak values can be obtained by evaluating the current during the conduction of upper switch or lower switch, i.e. $[0, \frac{T}{2} - \theta]$ or $[\frac{T}{2} - \theta, T]$. According to the equations listed in Eqs. (4.13) - (4.15), the peak-to-peak currents are calculated and Eq. (4.6) is used to simplify the equations. The expressions of the P2P current for magnetization $I_{\mathrm{m,pp}}$, primary leakage $I_{\mathrm{lk1,pp}}$ and primary-referred secondary leakage $I_{\mathrm{lk2,pp}}$ are shown in Eqs. (4.19) - (4.21).

$$\begin{aligned} I_{\mathrm{m,pp}} &= \left| i_{\mathrm{m}}\left(\frac{T}{2} - \theta\right) - i_{\mathrm{m}}(0) \right| = \left| i_{\mathrm{m}}(T) - i_{\mathrm{m}}\left(\frac{T}{2} - \theta\right) \right| \\ &= \frac{k}{f L_{\mathrm{m}}(k+1)} \left[ V_2 - V_{\mathrm{o}}' d' - \frac{V_2(V_2 - V_{\mathrm{o}}')}{V_1 + V_2} \right] \\ &= \frac{1}{f L_{\mathrm{p}}(k+1)} \left[ V_2 - V_{\mathrm{o}}' d' - \frac{V_2(V_2 - V_{\mathrm{o}}')}{V_1 + V_2} \right] \end{aligned} \tag{4.19}$$

$$
\begin{aligned}
I_{\mathrm{lk1,pp}} &= \left| i_{\mathrm{lk1}}\left(\frac{T}{2}-\theta\right) - i_{\mathrm{lk1}}(0) \right| = \left| i_{\mathrm{lk1}}(T) - i_{\mathrm{m}}\left(\frac{T}{2}-\theta\right) \right| \\
&= \frac{1}{f L_{\mathrm{lk1}}(k+1)} \left[ V_2 + V_{\mathrm{o}}' d' k - \frac{V_2(V_2 + V_{\mathrm{o}}' k)}{V_1 + V_2} \right] \\
&= \frac{1}{f L_{\mathrm{p}}(1-k^2)} \left[ V_2 + V_{\mathrm{o}}' d' k - \frac{V_2(V_2 + V_{\mathrm{o}}' k)}{V_1 + V_2} \right]
\end{aligned}
\tag{4.20}
$$

$$
\begin{aligned}
I_{\mathrm{lk2,pp}}' &= \left| i_{\mathrm{lk2}}'\left(\frac{T}{2}-\theta\right) - i_{\mathrm{lk2}}'(0) \right| = \left| i_{\mathrm{lk2}}'(T) - i_{\mathrm{lk2}}'\left(\frac{T}{2}-\theta\right) \right| \\
&= \frac{1}{f L_{\mathrm{lk2}}'(k+1)} \left[ V_2 k + V_{\mathrm{o}}' d' - \frac{V_2(V_2 k + V_{\mathrm{o}}')}{V_1 + V_2} \right] \\
&= \frac{1}{f L_{\mathrm{s}}'(1-k^2)} \left[ V_2 k + V_{\mathrm{o}}' d' - \frac{V_2(V_2 k + V_{\mathrm{o}}')}{V_1 + V_2} \right]
\end{aligned}
\tag{4.21}
$$

The equations show highly non-linearly coupled parameters that determine the ripple amplitudes, e.g. switching frequency, voltages of the input and output, and coupling factor of the transformer. But effects of some of them can be isolated from each other.

### 4.3.2 Parameters influencing the ripple currents

**phase shift** $d'$

The effect of the phase shift linearly contributes to higher ripple if it is increasing for both leakage inductor currents, assuming other parameters are constant. However, the phase shift puts negative effects on magnetizing current ripple, i.e. higher phase shift, less ripple. The worst case then happens when phase shift reaches the maximum for leakage inductor currents and the minimum for magnetizing inductor current.

**Cell voltage** $V_1$

Higher cell 1 voltage contributes to less ripple for all inductor current.

**Cell voltage $V_2$ and output voltage $V_o'$**

These two terms are non-linearly dependent. It is not straightforward to locate the worst case scenario for both of them. As the analyzed effects of $d'$ and $V_1$ show clear trends, the parameter sweep can be applied to $V_2$ and $V_o'$ and find the worst case. Note that the magnetizing inductance is also proportional to coupling factor and the ripple decreases with higher coupling. The effect of each parameter is summarized in Table 4.3.

Table 4.3: The parameters affecting the ripple currents

| **Parameter** | Direction of change | Current ripple |
|---|---|---|
| Phase shift $d$ | $\uparrow$ | $I_{lk1,pp}$ and $I_{lk2,pp}$ $\downarrow$ |
| Cell voltage $V_{cell1}$ | $\uparrow$ | $I_{lk1,pp}$ and $I_{lk2,pp}$ $\downarrow$ |
| Cell voltage $V_{cell2}$ and $V_o$ | Nonlinear | Nonlinear |
| Coupling coefficient | $\uparrow$ | $I_{m,pp}$ $\downarrow$ |

### 4.3.3 Worst peak-to-peak currents

In order to represent the trend without sacrificing the generality of this study for different couplings and switching frequencies, the ripple current is represented by a per unit system through fixing the switching frequency $f$ and the inductances to be 1. When the transformer is designed and switching frequency is decided, the ripple current can be obtained by multiplying the factor $1/Lf$. Unfortunately, the coupling factor $k$ cannot be decoupled from the equations, so it is leaved as a variable in the parameter sweep.

**Magnetizing inductor current ripple**

The sweep is shown in Fig. 4.9 for the coreless and cored systems with the same primary self-inductance $L_p$. The figures show insignificant difference between coreless and cored transformers. That's because the magnetization inductance has small difference when the total inductance is fixed. The trend is that when both cell 2 voltage and LV voltage reach the maximum the ripple current is maximum. However, more attentions should be paid to the leakage inductance that de-

termines the output power at given switching frequency and phase shift. Another ripple current comparison of the magnetizing inductor for coreless and cored transformers is given in Fig. 4.10 for same primary leakage inductance $L_{lk1}$. When the leakage inductance is constant, the magnetizing inductance is sufficiently different which makes the ripple current increases by a factor of 1000 in air-cored version compared with cored transformer. Note that in the simulation the coupling factors used for coreless and cored transformers are 0.75 and 0.999, respectively. The magnetization inductor current ripple is expected to reduce when the coupling is improved.

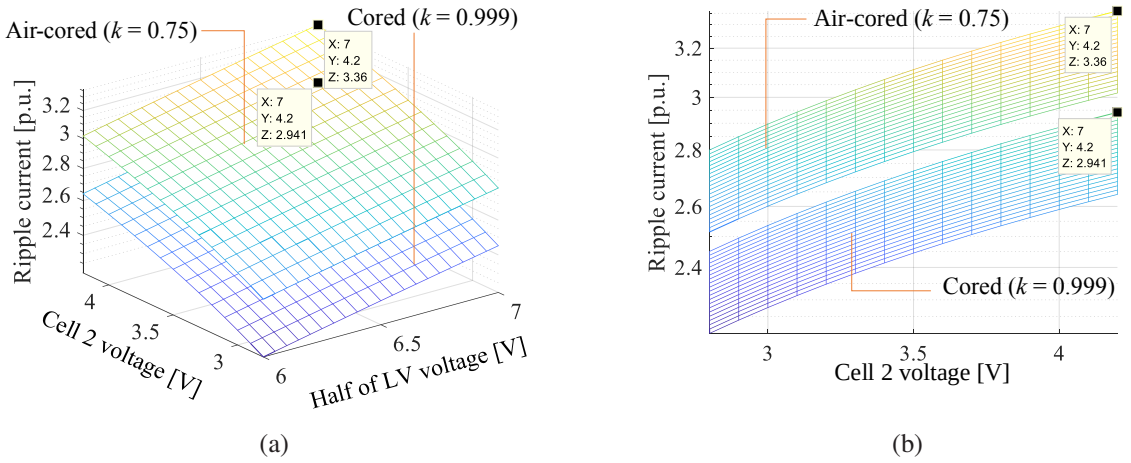



Figure 4.9: Per-unit magnetizing inductor ripple current with the same total inductance: (a) 3D view (b) side view

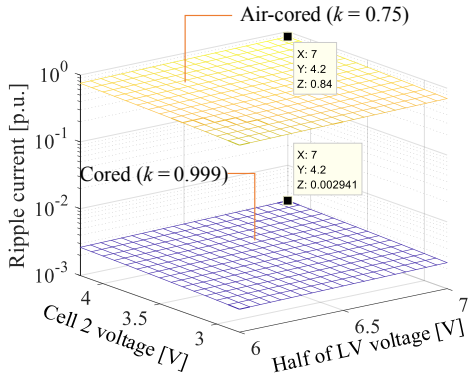
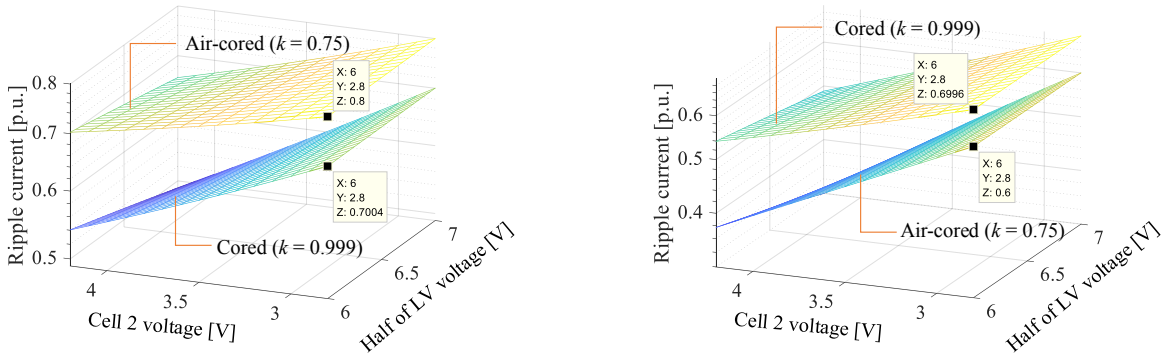



Figure 4.10: Per-unit magnetizing inductor ripple current with the same leakage inductance in log scale

### Primary and primary-referred leakage inductor ripple currents

The same sweep is performed on the primary and primary-referred secondary leakage inductor ripple currents, as shown in Fig. 4.11. It can be seen from the figures that in primary leakage inductor ripple currents, as the coupling is more tight, the ripple current decreases while the ripple current increases for secondary one. In the worst scenario, the primary ripple drops from 0.8 p.u. to 0.7 p.u. and secondary one rises from 0.6 p.u. to 0.7 p.u. in Fig. 4.11a and 4.11b. The reason why the secondary ripple is smaller compared with cored transformer is that some energy is circulating in the magnetization inductor, leading to decreased output power which will be explained in the following section.




(a) (b)

Figure 4.11: Per-unit (a) primary leakage secondary inductor ripple current with the same leakage inductance, (b) primary-referred leakage inductor ripple current with the same leakage inductance

In order to find the correlation between coupling, effective turns ratio and amplitude of ripple current and locate the worst case, optimization tools subject to given constraints applied on the operation conditions are used. The LS built in *fmincon* toolbox in MATLAB is used and the cost function is stated in Eq. (4.22). The condition where the circuit needs to operate is the same as the HFB configuration. That is, providing at least 30 W when SOC is greater than 20%, which

translates to 3.32 V on the cell voltage.

$$\min_{I_{\mathrm{lk}x,\mathrm{pp}}} I_{\mathrm{lk}x,\mathrm{pp}} \text{ such that } \begin{cases} 3.32\ \mathrm{V} \le V_1 \le 4.2\ \mathrm{V}, \\ 3.32\ \mathrm{V} \le V_2 \le 4.2\ \mathrm{V}, \\ 12\ \mathrm{V} \le V_{\mathrm{LV}} \le 14\ \mathrm{V}, \\ 30\ \mathrm{W} \le P_{\mathrm{o}}(d) \le 50\ \mathrm{W} \end{cases} \tag{4.22}$$

The results are shown in Figs. 4.12(a) and 4.12(b). The primary ripple current proportionally decreases as coupling is tighter. On the contrary, the secondary one is higher when the coupling improves, which is because there is more flux generated from primary side is coupled to the secondary side as the coupling becomes tighter. This phenomenon can also be theoretically explained by Eq. (4.21).

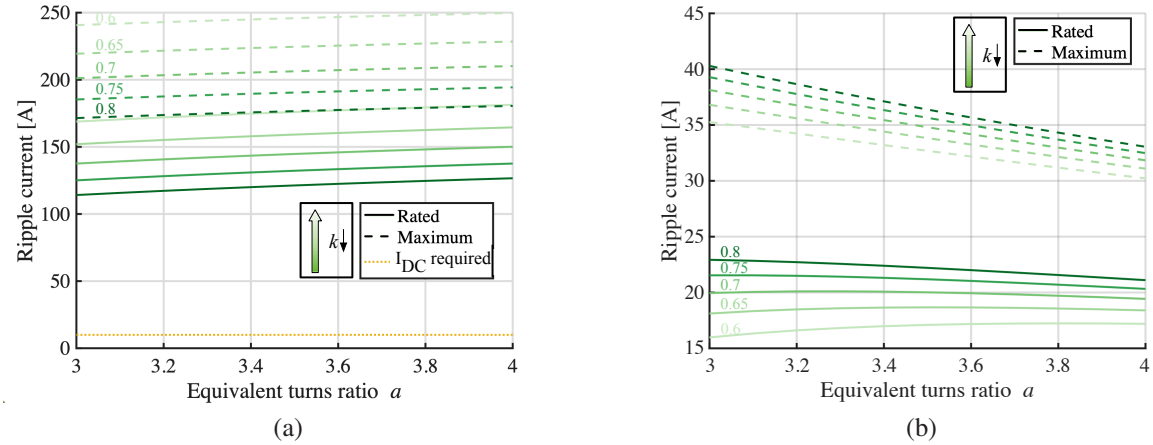



Figure 4.12: The worst leakage ripple current with different coupling factors and effective turns ratios on (a) primary side and (b) secondary side

### 4.3.4 Worst RMS currents

As the peak values partially decides the optimum MOSFETs selection, the RMS values of each component not only finalize the MOSFETs section, but also determine the conduction losses in transformer and switching devices. Combining with the primary leakage inductor voltage in Eq.

(4.14), the primary RMS current on the leakage inductor can be calculated based on the RMS current definition in Eq. (3.22).

$$\begin{aligned} I_{\text{lk1,rms}} &= \frac{T}{4\sqrt{3}L_{\text{lk1}}(V_1+V_2)(k+1)}\sqrt{k^2V_{\text{o}}'^2(V_1+V_2)^2+4a^2V_1^2V_2^2-4akV_{\text{o}}'\Gamma} \\ &= \frac{T}{4\sqrt{3}L_{\text{lk1}}(V_1+V_2)(k+1)}\sqrt{k^2\left(\frac{V_{\text{LV}}'}{2}\right)^2(V_1+V_2)^2+4a^2V_1^2V_2^2-4ak\frac{V_{\text{LV}}'}{2}\Gamma} \end{aligned} \tag{4.23}$$

The primary-referred secondary RMS current can also be obtained based on Eqs. (3.22) and (4.15).

$$\begin{aligned} I_{\text{lk2,rms}} &= \frac{T}{4\sqrt{3}L_{\text{lk2}}a(V_1+V_2)(k+1)}\sqrt{V_{\text{o}}'^2(V_1+V_2)^2+4a^2k^2V_1^2V_2^2-4akV_{\text{o}}'\Gamma} \\ &= \frac{T}{4\sqrt{3}L_{\text{lk2}}a(V_1+V_2)(k+1)}\sqrt{\left(\frac{V_{\text{LV}}'}{2}\right)^2(V_1+V_2)^2+4a^2k^2V_1^2V_2^2-4ak\frac{V_{\text{LV}}'}{2}\Gamma} \end{aligned} \tag{4.24}$$

The maximum RMS current can then be found by the same approach that is used in previous chapter, as shown in Eq. (3.34). The worst $I_{\text{lk1,rms}}$ and $I_{\text{lk2,rms}}$ are given in Fig. 4.13(a) and 4.13(b). The coupling factor and effective turns ratio are swept between 0.6 and 0.8 with 0.05 interval, and 3 and 4, respectively. As the coupling factor increases, the worst RMS currents of both primary and secondary change significantly with a rough 5 A decrease every 0.05 change of coupling factor. The loss generated by the coreless transformer is purely copper loss including skin and proximity effects. Therefore, how to tightly couple the primary and secondary windings in the coreless configuration becomes crucial to achieve high efficiency, which will be discussed in the section of coreless magnetic design.

**Model accuracy**

To verify the proposed mathematical models are accurate, a circuit-based simulation is conducted at the condition of $a = 3.5$ and the measurements are plotted in Fig. 4.14. The P2P current on the primary leakage inductor is simulated as 168.9 A, which is extremely close to the analytical result of 169.2 A calculated using Eq. 4.20. Other parameters, such as the RMS and P2P values of both primary and secondary leakage inductor currents, are compared with the simulated ones,

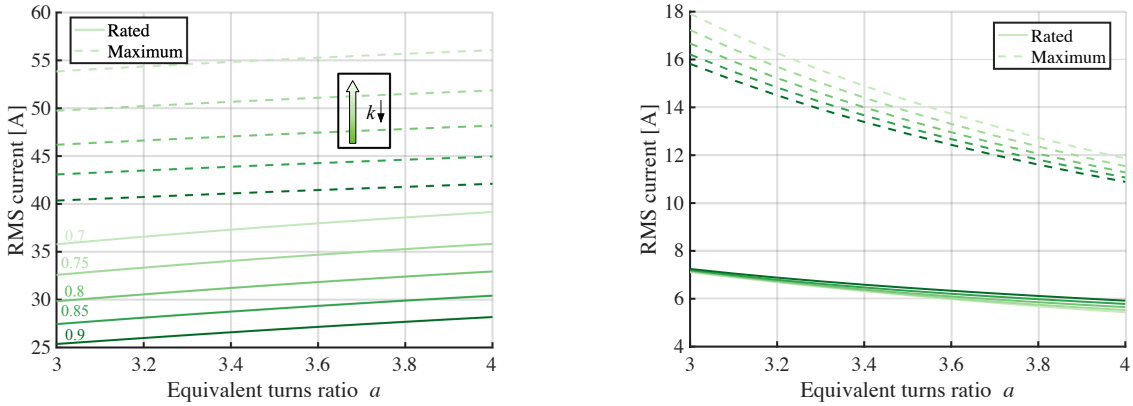



Figure 4.13: The worst leakage RMS current with different coupling factors and effective turns ratios on (a) primary side and (b) secondary side

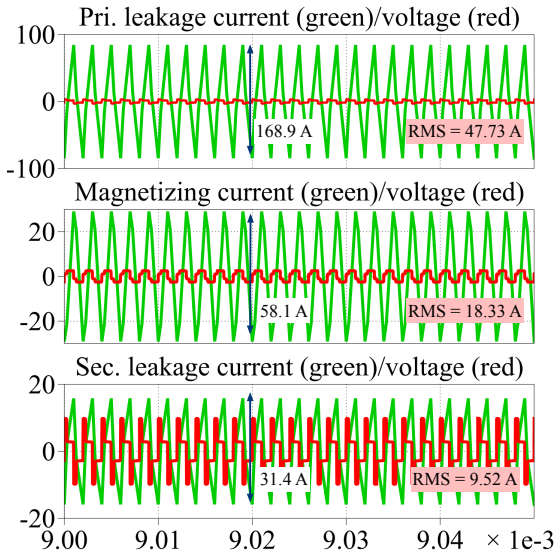



Figure 4.14: Model vs. simulation at worst case when $a = 3.5$

and the results are summarized in Table 4.4. It can be seen that the analytical model is sufficiently accurate.

Table 4.4: Model accuracy compared with simulation

| | | Analytical | Simulation | Error (%) |
|---|---|---|---|---|
| Ripple current | Pri. | 169.2 | 168.9 | 0.18 |
| | Sec. | 31.66 | 31.4 | 0.7 |
| RMS | Pri. | 47.62 | 47.73 | 0.23 |
| | Sec. | 9.47 | 9.52 | 0.5 |

### 4.3.5 Output power

In DAHB configuration, due to the existence of two capacitor on the output, the output power consists of output power on the upper capacitor and the lower capacitor, i.e. $p_o = p_{o1} + p_{o2}$. Assuming two caps' voltages are balanced and remain constant during one switching period ($V_{o1} = V_{o2} = {}^{V_{LV}}/_{2}$),

$$p_o = V_{o1} i_{o1}(t) + V_{o2} i_{o2}(t) = \frac{V_{LV}}{2} \left( i_{o1}(t) + i_{o2}(t) \right). \tag{4.25}$$

Therefore, the average output power is then obtained by integrating the currents over one period and divided by the period $T$ then multiplying the capacitor voltages.

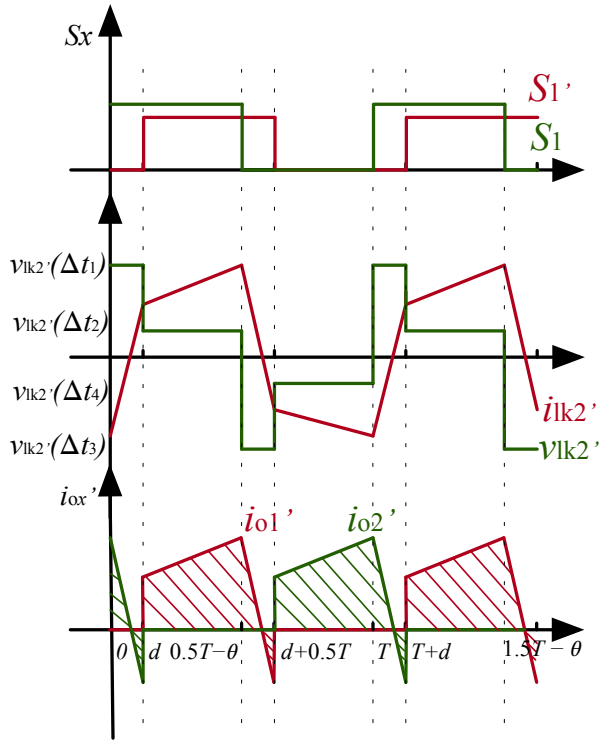



Figure 4.15: The necessary waveforms to calculate the secondary leakage inductor value

The secondary-referred leakage and output currents are drawn in Fig. 4.15. It can be seen that

the output currents $i'_{o1}$ and $i'_{o2}$ are rectified waveforms of $i'_{lk2}$ and can be represented by

$$i'_{o1} = \begin{cases} i'_{lk2} & , \quad d + nT \le t \le d + (n + 0.5)T \\ 0 & , \quad d + (n + 0.5)T \le t \le d + (n + 1)T \end{cases} , \; n \in \mathbb{Z} \tag{4.26}$$

$$i'_{o2} = \begin{cases} 0 & , \quad d + nT \le t \le d + (n + 0.5)T \\ -i'_{lk2} & , \quad d + (n + 0.5)T \le t \le d + (n + 1)T \end{cases} , \; n \in \mathbb{Z}. \tag{4.27}$$

In order to find the average current of each branch $i_{o1}$ and $i_{o2}$, the initial current $i'_{lk2}(0)$ is required. Assuming the average secondary leakage inductor current is controlled to be 0, this keeps both caps charged at the same time. If the caps happen to be out of balance, the non-zero average current can balance them in the same means of balancing the battery cells on primary side or simply by the bleeding resistor [92]. Therefore, considering the average current of $i'_{lk2}$ to be zero, the initial current $i'_{lk2}(0)$ can be calculated as follows:

$$I'_{lk2} = \frac{1}{T} \int_0^T i'_{lk2}(t)dt = 0 \tag{4.28}$$

$$i'_{lk2}(0) = \frac{k \left[ \left( -3 + 2\theta' + \theta'^2 \right) V_1 + \left( 1 + 2\theta' + \theta'^2 \right) V_2 + 2V'_o(1 - 2d') \right]}{8 f L'_{lk2}(k + 1)} \tag{4.29}$$

Eq. (4.29) shows the result with duty cycle adjustment $\theta$ involved, which can be used when the system is in transit as $\theta$ varies. In steady state, $i_{lk2}(0)$ can be obtained by substituting $\theta$ by steady-state equation (3.18), as shown in Eq. (4.30).

$$i'_{lk2}(0) = \frac{2V'_o d'(V_1 + V_2) - V'_o(V_2 + V_1) + 2V_1 V_2 k}{4 f L_{lk2}(V_1 + V_2)(k + 1)} \tag{4.30}$$

Similar with Eq. (4.28), the averaged output currents from each branch $i'_{o1}$ and $i'_{o2}$ on secondary

side can be obtained:

$$I'_{o1} = I'_{o2} = \frac{k}{k+1}\frac{1}{16fL'_{lk2}}(V_1\alpha_{lk2,i_o} + V_2\beta_{lk2,i_o}). \tag{4.31}$$

where

$$\alpha_{lk2,i_o} = -1 + 4d' + 2\theta' - 2d'^2 - \theta'^2 - 4d'\theta'$$
$$\beta_{lk2,i_o} = 1 + 2\theta' - 2d'^2 - \theta'^2 - 4d'\theta'.$$

Therefore, the total output power is then equal to

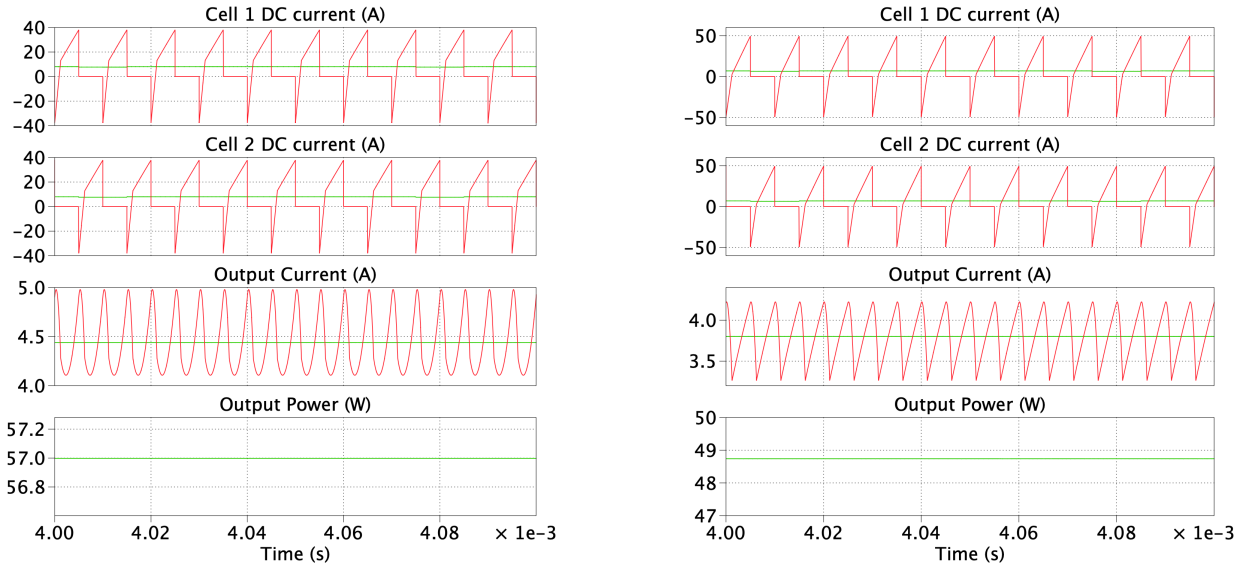
$$\begin{aligned} P_o = (I'_{o1} + I'_{o2})\frac{V'_{LV}}{2} &= \frac{k}{k+1}\frac{V'_{LV}}{16fL'_{lk2}}(V_1\alpha_{lk2,i_o} + V_2\beta_{lk2,i_o}) \\ &= \frac{k}{k+1}\frac{aV_{LV}}{16fL_{lk2}}(V_1\alpha_{lk2,i_o} + V_2\beta_{lk2,i_o}) \\ &= \underbrace{\frac{k}{k+1}\frac{a}{16fL_{lk2}}}_{\text{Power scaling factor}} V_{LV}(V_1\alpha_{lk2,i_o} + V_2\beta_{lk2,i_o}), \end{aligned} \tag{4.32}$$

which is consistent with the design of cored transformers when $k \to 1$ and $a \to n$. So this equation states the power deduction due to the imperfect coupling using coreless transformer.

It shows that if the coupling is as low as 0.7 the output power drops to 80% of the output power compared with tightly coupled transformers. Should a drop-in replacement design be wanted from cored transformer to coreless one without modifying the circuit, it can be achieved by tuning the operating frequency. The power reduction due to the lowered coupling coefficient can then be compensated by the decreased operating frequency. However, the allowable maximum RMS current for each component has to be checked in case the limit is violated. In Appendix B, the coreless transformer is installed on the HFB platform, showing the feasibility of the drop-in replacement.

A simulation is conducted to verify the proposed power equation and the correlation between cored and coreless transformer in terms of output power scaling factor. In Fig. 4.16, a constant phase shift of $d = 0.25$ is applied to both simulations while varying the coupling factor from 0.999

to 0.75. The output power is roughly 57 W when $k = 0.999$ and 48.7 W when $k = 0.75$, which introduces a scaling of 0.85. It matches the theoretical derivation above.




(a) (b)

Figure 4.16: The output power simulation with (a) $k = 0.999$ and (b) $k = 0.75$

In steady state, the duty cycle adjustment $\theta$ can be substituted by Eq. (3.18) and the power equation is rearranged to

$$P_{\mathrm{o}} = \underbrace{\frac{k}{k+1}\frac{1}{8a}\frac{1}{fL'_{\mathrm{lk2}}}}_{\text{Transformer-related power multiplier } G_{\mathrm{p}}} \underbrace{V_{\mathrm{LV}}\left(-V_{\Sigma}d'^{2} + 2V_2 d' + \frac{V_2 V_{\Sigma} - 2V_2^2}{V_{\Sigma}}\right)}_{\text{Transformer-independent } P_{\mathrm{o,base}}} \tag{4.33}$$

The output power is divided into two factors, 1) transformer-independent factor $P_{\mathrm{o,base}}$ and 2) transformer-dependent factor $G_{\mathrm{p}}$ . The transformer-independent component is mainly the function of operating conditions from the BB-APM application, e.g. cell 1 and 2 voltage range and phase shift, which are determined by the application instead of the specific transformer design. The factor $P_{\mathrm{o,base}}$ is a typical quadratic function of $d'$ with a maximum located at $d' = \frac{1}{V_1/V_2+1}$ and can be pre-calculated based on the given operation conditions. On the other hand, the multiplier $G_{\mathrm{p}}$ is based on design choices such as transformer design and operating frequency point.

## 4.4 Coreless transformer design

### 4.4.1 Requirements of the coreless transformer

It has been shown that the parameters of the transformer determines the ripple, RMS currents and output power. The transformer should be carefully design to satisfy the power capability and the efficiency expectation. The output power is firstly calculated based on the parameter-independent factor $P_{\text{o,base}}$ and selected as the base of the per-unit (pu) system, which will not change with the design decisions for transformer but only the application-oriented conditions, e.g. cell operating voltage range and LV range. In other words, the factor $P_{\text{o,base}}$ will not change as long as the operating ranges of cell and LV voltage remain the same. Then the power multiplier $G_{\text{p}}$ in Eq. (4.33) is carefully selected and designed to match the output power requirement.

The design should satisfy the power requirement under the worst condition. Therefore, a minimum $P_{\text{o,base}}$ that is resulted from a certain combination of cell voltages should be found and a power multiplier $G_{\text{p}}$ selected to guarantee the minimum power delivery. As the output power base $P_{\text{o,base}}$ is varying with phase shift in addition to cell voltages, the peak power that can be achieved from varying phase shift for given cell voltages can be found by substituting $d' = \frac{1}{V_1/V_2+1}$ into $P_{\text{o,base}}$:

$$P_{\text{o,base}}\left(\frac{1}{V_1/V_2+1}\right) = \frac{2V_{\text{LV}}V_1V_2}{V_\Sigma} \tag{4.34}$$

The minimum of Eq. (4.34) can be found using constrained optimization techniques, such as *fmincon*. The minimized cost function (4.34) with constraints $V_1, V_2 \in [2.8, 4.2]$ and $V_{\text{LV}} \in [12, 14]$ is located at 33.6 when $V_1 = V_2 = 2.8$ V, $V_{\text{LV}} = 12$ V and $d' = 0.5$. According to previous analysis, the minimum cell voltage where the rated power should be maintained is set to be 20% of SOC or 3.32 V for the NMC cells. The minimum of $P_{\text{o,base}}$ is found to be located where the cells' and LV's voltages reaches minimum. Some representative samples of the power curves are shown in Fig. 4.17. It shows the minimum of $P_{\text{o,base}}$ is at 19.92 when cells are at minimum threshold 3.32 V

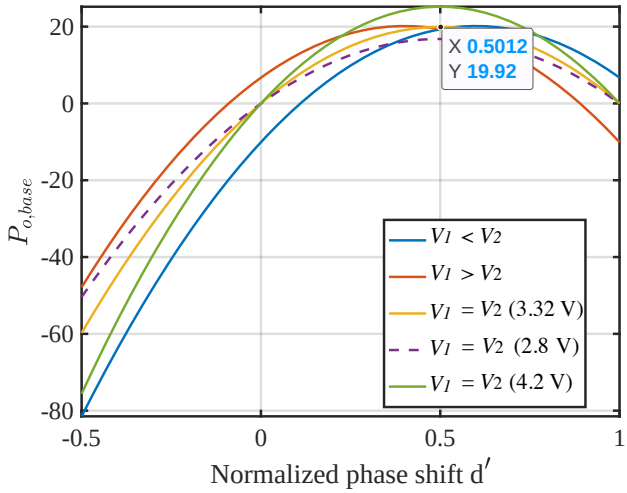



Figure 4.17: Output power in p.u. system at extreme conditions

beyond which the system is required to provide the rated power. The desired $G_{\mathrm{p}}$ can be obtained:

$$G_{\mathrm{p,required}} = \frac{k}{k+1}\frac{1}{8afL'_{\mathrm{lk2}}} \geq \frac{50}{19.92} \geq 2.51. \tag{4.35}$$

In this study, 50 W per link is selected explained also in the previous chapter. According to Eq. (4.35), the transformer needs to have at least 2.51 of the multiplier $G_{\mathrm{p}}$ for providing 50 W across entire cell operating voltage above 3.32 V. According to previous analysis, the equivalent turns ratio is determined based on coupling factor according to Eq. (4.18). However, the equivalent turns ratio $a$ cannot be accurately obtained until the transformer is designed, simulated and even assembled. In addition, the parameters of the transformer are also coupled with output power, which turns the design into a dilemma. Therefore, some form of iterative design process has to be conducted. So $a$ and $k$ are originally assumed to be 4 and 0.75 to start the transformer design, then the proposed design is fed back to power equation to see if the required power can be delivered. Adjusting the switching frequency will be correspondingly performed if power requirement cannot

be met. Then the range of transformer-related multiplier $G_\mathrm{p}$ can be simplified to

$$G_\mathrm{p} = \frac{k}{k+1}\frac{1}{8afL_{\mathrm{lk1}}} \geq 2.51 \tag{4.36}$$

$$fL_{\mathrm{lk1}} \geq \frac{1}{20a(1+\frac{1}{k})} \tag{4.37}$$

$$\approx 5.357e^{-3}$$

It is hard to know the operating frequency at this point, as the parameters of air-core transformer is not determined. But in order to give a design guidance for the transformer, switching frequency is firstly assumed to be 500 kHz. Then $L_{\mathrm{lk1}}$ is calculated to be 12.2 nH. Once the accurate leakage inductance is acquired either from FEA simulation or measurements, the frequency will be slightly adjusted to satisfy the requirement of $G_\mathrm{p}$. If the switching frequency is drastically away from initial design, the available MOSFETs need to be re-evaluated in terms of current carrying capability and performance. Based on the initial approximation, further validation needs to be conducted.

### 4.4.2 Possible winding layouts

According to Eq. (4.18), the effective turns ratio needs to be at least 3. Therefore, the physical turns ratio is chosen to be 4 to provide a reasonable buffer. Since the core is removed, the number of turns can be designed arbitrarily instead of following the Faraday's Law for a bounded peak flux density switching as shown in Eq. (3.36). The design is minimal when primary number of turns is picked for 1 and thus secondary one is picked for 4. Then the possible combinations of planar winding layouts are illustrated in Fig. 4.18

It can be seen that the 2-layer and 8-layer designs are wide and tall, respectively, leading to a larger space usage. In addition, the 2-layer is a non-interleaved structure that increases the losses due to eddy current and proximity effects [47], [68], [93]. On the other hand, the interleaved structures like 4-layer and 8-layer designs will result in better coupling and less losses due to the improved magnetomotive force (MMF) distribution. However, the 8-layer structure is costly to manufacture due to its high layer count. The 4-layer structure is thus selected while maintain

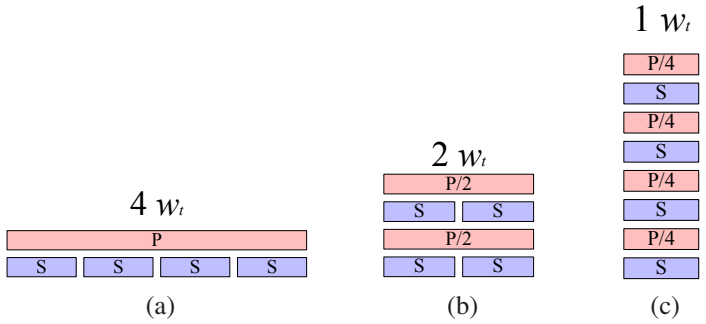



Figure 4.18: The possible planar winding layouts with (a) 2-layer, (b) 4-layer and (c) 8-layer structures (cross-section on one side of the windings)

low-profile and tight coupling.

### 4.4.3 Correlation between winding geometries and coupling coefficient

According to previous circuit analysis, a high coupling coefficient is desired as it determines the effective output power ratio and transformer RMS currents that is closely tied to the conduction loss. Unlike the conventional transformer equipped with the magnetic cores, the coupling is tightly correlated with the winding design, especially the geometry and spacing. A various of optimizations on the winding structure are performed to guide the design of the coreless transformer to achieve the high coupling coefficient.

A helical winding type is drawn in the ANSYS/Maxwell 3D modeler with the 4-layer structure as shown in Fig.4.18b to investigate how the geometrical parameters affect the coupling coefficient. The Eddy Current solver is selected to simulate the transformer parameters under the high-frequency excitation. The 500-kHz simulations are selected to show later as a reference since the coupling coefficient stays relatively constant around 500 kHz.

**Coupling coefficient vs. winding radius**

Firstly, the inner winding radius is varied from 20 mm to 150 mm. The change of the coupling coefficient is captured in Fig. 4.20. The plot suggests that the coupling improves as the radius of the windings increases. However, as a trade off, the resistance also grows as the radius increases.

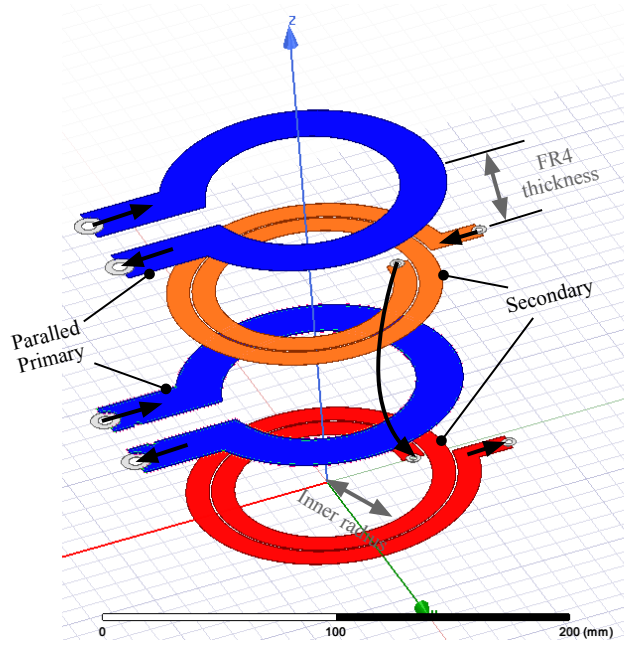



Figure 4.19: The ANSYS/Maxwell model of a helical 4-layer coreless transformer

In addition, the space that the transformer takes also increases. Therefore, a trade-off between radius and the coupling coefficient has to be made.

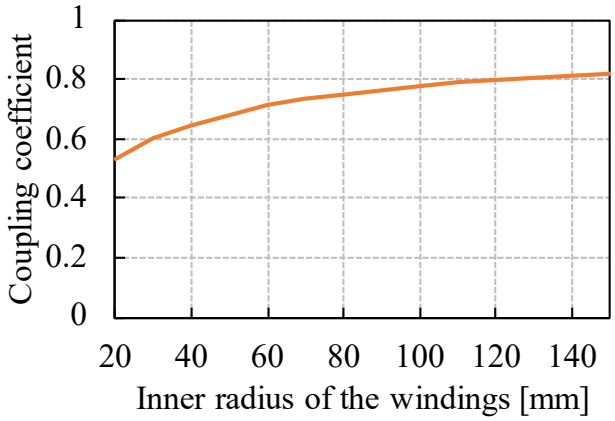



Figure 4.20: The coupling coefficient vs. windings inner radius

**Coupling factor vs. copper thickness and FR4 thickness**

Aside from the radius, the distance between each winding is also dominant in coupling coefficient. At a fixed 90 mm inner radius, the different commonly used copper thickness and insulation

(FR4) thickness are swept to obtain the correlation with the coupling coefficient. The results are summarized in Fig. 4.21. They clearly show that FR4 thickness is inversely proportional to coupling effect, i.e. shorter distance between windings leads to higher coupling. Similarly, thicker copper lowers the coupling effect, which can be explained by increased effective copper-to-copper distance.

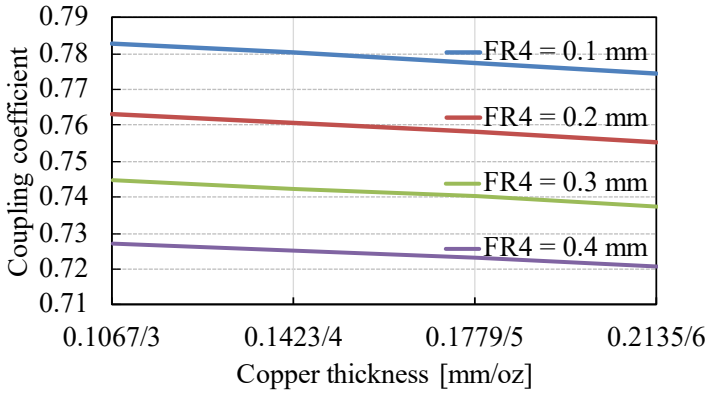
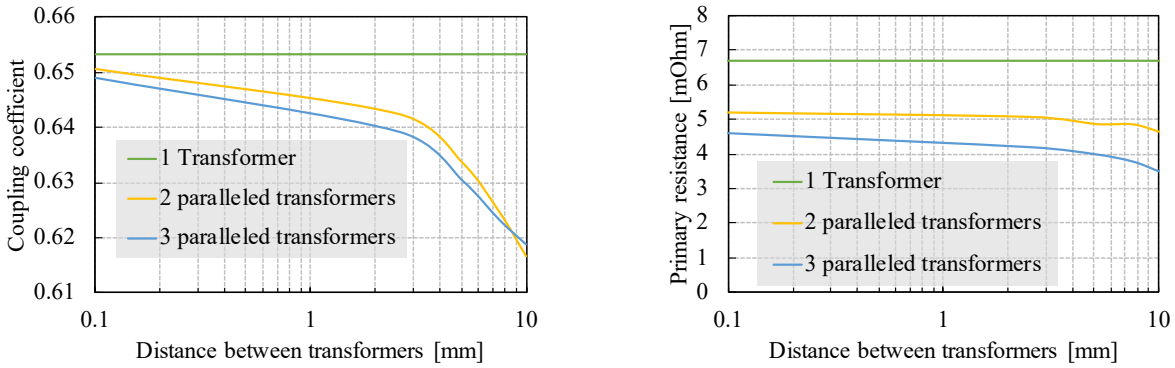



Figure 4.21: The coupling coefficient vs. copper and FR4 thickness

**Paralleled transformers vs. coupling coefficient and resistance**

Sometimes, if the resistance of the windings needs to be minimized to reduce the conduction loss while the trace width is already maximized, the cross area of the copper needs to be increased. However, increasing on copper thickness while maintaining the same layer-to-layer distance is challenging due to manufacturers' capabilities. The multiple transformers can be paralleled to reduce the resistance, and thus, to increase the current carrying capability. It is worth to investigate the effect of paralleled transformers on the coupling coefficient. The simulations with 1-3 paralleled transformers show that the change on the coupling coefficient when the number of paralleled transformers and the distance between the paralleled transformers are varying, as shown in Fig. 4.22(a). The increasing number of paralleled transformers slightly reduces the coupling coefficient when the distance is small, e.g. 0.1 mm. However, the coupling becomes worse if they are spaced relatively far away from each other. The primary resistance shown in Fig. 4.22(b) decreases as the

more transformers are paralleled, which is expected. Therefore, the distance between the paralleled transformers should be minimized when maximum coupling coefficient is desired.




(a) (b)

Figure 4.22: The simulated effect of distance between paralleled transformers on (a) coupling coefficient and (b) primary resistance, with a winding inner radius of 20 mm

### 4.4.4 Coreless transformer design suggestions

Based on the previous analysis, in order to increase the coupling, the windings need to make as large as possible while reducing the winding distance. Therefore, there needs to be a guidance for the coreless transformer design. However, the winding structure is dependent on the integration level of the system. Due to the removal of the core, there are two options for placing the main electronics components and the transformer: a "frame" transformer and a "discrete" transformer. The frame transformer circulates the windings around the main electronics components with a highest integration level. On the other hand, the PCB transformer resembling a discrete transformer can be placed on the side of the main electronics components. These two options are illustrated in Fig. 4.23. Note that the transformer is not scaled proportionally. The frame transformer structure slightly sacrifices the system efficiency due to the Eddy-current losses generated in the traces or components circulated inside of the transformer. The frame transformer geometry is limited by the area of the main component section. In addition, the frame transformer needs to have the same number of PCB layers as the main components. If the required number of stack-up for the frame

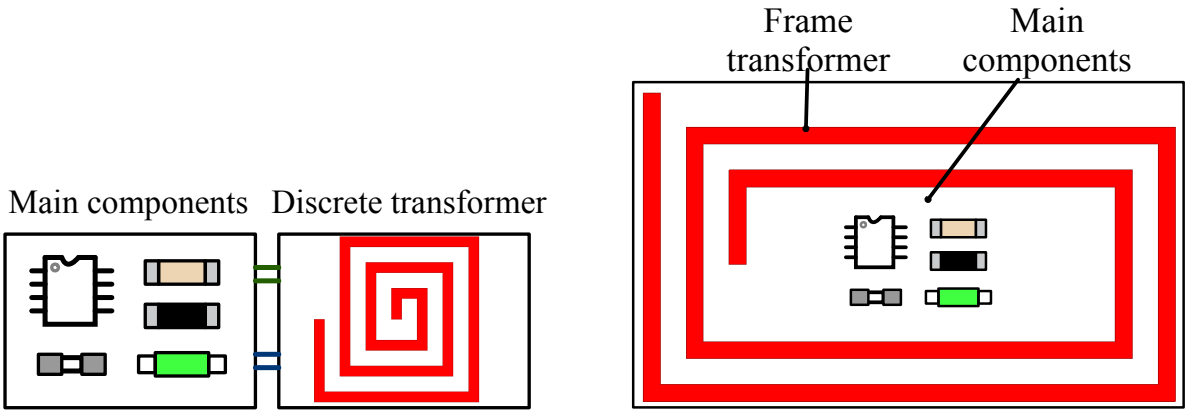



Figure 4.23: The possible transformer layout structures: (a) discrete transformer structure and (b) frame transformer structure

transformer is larger than the main PCB, e.g. 8-layer transformer structure on a 4-layer PCB, it is infeasible to manufacture on the same board unless the main PCB is increased to 8 layers. Unlike the discrete transformer that can be manufactured separately from the main PCB, the frame transformer will be limited by the main PCB. So there are more limitations on the designs of the frame transformer than the discrete transformer. The summary of tunable parameters of designing a high coupling coefficient coreless transformers is listed in Table 4.5

### 4.4.5 Main PCB layout and stack-up options

The necessary electronics are firstly laid out according to the topology in Fig. 4.4, based on which the frame or discrete coreless transformers can be correspondingly designed given the space constrains. The dimensions of the main component board are illustrated in Fig. 4.24. The frame

Table 4.5: The tunable parameters of the coreless transformer vs. coupling coefficient

| **Parameter** | **Tuning direction** | **Coupling coefficient** |
|---|---|---|
| Winding inner radius | ↑ | ↑ |
| Distance between internal layers | ↓ | ↑ |
| Copper thickness | ↓ | ↑ |
| Number of paralleled transformers | ↑ | ↘ (resistance ↓) |
| Distance between paralleled transformers | ↓ | ↑ |

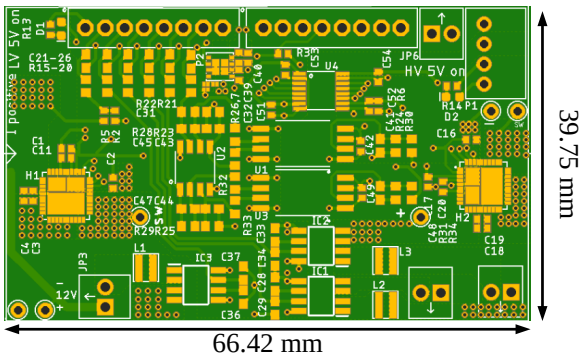



Figure 4.24: The dimensions of the main component board

transformer then needs to circulate around the rectangular area defined by the main component board.

Based on previous analysis, the winding radius and layer-to-layer distance govern the coupling coefficient. The transformer can be designed as large as possible to increase the coupling between windings. However, to also keep the footprint compact, the winding radius is set to the exact size of the main component PCB for the frame transformer with a 5 mm tolerance between windings and main component area. Instead, the discrete transformer can be designed arbitrarily.

On the other hand, the layer-to-layer distance, or FR4 thickness, should be kept minimal within galvanic isolation requirement and manufacturing capabilities. However, the achievable FR4 thickness is determined by the copper thickness and the number of PCB layers. Therefore, not all the combinations in Fig. 4.21 can be properly manufactured, especially the 4-layer configuration with 6-oz copper and 0.1-mm FR4. After a survey of the PCB manufacturers' capabilities, the stack-up of 4-layer board with 3-oz copper and 0.1-mm FR4 is selected to maintain a minimized layer-to-layer distance with the maximized copper weight. In addition, two transformers are paralleled to increase current carrying capability and thus, to lower conduction loss.

### 4.4.6 Maxwell simulations

The 3D models of the windings and the main component board are imported from Eagle CAD to ANSYS Maxwell to perform FEA simulations at desired frequencies, as shown in Fig. 4.25.

The extracted parameters from the simulation are summarized in Table 4.6.

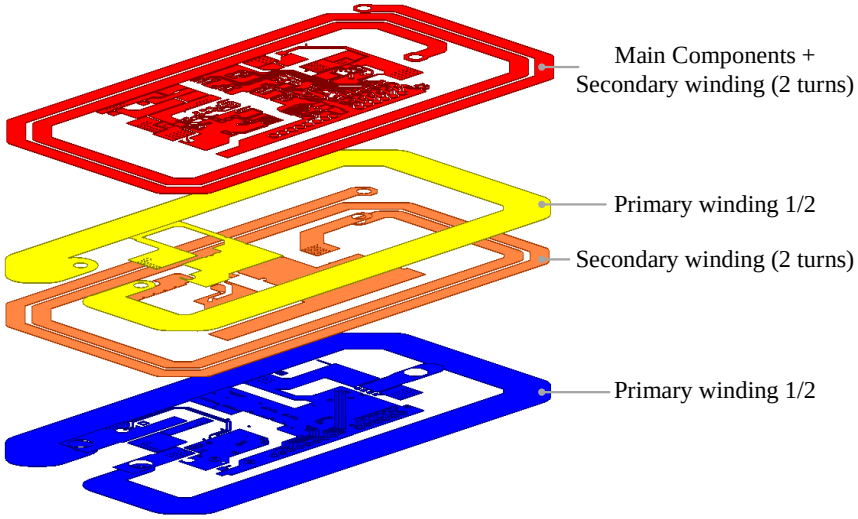



Figure 4.25: The 3D model for FEA in Maxwell/ANSYS

Table 4.6: The primary parameters of the coreless transformer

| Magnetization inductance | Leakage inductance | coupling coefficient | Effective turns ratio |
|---|---|---|---|
| 141.5 nH | 24.9 nH | 0.85 | 3.74 |

## 4.5 Experimental results

The self-designed power stage and coreless transformer are shown in Fig. 4.26. The compact half bridge modules SiC789 from Vishay are used in the power conversion stage, which is selected based on the worst RMS and ripple current shown in Fig. 4.13(a). The primary cells are simulated by two DC power supplies; the LV battery and load are replaced by a DC power supply in parallel with a DC electric load. Different balancing modes have been verified on the test bench and plotted in Fig. 4.27. The Mode C C2LV only where two cells provide the same amount of power to LV load is shown in Fig. 4.27a. With the duty cycle adjustment $\theta$, the DC bias current can be introduced between cells, resulting in one cell provides more power than the other. The cell 2 can also be entirely disabled by controlling the DC bias while doubling cell 1 current, as shown in Fig. 4.27(c). Note that the cell 2 can be set to receive charges from cell 1 if $I_{DC}$ continues to increase.

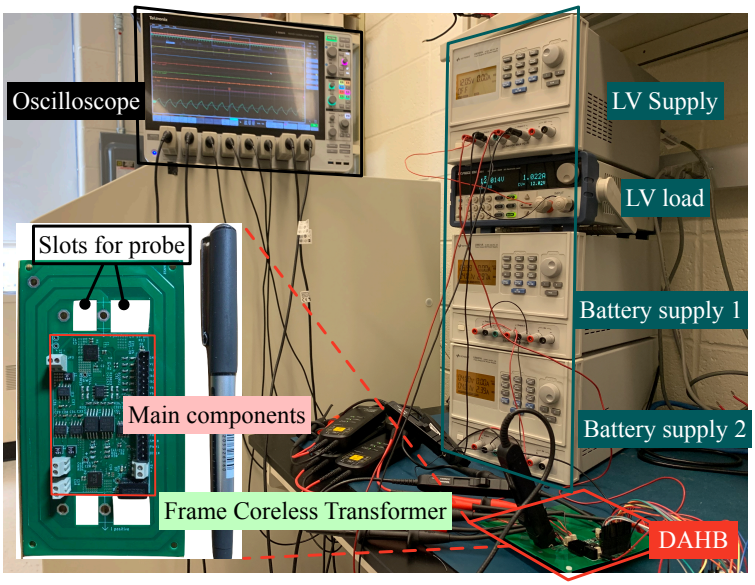



Figure 4.26: The prototype of the proposed DAHB with coreless transformer under testing

In addition, reverse power flow (LV2C) can be achieved by reversing the phase shift angle between primary and secondary switches. The efficiency of the prototype across the entire power range has been plotted in Fig. 4.28. The efficiency constantly surpasses 72% when the output power is greater than 8 W. The peak efficiency is reached at 80% with the higher operating frequency where less RMS current is flowing and the circuit is running under ZVS. Note that the higher efficiency can be achieved with the MOSFETs that have lower $R_{\text{ds,on}}$.

## 4.6 Conclusion

The HFB topology is modified to further simplify the circuit design and thus, reduce the cost of the BB-APM. Instead of the full bridge on the secondary side, only a half bridge is kept on the secondary side without sacrificing circuit functions. In addition, the core of the transformer is removed, leading to higher integration level of the circuit. The removal of the core invalidates the derivations of the system model in Chapter 3 due to the significant leakage inductance. A more generalized system model is proposed considering the coupling coefficient and effective turns ratio. The model is verified with a high-fidelity PLECS circuit model with a very high consistency.

It is shown that the coupling coefficient is preferred as high as possible to reduce the undesired

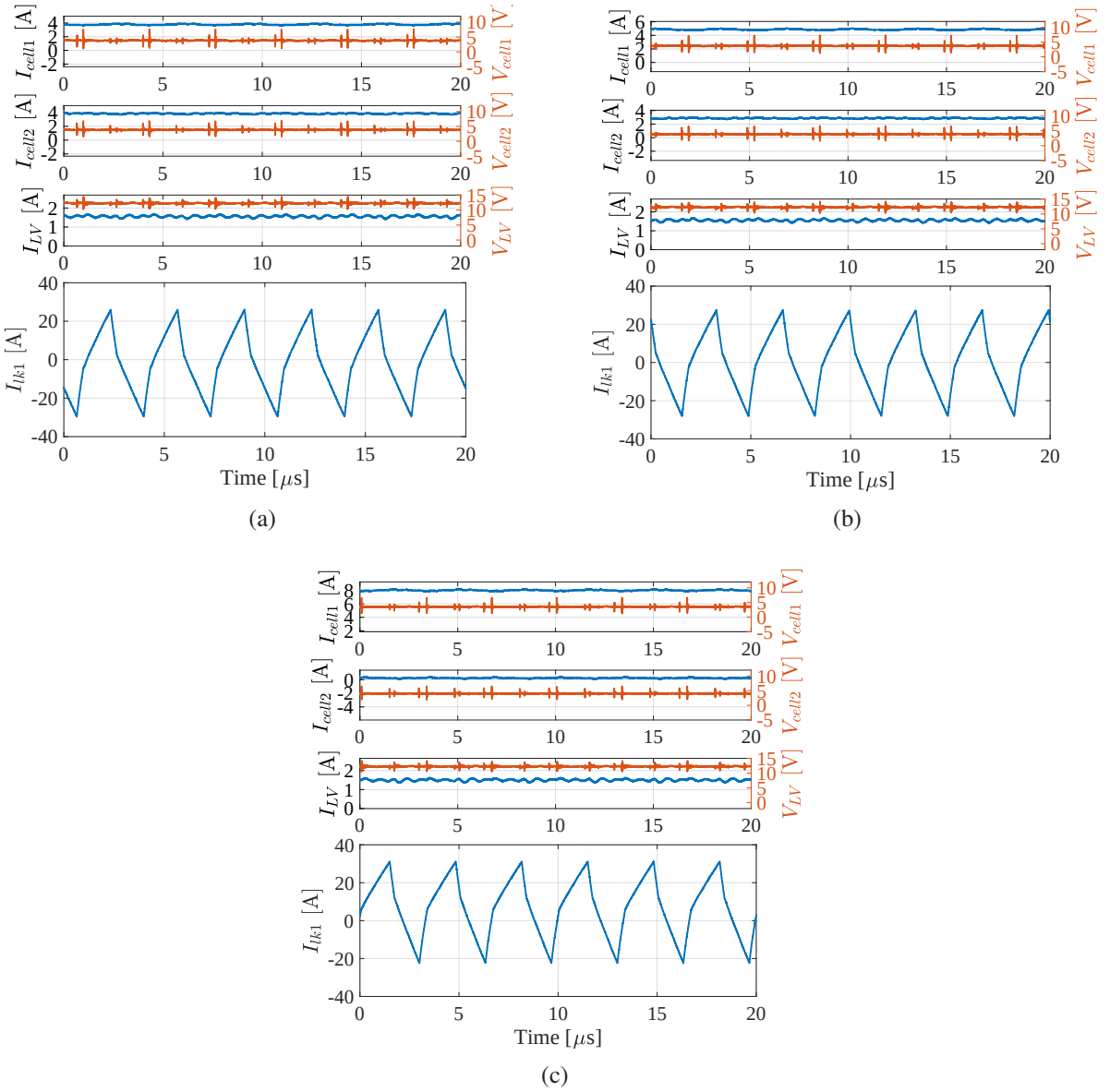



Figure 4.27: The measured waveforms at 300 kHz when consuming 30 W with (a) $I_{\mathrm{DC}}$ = 0 A, (b) $I_{\mathrm{DC}}$ = 2 A, (c) $I_{\mathrm{cell2}}$ = 0 A, cell 1 providing full power (replotted in MATLAB)

RMS currents. The requirement for the characteristics of the coreless transformer is given based on an application-independent multiplier $G_{\mathrm{p}}$. A simple check can determine the power capability of a designed coreless transformer. In order to optimize the coupling coefficient, a generalized 4-layer coreless transformer is developed in ANSYS/Maxwell to investigate the effect of varying geometric parameters. Design suggestions on the coreless transformer are discussed to maximize the coupling coefficient. Following the design suggestions, a prototype DAHB with a coreless

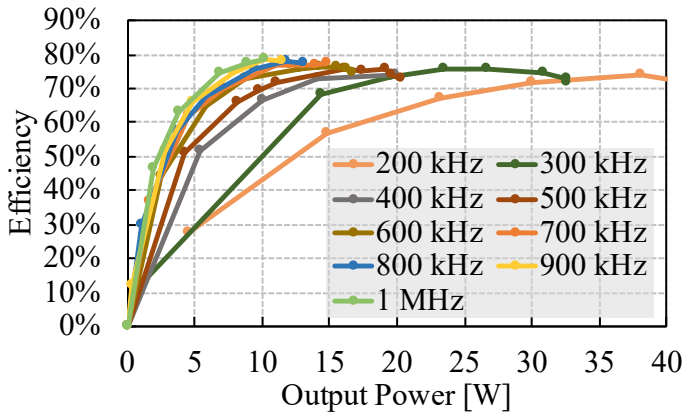



Figure 4.28: The measured efficiency with respect to output power at different operating frequency

transformer is built and tested. And all balancing modes are verified.

# Chapter 5: Conduction-Loss Based Variable Frequency Modulation

The DAB-based converters with the phase-shift modulation inherently equip with the soft-switching capability to increase the efficiency of the converter [46], [85]. However, the converters are commonly designed for their nominal load conditions under ZVS operation. When the converter is operating with the low power load, the soft-switching capability is compromised.

In order to overcome the issue, the switching frequency is increased at low-load conditions to maintain soft-switching capability and it is reduced to nominal switching frequency when load increases. This is so-called variable frequency modulation. The optimized VFM [94] is achieved through comprehensively analyzing each component and concluding on an optimal operating frequency to minimize the loss of the entire system. The repetitive modeling and time-consuming surveying of the components that generate the major losses, such as power MOSFETs and inductors/transformers, are required. Another strategy is oriented to enable the ZVS at its minimal energy, so-called critical soft switching [95], [96]. In addition, the ZVS current is significantly dynamic and highly dependent on the half-bridge input voltages which are often assumed to be identical for most of the applications [46], [85], i.e. $V_1 = V_2$. However, the additional freedom on the half-bridge voltages leads to a 4D-look-up table (LUT) of a function of $[V_1, V_2, d, f]$ instead of $[V_{\text{in}}, d, f]$, which makes storing and extracting the desired operating points less efficient on the embedded systems. This chapter analyzes the conditions to enable ZVS at low load conditions, and proposes a simplified criteria and a control law of VFM to drive the half-bridge based topologies, e.g. DAB, HFB and DAHB, to their pseudo-optimal condition in order to increase the system efficiency at low-load conditions without complicating the implementation on a microcontroller.

## 5.1 Critical soft switching

The MOSFETs that are soft-switched need to satisfy some criteria. This section describes the requirements that are necessary for achieving ZVS for the primary and secondary switches.

### 5.1.1 Primary-side ZVS

The nominal waveform of the current across the primary leakage inductor is re-illustrated in Fig. 5.1(a). The primary switch $S_2$ is turned on at the time instance $[(n + 0.5)T - \theta]$, and to achieve the ZVS, the current has to flow in the direction depicted in Fig. 5.1b, in order to discharge the parasitic capacitor $C_{\text{oss2}}$ before $S_2$ is turned on. The required current direction accordingly demands the current to be larger than the commutating current $I_{\text{cm}}$ that fully discharges the parasitic capacitor of the MOSFET that is softly turned on. Similarly, before primary switch $S_1$ is switched on, the current should be reversed and larger than $I_{\text{cm}}$. The amplitude of the commutating current is dependent on the switch voltage $v_{\text{ds}}$, parasitic capacitance $C_{\text{oss}}$ and desired deadtime $t_{\text{dead}}$. For the operation in Fig. 5.1(c), at the beginning of discharging/charging the parasitic capacitors, the primary leakage inductor current is divided to two branches, i.e. the switch to be turned on $S_1$ and the switch to be turned off $S_2$

$$i_{\text{lk1}}(t) = i_{\text{oss1}} + i_{\text{oss2}} = C_{\text{oss2}}\frac{dv_{\text{coss2}}}{dt} - C_{\text{oss1}}\frac{dv_{\text{coss1}}}{dt}. \tag{5.1}$$

It can be integrated over the deadtime $t_{\text{dead}}$ during which the soft commutating is allowed to complete

$$\int_0^{t_{\text{dead}}} i_{\text{lk2}}(t)dt = \int_0^{V_\Sigma} C_{\text{oss2}}dv_{\text{coss2}} - \int_{V_\Sigma}^0 C_{\text{oss1}}dv_{\text{coss1}} \tag{5.2}$$

$$i_{\text{lk2}}t_{\text{dead}} = V_\Sigma(C_{\text{oss1}} + C_{\text{oss2}}). \tag{5.3}$$

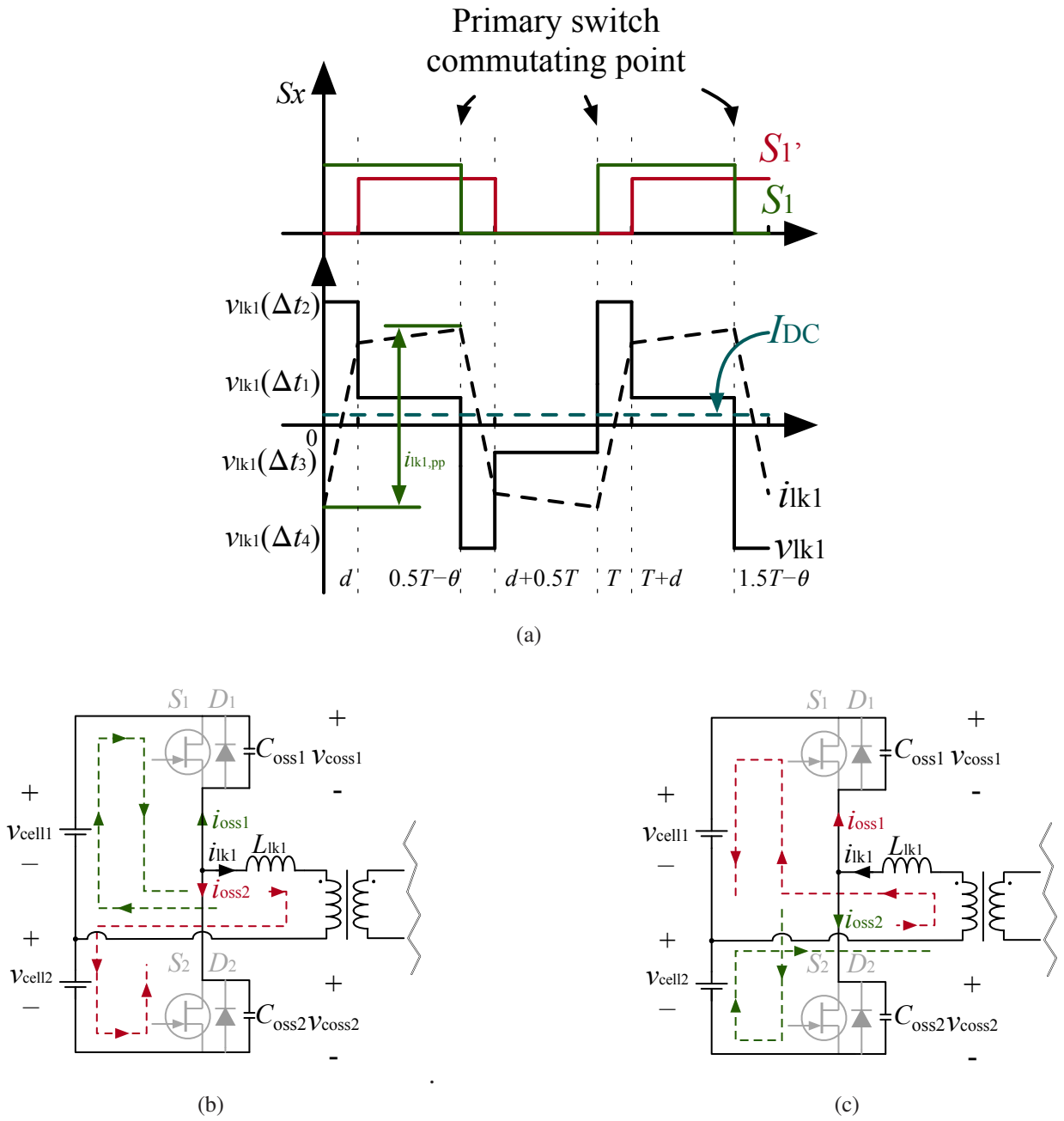



Figure 5.1: The ZVS condition for primary switches: (a) the primary leakage inductor current waveform; the current flow to achieve ZVS: (b) at time instance of $0.5T - \theta$, (c) at time instance of $T$

Assuming the leakage inductor current during the dead time is constant, it can further be simplified as

$$I_{\text{cm}} = \frac{V_{\Sigma}(C_{\text{oss1}} + C_{\text{oss2}})}{t_{\text{dead}}}. \tag{5.4}$$

Therefore, given the P2P current ($i_{\mathrm{lk1,pp}}$) of $i_{\mathrm{lk1}}$ and DC bias current $I_{\mathrm{DC}}$, the condition for achieving ZVS on primary-side switches is

$$I_{\mathrm{ZVS}}^{\mathrm{pri}} = I_{\mathrm{pp,lk1}} \geq I_{\mathrm{DC}} + 2I_{\mathrm{cm}}. \tag{5.5}$$

If the ZVS over the entire operating region is desired, the minimum current ripple of $I_{\mathrm{lk1}}$ that can be calculated using optimization algorithms (e.g. *fmincon*) according to Eq. (4.20) needs to satisfy the condition in Eq. (5.5). As long as the results satisfy the inequality of Eq. (5.5), the soft switching is guaranteed.

If the coupling and effective turns ratio in practice are different than assumption, the capability of ZVS needs to be reevaluated. In order to avoid unnecessarily repeated work, the parametric sweep of the P2P current is conducted with respect to coupling factor and effective turns ratio. This analysis was performed when investigating the effect of the coupling factor on the ripple current in Fig. 4.12(a). It can be seen from Fig. 4.12(a) that achieving primary ZVS is not challenging with a vide range of coupling and effective turns ratio combinations. Therefore, the primary switches are soft-switched within the entire operating range.

### 5.1.2 Secondary-side ZVS

Similarly, the secondary-side switches can be soft-switched if the $I_{\mathrm{ZVS}}^{\mathrm{sec}\prime}$ in Fig. 5.2 meet the condition like Eq. (5.5). The derivation of the commutating current requirement is identical to the primary side due to the symmetry of the topology. The minimum required amplitude for secondary switches can be simplified due to the absence of the DC bias current as shown below

$$I_{\mathrm{ZVS}}^{\mathrm{sec}\prime} \geq 2aI_{\mathrm{cm}}. \tag{5.6}$$

The expression of $I_{\mathrm{ZVS}}^{\mathrm{sec}\prime}$ can be obtained as

$$I_{\mathrm{ZVS}}^{\mathrm{sec}\prime} = \frac{T\left[k\left(V_1 + V_2\right)d - kV_2 + V_{\mathrm{o}}'\right]}{2L_{\mathrm{lk2}}'a(k+1)}. \tag{5.7}$$

If the operating conditions, such as $V_1$, $V_2$ and $V_o'$, are given, the combination of the switching period $T$ and phase shift $d$ can be determined. How to choose them is then answered by the constant power regulation.

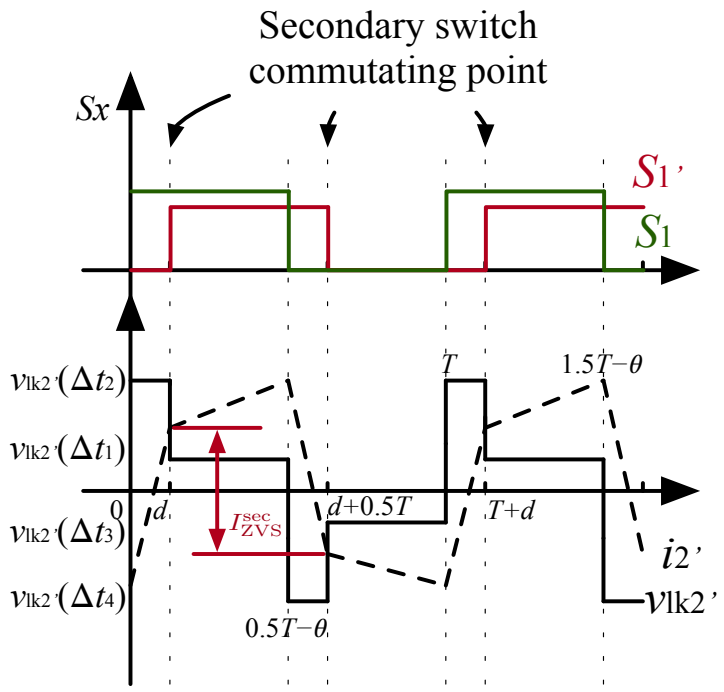



Figure 5.2: The worst primary leakage ripple current with different coupling factors and effective turns ratios

### 5.1.3 Constant power regulation

The frequency and phase shift are swept to obtain the output power trajectory given the parameters of the DAHB. Since the HFB modeling is a special condition of the coreless DAHB, the same tendency of HFB should be observed. As it can be seen from previous analysis and Fig. 5.3 that the output power is a function of the switching frequency and phase shift. Sometimes, the cells are required to generate a constant power while achieving ZVS. Based on the previously calculated combination of $T$ and $d$ using Eq. (5.7), they can be solved by combining with the output power

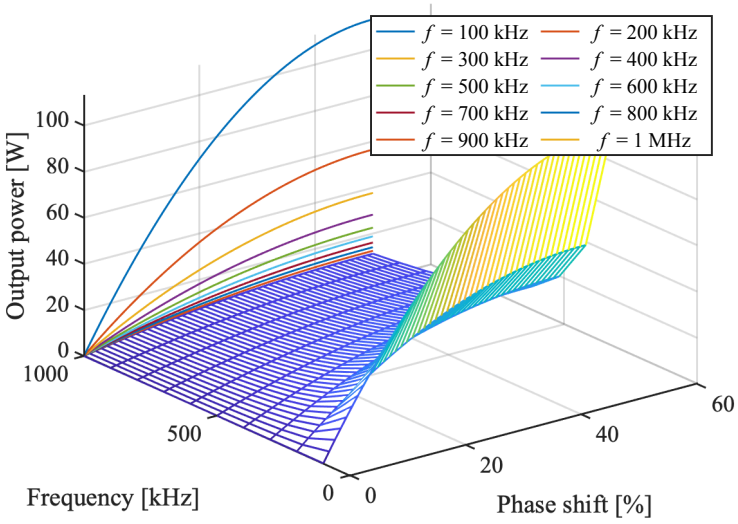



Figure 5.3: The output power trajectory with varying frequency and phase shift

regulation, as shown in Eq. (5.8).

$$\begin{cases} I_{\mathrm{ZVS}}^{\mathrm{sec}\prime}(d,T) \geq 2aI_{\mathrm{cm}} \\ P_{\mathrm{o}}(d,T) = P_{\mathrm{o,required}} \end{cases} \tag{5.8}$$

A LUT can be generated to locate the phase shift and the switching frequency in real time. However, the input and output voltages also play an important role on the output power and ZVS current requirement, as explained previously. Therefore, a very large 4-D LUT is needed to cover all the operation conditions, which complicates the computations in real-time embedded systems and may even lead to infeasibility in the computation-constrained environments.

### 5.1.4 Experimental results

Two steady-state operations tested on the HFB test bench are shown in Fig. 5.4. It can be seen that a higher $I_{\mathrm{DC}}$ at 3 A is achieved with ZVS enabled at 600 kHz whereas the ZVS condition is violated with a lower C2C current, 2 A, at 300 kHz. In addition, it can be observed that the ripple and RMS currents at 600 kHz are much smaller than the ones at 300 kHz as expected, leading to less conduction loss. This reduced ripple/RMS current can be explained by Eqs. (4.21) and (4.24). This behavior will be utilized to derive the proposed conduction-loss based VFM modulation in

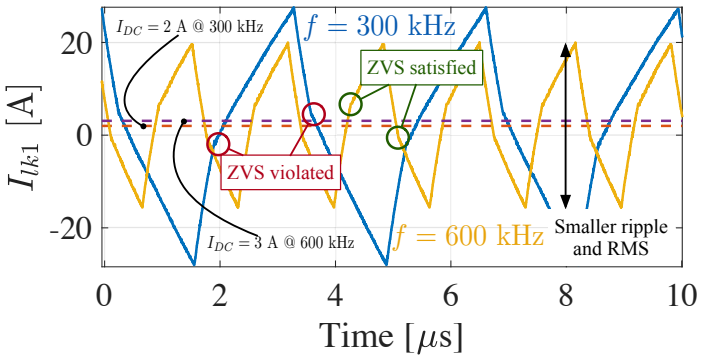



Figure 5.4: The measured waveforms of leakage inductor current at 300 kHz and 600 kHz

the following section.

### 5.1.5 Benefits brought by VFM

Not only can the VFM enable soft switching at low-load condition, but also it can reduce the ripple and RMS currents of the transformer. At low-load condition, the frequency is increased and the phase shift is controlled correspondingly to provide the required power. A statistical analysis is conducted to illustrate how increasing frequency results in the lowered output power levels that can achieve ZVS. Given that primary-side switches are always soft switched, the secondary-side

Table 5.1: Voltage ranges for VFM calculation

| | |
|---|---|
| Cell voltages | 3.3 – 4.2 V |
| LV voltage | 12 – 14 V |
| Output Capacitor voltage | 6 – 7 V |

switches are soft switched under conditions solved by Eq. (5.8). In this analysis, the transformer parameters listed in Table 4.6 are substituted to find the minimum output power that enables a 0.5 A of $I_{\text{ZVS}}^{\text{sec}}$. The operating frequencies are swept from 200 kHz to 1 MHz with the operating conditions defined in Table 5.1. And the ZVS-operatable minimum output power is obtained, as shown in the box plot Fig. 5.5. It shows that the overall trend of the output power to achieve ZVS is decreasing with higher switching frequency. The soft switching can be realized at 10 W load under the most operating conditions at 1 MHz. On the other hand, if the circuit is operated at

600 kHz, the soft switching can not be achieved. Therefore, higher operating switching frequency lowers the output power that is required to enable ZVS.

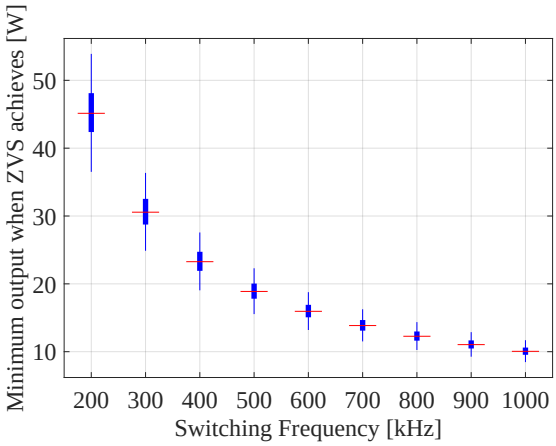



Figure 5.5: The minimum output power when soft switching is enabled at different frequencies

The RMS current for a given load level at higher operating frequency is significantly less than the one at low operating frequency. For the same ranges of the input voltages and frequencies, the RMS currents for a 10-W power load between 200 kHz and 1 MHz are shown in Fig. 5.6. It shows that the RMS current at 200 kHz is roughly seven times larger than the one at 1 MHz, leading to 49 times higher conduction loss compared the one switching at 1 MHz while the switching loss is only theoretically 5 times larger. Same trend is expected for higher power load, except that the increased power requirement may not be satisfied at higher frequency, based on the power equation in Eq. (4.32). Note that the lower RMS current still reduces the conduction loss significantly even though the increased AC resistance is expected at higher switching frequency. It will be analyzed later this Chapter.

### 5.1.6 Drawbacks of the critical soft switching

The critical soft-switching is only oriented to eliminate the switching loss from turning on the MOSFETs. The conduction loss, as another dominant source of the system loss in the phase-shifted half-bridge converters [73], however, is not considered.

In addition, the operating points are solved from two complicated equations depending on input

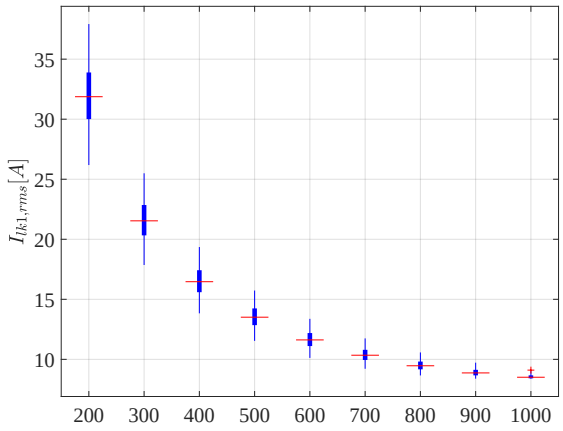



Figure 5.6: The RMS current for a 10 W load at different frequencies

and output voltages. In order to implement it on the embedded systems, a large LUT is needed. This may not be feasible in computation-constrained environments. And the system runs in an open-loop fashion, which makes it impossible to compensate or correct for any changes under the disturbances. The following sections propose a conduction-loss oriented VFM to inherit the soft-switching capability and reduce the complexity of the control strategy.

## 5.2 Power losses in the half-bridge based of topologies

In order to simplify the control law of VFM to a reasonable extent and take conduction losses into account, the sources of the power losses from the circuit should be identified. The frequency dependency on each loss component needs to be analyzed so that the simplified control law can capture the most dominant effects without sacrificing the system efficiency compared with a fully modeled system.

### 5.2.1 Transformers

The losses of the transformers consist of conduction loss and core loss as explained in previous chapters. Both of them are proved to be non-linearly frequency-dependent. However, if the net effect of the both losses with the varying frequency can be identified, a simpler control law can be developed without the comprehensive modeling.

**Conduction loss**

The conduction loss is frequency dependent due to the skin and proximity effects developed on the conductor at high frequencies. The total conduction losses due to the DC and AC resistances can be represented by

$$P_{\mathrm{cu}}^{\mathrm{trans}} = R_{\mathrm{DC}}^{\mathrm{pri}} \sum_{k=0}^{+\infty} F_{\mathrm{r}}^{\mathrm{pri}}(f_k) I_{\mathrm{lk1,rms}}(f_k) + R_{\mathrm{DC}}^{\mathrm{sec}} \sum_{k=0}^{+\infty} F_{\mathrm{r}}^{\mathrm{sec}}(f_k) I_{\mathrm{lk2,rms}}(f_k) \tag{5.9}$$

where $F_{\mathrm{r}}^{\mathrm{pri}}(f_k)$ is the primary-side AC/DC resistance ratio at the $k$th harmonic frequency $f_k$. Similarly, $F_{\mathrm{r}}^{\mathrm{sec}}(f_k)$ is the secondary-side AC/DC resistance ratio at the $k$th harmonic frequency $f_k$. DC component is evaluated at $f_0$. $I_{\mathrm{lk1,rms}}(f_k)$ and $I_{\mathrm{lk2,rms}}(f_k)$ denote the RMS currents at frequency $f_k$ for primary and secondary sides, which are calculated by the Fourier Series of the leakage inductor currents. The detailed Fourier Series of the leakage inductor currents is analyzed and given in [97]. The derivations in [97] show that the higher-order RMS component can be represented by the fundamental one.

$$I_{\mathrm{lk}x,\mathrm{rms}}^2(f_k) = \frac{I_{\mathrm{lk}x,\mathrm{rms}}^2(f_1)}{k^4},\ k \in \mathbb{Z}^+ \tag{5.10}$$

The total RMS currents are the geometrical summations of the RMS currents at each harmonic frequency, i.e.

$$I_{\mathrm{lk}x,\mathrm{rms}}^2 = \underbrace{I_{\mathrm{lk}x,\mathrm{rms}}(f_0)^2}_{\text{DC component}} + I_{\mathrm{lk}x,\mathrm{rms}}(f_1)^2 + \underbrace{I_{\mathrm{lk}x,\mathrm{rms}}(f_2)^2 + \ldots}_{\text{negligible}} \tag{5.11}$$

The DC component in the equation above is frequency independent but balancing-mode dependent. In addition, the DC component on the secondary side does not exist. As a result, the transformer copper loss can be simplified to

$$P_{\mathrm{cu}}^{\mathrm{trans}} = R_{\mathrm{DC}}^{\mathrm{pri}} I_{\mathrm{DC}}^2 + R_{\mathrm{DC}}^{\mathrm{pri}} F_{\mathrm{r}}^{\mathrm{pri}}(f_{\mathrm{s}}) I_{\mathrm{lk1,rms}}^2 + R_{\mathrm{DC}}^{\mathrm{sec}} F_{\mathrm{r}}^{\mathrm{sec}}(f_{\mathrm{s}}) I_{\mathrm{lk2,rms}}^2. \tag{5.12}$$

Therefore, if the products of $F_{\mathrm{r}}^{\mathrm{pri}}(f_{\mathrm{s}}) I_{\mathrm{lk1,rms}}^2$ and $F_{\mathrm{r}}^{\mathrm{sec}}(f_{\mathrm{s}}) I_{\mathrm{lk2,rms}}^2$ are decreasing with the operating frequency, the transformer copper loss will be lower if the operating frequency is higher. It can

be seen from Eqs. (3.23), (3.24), (4.23) and (4.24) that the RMS currents of the leakage inductors are proportional to the switching period $T$ and inversely proportional to the switching frequency $f_s$ given an operating condition. The Fig. 5.7 shows the per-unit change of the products of

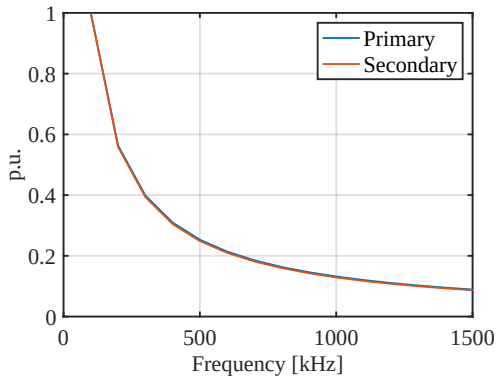



Figure 5.7: The p.u. changes of products $F_r^{pri}(f_s)I_{lk1,rms}^2$ and $F_r^{sec}(f_s)I_{lk1,rms}^2$ as switching frequency increases for the cored transformer designed in Chapter 3

$F_r^{pri}(f_s)I_{lk1,rms}^2$ and $F_r^{sec}(f_s)I_{lk2,rms}^2$ as the switching frequency increases. It suggests that the overall conduction loss of the transformer significantly decreases as the switching frequency ascends.

### Core loss

The core loss is a function of switching frequency and the peak flux density swing according to Steinmetz equation in Eq. (3.48). For a given transformer design, the flux density is then dependent on the operating frequency based on the Faraday's Law in Eq. (3.35). Therefore, the core loss at different frequencies of the proposed cored transformer design in Chapter 3 can be calculated and plotted in Fig. 5.8. It shows that the core loss increases as the frequency rises up. The core loss however is relatively negligible compared with the conduction losses. This can be explained by the fact that the voltage which introduces the flux density swing is as low as a cell's voltage. As a result, the core loss for the proposed transformer or low voltage transformer in general can be approximated independent of the operating frequency. On the other hand, the coreless transformers inherently have no core losses. Therefore, varying frequency will not introduce extra core losses on the transformer.

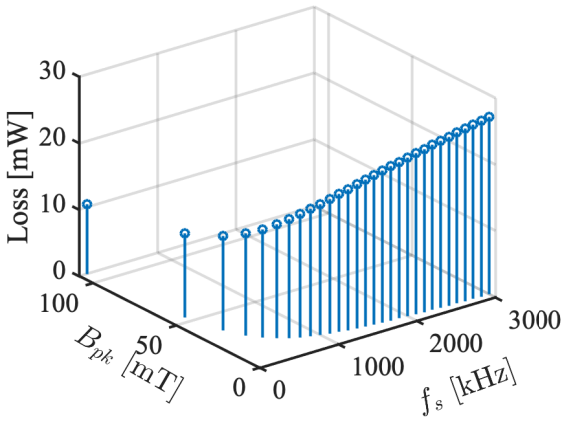



Figure 5.8: The core loss varying with frequency

### 5.2.2 Power switches

The losses of the power switches consist of the conduction losses due to the resistance when it is turned on, and the switching loss during the switching transient.

#### Conduction loss

Similar with the analysis conducted in Section 5.2.1, the conduction loss of the power switches is calculated by

$$P_{\text{cu}}^{\text{MOS}} = R_{\text{ds,on}} \left( n_{\text{HB}}^{\text{pri}} I_{\text{lk1,rms}}^2 + n_{\text{HB}}^{\text{sec}} I_{\text{lk2,rms}}^2 \right) \tag{5.13}$$

where, $R_{\text{ds,on}}$ is the turn-on resistance of the power MOSFET. Assuming the switches are identical on both primary and secondary sides, the resistances are the same. Otherwise, each MOSFET's on-resistance should be substituted. The numbers of half-bridge on primary and secondary side are denoted as $n_{\text{HB}}^{\text{pri}}$ and $n_{\text{HB}}^{\text{sec}}$, respectively. For example, for the HFB configuration, $n_{\text{HB}}^{\text{pri}} = 1$ and $n_{\text{HB}}^{\text{sec}} = 2$. As the frequency increases, the leakage inductor RMS current decreases according to the previous analysis, leading to less MOSFET conduction loss.

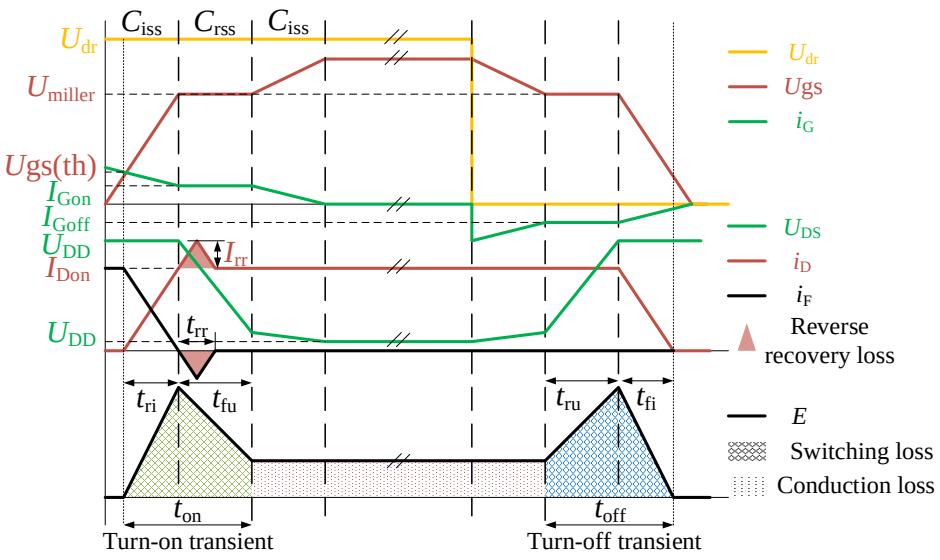



Figure 5.9: The switching transient of a MOSFET

**Switching loss**

The switching transient of the MOSFET can be plotted in Fig. 5.9. The switching loss consists of turn-on loss of MOSFET $P_{on}^{MOS}$, turn-off loss of MOSFET $P_{off}^{MOS}$, diode reverse recovery loss $P_{rr}^{Diode}$ and driver loss $P_{dr}^{MOS}$, i.e.

$$P_{sw}^{MOS} = P_{on}^{MOS} + P_{off}^{MOS} + P_{rr}^{Diode} + P_{dr}^{MOS} \tag{5.14}$$

They can be calculated by [47], [98]

$$P_{on}^{MOS} = \left(f I_{Don}\right)\left(U_{DD}\frac{t_{ri}+t_{fu}}{2}\right), \tag{5.15}$$

$$P_{off}^{MOS} = \left(f I_{Doff}\right)\left(U_{DD}\frac{t_{ru}+t_{fi}}{2}\right), \tag{5.16}$$

where the rising times of the switch voltage and current are denoted as $t_{ru}$ and $t_{ri}$. Similarly, the falling times of the switch voltage and current are $t_{fu}$ and $t_{fi}$. Those time characteristics are mainly dependent on the switching voltage and the intrinsic properties of the switch device, such as gate threshold voltage and gate charges [47]. As long as the switching voltage maintains the same

level, the rising and falling characteristics are expected to be roughly constant with the varying frequency.

The previous analysis has shown that the currents on primary and secondary sides are inversely proportional to the operating frequency as shown in Eqs. (4.20) and (5.7). That is,

$$I_{\text{Don}}^{\text{pri}} = \frac{I_{\text{ZVS}}^{\text{pri}} - I_{\text{DC}}}{2} \propto \frac{1}{f}, \tag{5.17}$$

$$I_{\text{Don}}^{\text{sec}} = \frac{I_{\text{ZVS}}^{\text{sec}}}{2} \propto \frac{1}{f}. \tag{5.18}$$

Substituting the equations in Eqs. (5.15) and (5.16) yields the MOSFETs turn-on and turn-off losses that are independent on the switching frequency. They can be approximated as constant if the rising and falling timing characteristics stay stable across the operating frequencies. Therefore, only two losses that increase with the increasing switching frequency are the reverse recovery power loss $P_{\text{rr}}^{\text{Diode}}$ and gate driver loss $P_{\text{dr}}^{\text{MOS}}$. In particular, eGaN semiconductors do not have body diodes therefore there are no reverse recovery losses. The reverse conduction capability is achieved by a different mechanism in eGaN devices [99]. On the other hand, the gate driver loss is relatively low compared with other losses. For example, the estimated gate driver loss using a commercially available GaN/SiC gate driver IC LM5113 is around 0.092 W for 100 kHz operation and 0.92 W for 1 MHz operation with a 1000 pF capacitive load and a 10 nC gate charge [100]. The reverse recovery power loss $P_{\text{rr}}^{\text{Diode}}$ and gate driver loss $P_{\text{dr}}^{\text{MOS}}$ are considered negligible [73]. Therefore, the overall trend of the total power loss as switching frequency increases is diminishing. The change of each loss component with respect to increasing operating frequency is summarized in Table 5.2

Table 5.2: The effect of varying frequency on losses

| **Loss** | **Operating frequency** | **Changing direction** |
|---|---|---|
| Transformer Cu | ↑ | ↓ |
| Transformer Core | | → |
| MOSFET Cu | | ↓ |
| MOSFET switching | | → |

## 5.3 The power per ampere criteria

Based on the previous analysis, the total loss of the system can be approximated to decrease as the frequency increases. In particular, the leakage inductor RMS currents determines the conduction loss that is a major part of the total loss [73]. Therefore, given a certain output power level, the operating condition resulting in the minimum RMS current theoretically will lead to the lowest total loss in the system. A simple mathematical expression can summarize this statement. That is,

$$MPPA(\phi) = \max(PPA(\phi)) = \max\left(\frac{P_{\mathrm{o}}(\phi, f_{\mathrm{s}})}{\sqrt{I^2_{\mathrm{lk1,rms}}(\phi, f_{\mathrm{s}}) + I^2_{\mathrm{lk2,rms}}(\phi, f_{\mathrm{s}})}}\right) \tag{5.19}$$

$$\text{where, } \phi = [d, V_1, V_2, V_{\mathrm{o}}]$$

where $PPA(\phi)$ is the equation describing the ratio between output power and total RMS current and named as power per ampere (PPA) in this study. It can be seen that PPA increases with higher output power and lower total RMS current, which is consistent with minimizing the total RMS current to improve the system efficiency. Since Eq. (5.19) attempts to maximize the output power over the total RMS current, this method is named as maximum power per ampere. For a given operating condition, e.g. cell voltages and switching frequency, the Eq. (5.19) tries to locate the phase shift $d$ that achieves the largest PPA ratio, at which the system should operate with the minimum conduction loss at a given power level.

### 5.3.1 Switching frequency independence

After substituting the output power and RMS current equations from Eqs. (4.32) and (4.23) and (4.24), the detailed expression of the PPA function can be obtained. Then the MPPA point is located by a non-linear optimization algorithm. Finding the maximum of a positive function is equivalent to find the maximum of the squared of the function. Therefore, in order to simplify the

expression of PPA, the squared PPA is computed instead.

$$PPA^2(\phi) = V_o^2 \frac{\underbrace{\frac{k^2\left[\alpha_3^{PPA}d^2 + \alpha_2^{PPA}d + \alpha_1^{PPA}\right]^2}{\beta_4^{PPA}d^3 + \beta_3^{PPA}d^2 + \beta_2^{PPA}d + \beta_1^{PPA}}}_{I_o^2}}{I_{lk1,rms}^2(\phi, f_s) + I_{lk2,rms}^2(\phi, f_s)} \tag{5.20}$$

where

$$\alpha_3^{PPA} = (V_1 + V_2)^2 \tag{5.21a}$$

$$\alpha_2^{PPA} = -2V_2^2 - 2V_1V_2 \tag{5.21b}$$

$$\alpha_1^{PPA} = V_2^2 - V_1V_2 \tag{5.21c}$$

$$\beta_4^{PPA} = \frac{-5V_o k}{196a}\left(V_1^3 + 3V_1^2V_2 + 3V_1V_2^2 + V_2^3\right) \tag{5.21d}$$

$$\beta_3^{PPA} = \frac{15V_o k}{196a}\left(V_1^2V_2 + 2V_1V_2^2 + V_2^3\right) \tag{5.21e}$$

$$\beta_2^{PPA} = \frac{15V_o k}{196a}\left(V_1^2V_2 - V_2^3\right) \tag{5.21f}$$

$$\begin{aligned}\beta_1^{PPA} =& \frac{V_o k}{196a^2}\left(V_o k V_1^2 - 15aV_1V_2^2 + 2V_o k V_1V_2 + 5aV_2^3 + V_o k V_2^2\right) \\ &+ \frac{V_1^2V_2^2a^2 + V_o^2(V_1 + V_2)^2}{196a^2}\end{aligned} \tag{5.21g}$$

It should be noted that the Eq. (5.20) is independent on the operating frequency. Therefore, the MPPA points will not vary with the changing operating frequency. This is a critical property of the proposed MPPA so that the frequency is not coupled with the phase shift as the conventional VFM, which simplifies the control logic.

### 5.3.2 Cell voltage dependence

Instead, the MPPA points only rely on the operating conditions, such as the cell voltages and phase shift. The cell voltages can be approximated as constant during one switching period and are measurable parameters in Eq. (5.20). It is thus arranged as an expression of phase shift only.

As a result, the MPPA point at given cell voltages are only determined by the phase shift $d$.

## 5.4 The solution for the MPPA optimization

Provided the operating conditions, the MPPA points can be solved based on Eq. (5.20). However, the equation is significantly non-linear, leading to online optimization infeasible due to the computational constrains on the embedded systems, even though it provides the most accurate MPPA phase shift. Implementing this full-order on the embedded systems can only achieved by pre-loaded LUTs. Nevertheless, the LUT is also constrained by the resolution and may introduce undesired error due to the interpolation between sampled points. The approximations to Eq. (5.20) can be applied in order to implement the online calculation of MPPA without drastically sacrificing the accuracy.

### 5.4.1 Full-order system

The non-linear optimization algorithm, such as sequential quadratic programming, can be applied to locate the phase shifts where the MPPA achieves using Eq. (5.20) to generate the pre-calculated phase shift LUT for online implementation. As an example, a MPPA phase shift plot

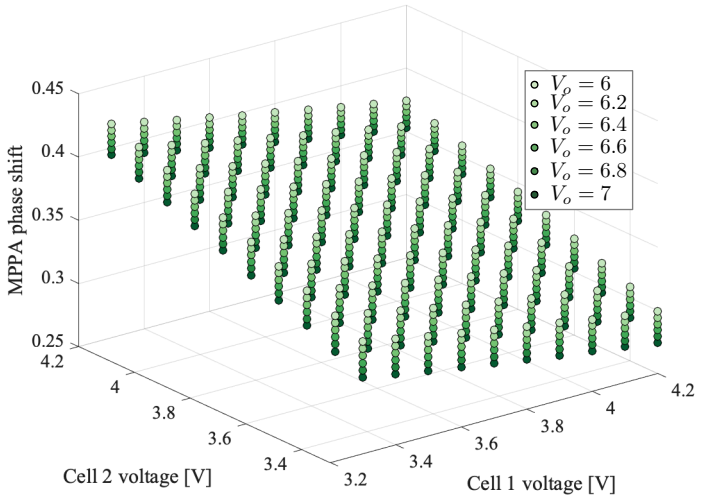



Figure 5.10: The MPPA phase shift with different combinations of cell voltages

is shown in Fig. 5.10 based on the coreless transformer designed in previous chapter and the circuit parameters specified in Table. 5.1. However, other transformer designs can be substituted to obtain the MPPA phase shifts at different voltage combinations. It can be seen from the plot that the MPPA phase shift varies with the cell voltages and LV/output capacitor voltage. The MPPA phase shift is minimum when cell 1 is at the maximum voltage while the cell 2 is at the lowest one. This can be explained by the shifted peak power if the cells are out of balance, as shown in Fig. 4.17. The peak power is achieved at smaller phase shift when $V_{\text{cell1}} > V_{\text{cell2}}$ and vice versa. So this MPPA map can be extracted as a LUT to find the desired phase shift when the cell voltages are measured.

### 5.4.2 Reduced-order systems for computation-restrained environments

The reduced-order PPA expression can be obtained by applying Taylor Series Expansion at a quiescent operating condition, whose maximum can be computed in the real-time controllers.

#### 1st-order Taylor Series Expansion

The first-order Taylor approximation is applied on Eq. (5.20) at the nominal condition where $\phi_{\text{q}} = [0.25, 3.6, 3.6, 6.5]$. The resulting expression is

$$PPA^{1st}(\phi_{\text{q}}) = 0.0612V_1 - 0.123V_2 + 0.22V_{\text{o}} + 1.33d - 0.332. \tag{5.22}$$

Then a partial derivative can be applied to it to locate the phase shifts where MPPA is achieved. Since this is a first-order approximation, the linear relationship constantly generates the MPPA phase shift at its maximum 0.5. The MPPA phase shift difference between the full-order model and first-order one is plotted in Fig 5.11. The errors are not negligible especially at extreme conditions. Therefore, it is not practical to implement due to its high error.

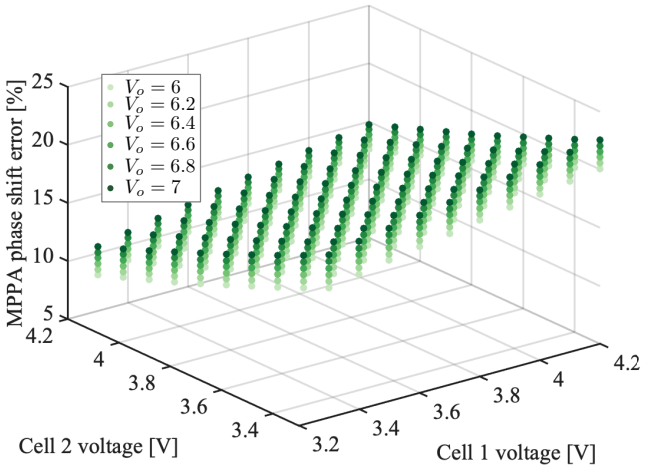



Figure 5.11: The MPPA phase shift error between 1st-order model and full-order one

### 2nd-order Taylor Series Expansion

In order to overcome the drawback of the first-order approximation, the second-order Taylor Series Expansion can be applied on the full-order model. Firstly, the MPPA is expanded at the same quiescent point $\phi_{\mathrm{q}}$ and the MPPA phase shift error is plotted in Fig. 5.12(a). It shows that

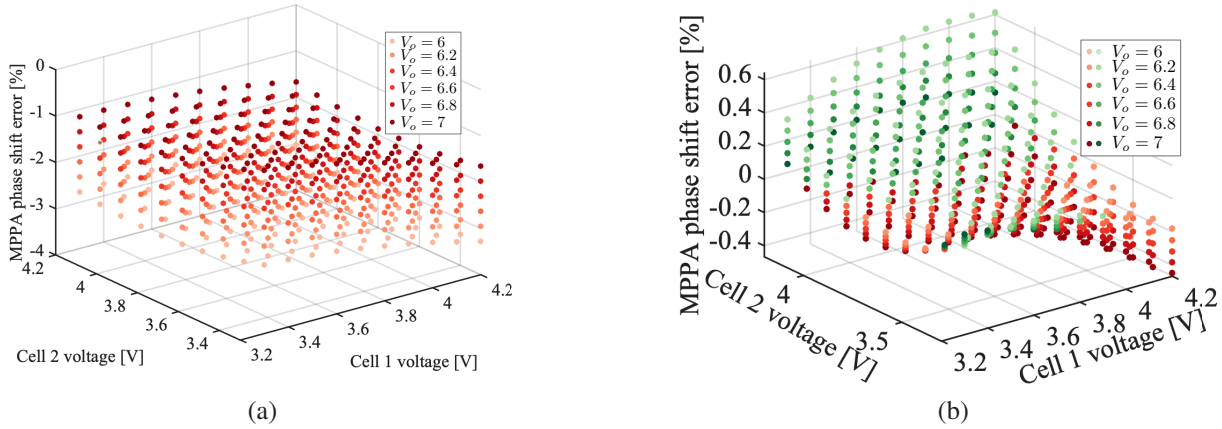



Figure 5.12: The MPPA phase shift error between 2nd-order model and full-order one expanded at (a) $d$ = 0.25 and (b) $d$ = 0.35

the second-order model constantly underestimate the MPPA phase shift but provides significantly more accurate results than first-order model. The model can be further improved by adjusting the quiescent point where it is expanded as the MPPA phase shift points locate around 0.35 based

on the full-order model in Fig. 5.10. Therefore, an updated quiescent point can be chosen as $\phi'_{\mathrm{q}} = [0.35, 3.6, 3.6, 6.5]$ to expand the full-order system, as shown in Eq. (5.23). The error between the updated second-order model and the full-order model is given in Fig. 5.12(b). It is more accurate than previous model.

$$\begin{aligned} PPA^{2nd}(\phi'_{\mathrm{q}}) = &- 0.0119V_1^2 - 0.0489V_2^2 + 0.00299V_{\mathrm{o}}^2 - 5.31d^2 \\ &+ 0.051V_1V_2 - 0.0151V_1V_{\mathrm{o}} - 0.486V_1d + 0.0259V_2V_{\mathrm{o}} + 0.987V_2d \\ &- 0.299V_{\mathrm{o}}d + 0.161V_1 - 0.0259V_2 + 0.299V_{\mathrm{o}} + 3.71d - 0.65 \end{aligned} \tag{5.23}$$

The maximum is located where derivative of Eq. (5.23) with respective to $d$ equals 0, i.e.

$$\frac{d(PPA^{2nd})}{d(d)} = 0 \tag{5.24}$$

$$\Rightarrow d_{\mathrm{MPPA}}^{2nd} = 0.0931V_2 - 0.0458V_1 - 0.0278V_{\mathrm{o}} + 0.35. \tag{5.25}$$

This form can be directly implemented in the real-time controller without putting much computational burden on it.

**Higher-order Taylor Series Expansion**

Even though the second-order model is sufficiently accurate, it is still worth to explore how much improvement the higher-order models could bring. A fourth-order Taylor Series Expansion is performed at $\phi_{\mathrm{q}}$ and the MPPA phase shift error is plotted in Fig. 5.13. It shows the error is comparably small as the second-order model in Eq. (5.23). However, the higher complexity it introduces makes implementing it on the embedded systems infeasible.

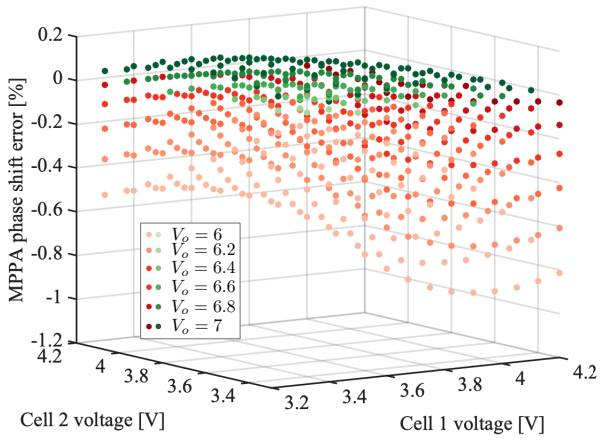



Figure 5.13: The MPPA phase shift error between 4th-order model and full-order one

## 5.5 MPPA-based variable frequency modulation

### 5.5.1 Proposed methodology

It has been shown that the MPPA is only dependent on the cell voltages and phase shift, regardless of the operating frequency. The phase shift generated from MPPA guarantees the maximum RMS utilization rate and thus, the minimized conduction loss are obtained at the MPPA operating point. However, if the frequency is introduced as a variable, the conduction loss due to the RMS currents can be also reduced with a higher operating frequency shown in Eqs. (4.23) and (4.24) as they are inversely proportional to the operating frequency $f$. If the switching loss stays relatively constant as analyzed in the previous section, the total loss of the system largely relies on the conduction loss. Therefore, the VFM algorithm can be simplified to directly adjusting the frequency to satisfy the requirement of the output power given an operating phase shift defined by MPPA. The control architecture for the conventional critical VFM and the direct MPPA-based VFM are plotted Fig. 5.14. The operating frequency is controlled based on the resulting output power $P_{\mathrm{o}}$. When the output power is lower than the reference, the frequency slightly drops to accommodate the error, and vice versa. Note that the operating frequency should be bounded by upper and lower limits beyond which the semiconductor devices might be damaged. On the other hand, the conventional critical VFM is shown in Fig. 5.14(b). It can be seen that the 4D-LUT is applied to obtain the

operating variables $d$ and $f$ and it is operated in an open-loop fashion. Therefore, any disturbance from the modeling would affect the final outcome.

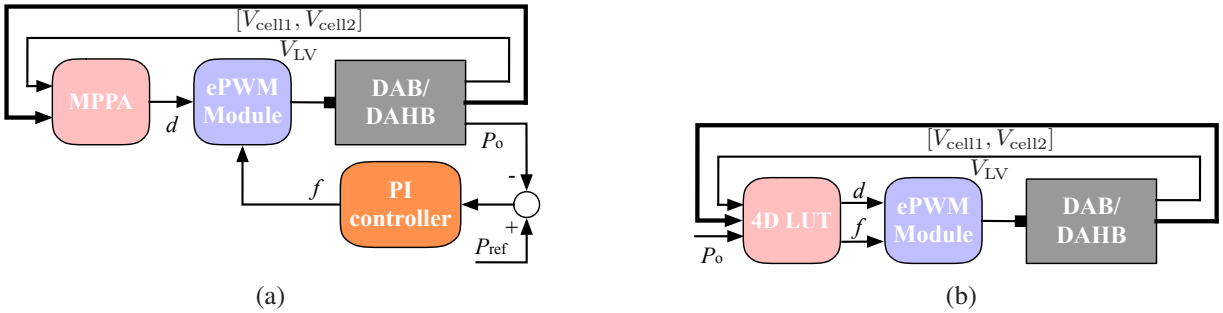



Figure 5.14: The control architecture with (a) direct MPPA-based VFM (b) conventional critical VFM

Since the MPPA suggests the operating phase shifts are at most around 45% at extreme conditions, as shown in Fig. 5.10, the full power capability is not utilized as a result of the phase shift modulation that is less than 50%. Therefore, frequency needs to be reduced in order to achieve the peak power with the MPPA enabled.

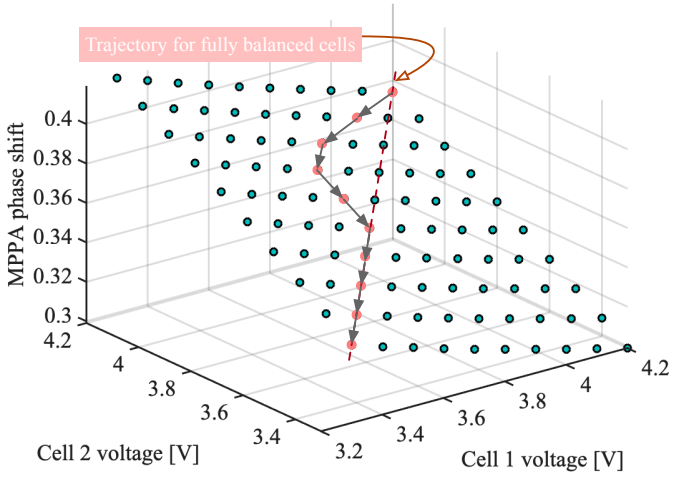



Figure 5.15: The example trajectory of MPPA phase shift as the cells discharge from full

An example of the trajectory that MPPA phase shift would follow when the cells discharge from fully charged is given in Fig. 5.15. It is assumed that the two cells in one link are both at full charge, i.e. 4.2 V. Due to the nonidentical capacities or internal impedances, the voltages of the cells start to deviate from the trajectory of the cells with exactly identical voltages as they

discharge. As a result, the MPPA phase shift is adjusted to the optimal points based on the cell voltages for a period of time. Once the cells voltages are corrected by the balancing mechanism, the diagonal MPPA trajectory is resumed until the batteries are below the minimum voltage where the rated power is provided or the voltages are unbalanced again. Note that the switching frequency is also varying to guarantee the output power capability.

### 5.5.2 Comparison with traditional VFM

The critical soft-switching commonly solves for the phase shift and switching frequency that allow the soft switching with a boundary condition where the current at the switching instance satisfies the ZVS requirement. The Fig. 5.16 shows the phase shifts generated from traditional VFM with a 0.5 A ZVS current requirement are smaller than the ones produced by MPPA. The ZVS requirement on the secondary leakage inductor current is obtained based on the parasitic parameters of the GaN MOSFETs.

Given the parasitic capacitance is 1450 pF for EPC 2021 [101], the required ZVS current for a dead time of 70 ns is 0.5 A based on Eq. (5.4), where 70 ns is 3.5% of the period of 500 kHz switching. The same analysis can also be applied to the switching process when $S_1'$ is turned off and $S_2'$ is turned on, which yields the same results because of the circuit's symmetry. It is noted that the required ZVS current may vary based on the different parasitic values, but for a low-voltage and fast MOSFETs the ZVS current is expected to be similar.

The calculated phase shifts based on the traditional VFM are worst-condition values which are obtained at maximum operating frequency, as higher phase shift is required to achieve soft switching at higher frequency, as explained by Eq. (5.7). The dependency of the phase shift on the switching frequency is given in Fig. 5.17. At minimum frequency 100 kHz, the required phase shift to achieve ZVS current is roughly 6% less than the one at maximum frequency 1 MHz. Therefore, the phase shifts that are optimized by MPPA criteria equivalently increases the soft switching capability, which in turn makes the statement rigorous that switching loss is relatively constant over a wide frequency range as explained in previous section. The secondary inductor

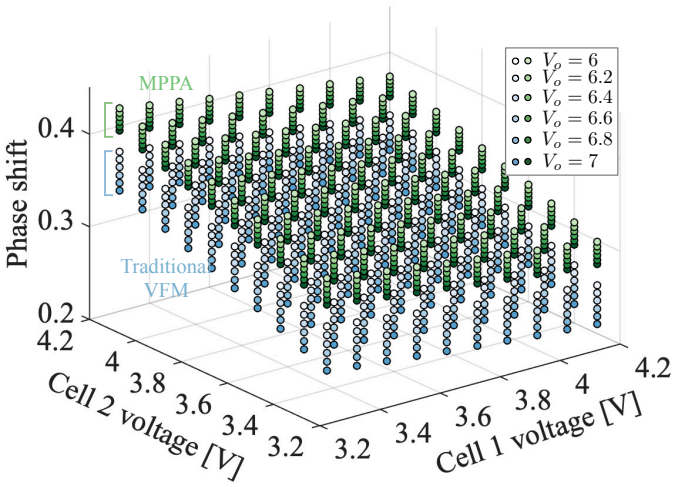



Figure 5.16: The operating phase shifts generated from the MPPA and the critical soft switching

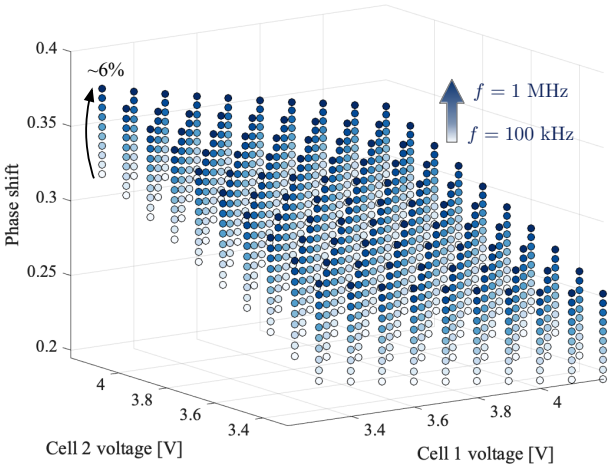



Figure 5.17: The operating phase shifts generated from the critical soft switching at different switching frequencies

current waveforms generated from MPPA and VFM are given in Fig. 5.18. It can be seen that MPPA ensures higher current at the commutation point while increasing the output power.

On the other hand, the PPA at that point generated by the critical soft-switching is not often maximized, leading to higher conduction losses. It can be also seen from Fig. 5.16 that applying MPPA not only reduces the conduction losses at the given operating frequency but also ensures the ZVS.

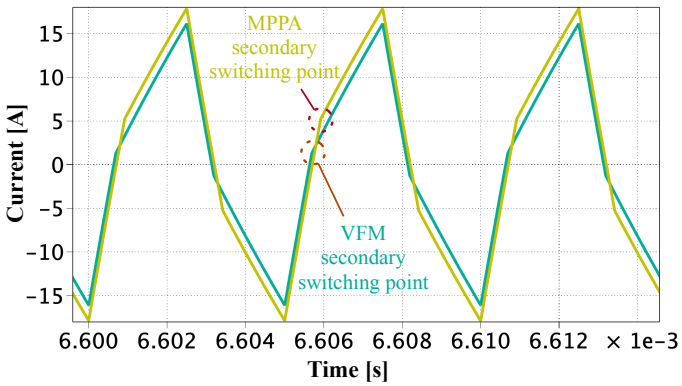



Figure 5.18: The waveform comparison between MPPA and VFM at 200 kHz

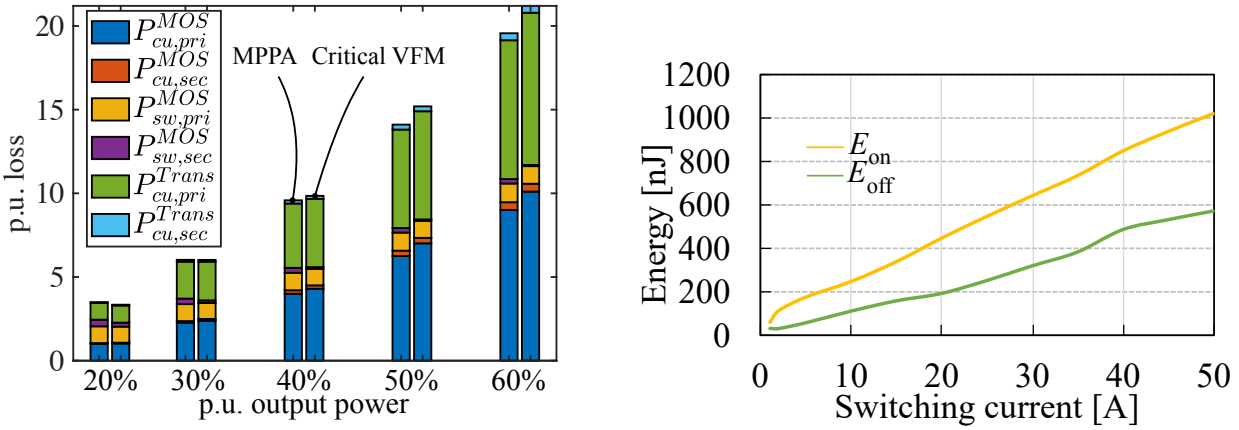
### 5.5.3 Example loss distribution for EPC 2021 and coreless transformer

An example of pu loss distributions between MPPA-VFM and critical VFM are plotted in Fig. 5.19(a). All the losses are normalized with respect to the primary-side MOSFET conduction loss at 20% output power. Only turn-off switching loss is considered in this analysis and is obtained by the double pulse test at the different switching currents from the official SPICE models of EPC 2021 [101], as shown in Fig. 5.19(b). It can be seen that, as the switching current reduces the energy is also reduced, which is consistent with the derivation in Section 5.2.2. It is assumed that the primary- and secondary-side MOSFETs are identical such that the $R_{\text{ds,on}}$ is the same for simplicity. It can be seen from the plot, the most dominant loss is the conduction losses from MOSFET and transformer. At high power load, the advantage of maximizing PPA appears, leading to lower pu loss compared with critical VFM.

## 5.6 Experimental validation

### 5.6.1 MPPA vs. actual maximum efficiency

The validation experiments are performed on the platform of the DAHB topology with the coreless transformer with the LV battery fixed at 12 V. In order for a good coverage of the most operating conditions, the representative operating points are selected. With each voltage combination, the efficiency recorded operating at MPPA phase shift is compared with the actual maximum




(a) (b)

Figure 5.19: (a) The example p.u. loss distribution between MPPA-VFM and critical VFM at different power levels; (b) The extracted switching energy from double pulse test using the SPICE model

efficiency by sweeping the entire phase shift range, as shown in Fig. 5.20. It shows that the MPPA method provides a 0.61% of average efficiency offset compared with the ground-true maximum efficiency, which is insignificant. Therefore, this method can provide the approximately maximum efficiency at a given frequency.

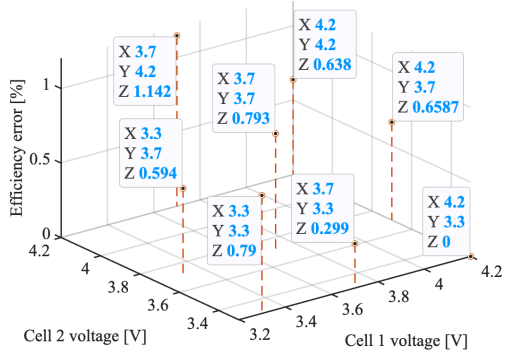



Figure 5.20: The error between ground-true maximum efficiency and MPPA efficiency

### 5.6.2 Light-load operation compared with constant frequency modulation

As the accuracy of the MPPA method is verified, the aforementioned MPPA-based VFM can be implemented following the control architecture shown in Fig. 5.14(a). A comparison among the maximum efficiencies from ground-true, MPPA-VFM and constant frequency modulation (CFM)

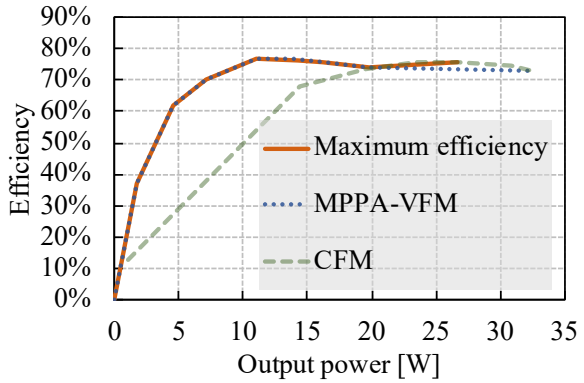



Figure 5.21: The comparison of ground-true VFM, MPPA-VFM and CFM

is illustrated in Fig. 5.21. The ground-true VFM measurements are made by finding the maximum efficiency points when sweeping the entire phase shift ranging from 0% to 50% and the frequency varying from 300 kHz to 700 kHz. The CFM is operating at 300 kHz constantly whereas the MPPA-VFM dynamically adjusts the frequency based on the required output power.

From Fig. 5.21, the results show that the CFM is inefficient at light load condition as power is mainly dissipated on the switching and conduction. Instead, the MPPA-VFM increases the frequency to decrease the RMS current and soft switch, leading to a higher efficiency when the load is low. When the load increases, the efficiencies of CFM and VFM merge since the switching frequency decreases to its minimum 300 kHz. In addition, the result also shows the high agreement between MPPA-VFM and the ground-true maximum efficiency, which proves the MPPA operates the system at its pseudo-optimal condition.

### 5.6.3 Light-load operation compared with critical soft-switching

The critical VFM is also compared with MPPA-based VFM at low load conditions with the output power between 20% - 50% of peak output power, as shown in Fig. 5.22. It shows that MPPA-based VFM improves the efficiency roughly 1% between 20 - 50% of peak load, thanks to the reduced effective power to RMS ratio. In addition to the efficiency improvements, the control logic for MPPA-VFM is significantly simplified compared with the critical VFM. The phase shift for MPPA-based VFM is kept constant over the most of the operating conditions while the critical

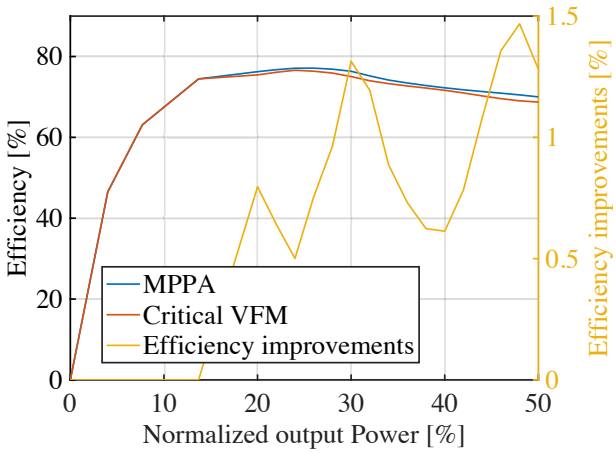



Figure 5.22: The comparison between critical VFM and MPPA-VFM at low load conditions

VFM needs to adjust the phase shift in order to achieve the required ZVS current level, as explained in section 5.5.2.

## 5.7 Conclusion

This section proposes a simplified variable frequency modulation that maximizes the effective total RMS current at a given switching frequency while maintaining soft-switching. The ratio of the output power and total RMS current flowing through the transformer is defined as power per ampere. By maximizing PPA, the RMS current maximally contributes to the actual output instead of generating losses and corresponding phase shift that achieves MPPA can be obtained. It is found that the factor PPA is independent of frequency, which makes a simplified variable frequency modulation feasible, i.e. MPPA-VFM. The output power is controlled by a PI controller regulating the frequency and the phase shift is set based on MPPA points for the given voltage measurements. In order for the real-time implementation of the MPPA calculation, the approximated MPPA expressions based on different orders of Taylor Series Expansion are given. The second-order system is concluded to be accurate and sufficiently low computational-intense, leading to a feasible real-time implementation. The MPPA operating points are also compared with the ground-true maximum efficiencies at various voltage combinations, which shows negligible offset between them. Lastly, the traditional CFM, VFM and proposed MPPA-based VFM are evaluated in terms of the efficiency

measurements. The MPPA-VFM shows similarly high efficiency compared with ground-true maximum efficiency.

# Chapter 6: Cost Analysis and Comparison with Existing Redistributive Balancer

In order to quantify the benefits of combining APM and redistributive balancing in terms of cost, this chapter estimates the distribution of the cost given the proposed topologies for both prototyping and mass production. The $-per-cell metric will be compared with commercialized BMS solutions listed in Table 2.4 and OEM on-board BMSs (especially Chevy Bolt) described in Table 2.3. Therefore, the statement that BB-APM can bring nearly complimentary distributive balancing into EV systems and accelerate the adoption of the redistributive balancing, can be quantitatively justified.

Please note that the manufacturing and assembling costs are out of the scope of this study, since it is believed that the work load of installing the proposed BB-APM should be approximately similar or less than installing BMS and APM. Installing BMS requires tooling for each battery module (paralleled connected cells) and separated labor for APM, however, the proposed BB-APM eliminated the need for configuring APM as it is integrated into the balancer. On the other hand, BB-APM monitors and regulates two battery modules at the same time instead of only one module, which translates to halved tooling/work load for installing the BMS related hardware.

## 6.1 DAHB configuration with coreless transformer

As the coreless configuration is simplified version of cored version, the cost of the coreless DAHB will be part of the HFB configuration with core and can be initially analyzed. The results of DAHB then can be modified and applied to the HFB assuming the components used in the cored-version design are identical with coreless version, except for the transformer and one extra half-bridge module.

Since the cost of mass production is not straightforward to obtain, the analysis is only based on what can be acquired from online distributors for small batch ordering. The prototyping price can also be compared with the ones of the commercial solutions listed in Table 2.4, since the evaluation cost is fairly close to prototyping. However, an appropriate extrapolation based on available information of the small-batch purchasing is applied to estimate the cost of bulk purchasing. The rule-of-thumb conversion from prototype/batch production to mass production will be provided to illustrate the cost compared to commercial and OEM solutions under consideration of mass production. The cost analysis is divided into four stages or volumes: prototype, batch production, optimized batch production as well as mass production. The definitions in this study of the four stages are given below:

- **Prototype:** proof of concept, small amount of purchased components (e.g. less than 50 units or 1 EV)
- **Batch production**: relatively large amount of purchased components after proof of concept (> 1,000 units but < 5,000 units, i.e. 200 - 1,000 EVs)
- **Optimized batch production**: updated component list considering cheaper alternatives without compromising performance, relatively large amount of purchased components (> 1,000 units but < 5,000 units, 200 - 1,000 EVs)
- **Mass production**: large quantities of standardized products, efficient production of a large number (> 5,000 units or 1,000 EVs)

The number of EVs mentioned above is determined assuming there are 96 cells/modules in the EV system to be managed.

### 6.1.1 Prototype

In the stage of prototyping, limited amount of components is purchased to validate the proposed operation. Thus, the cost of this stage is relatively high, but it is necessary for mainly proof of

concept as well as debugging and troubleshooting. Once the idea is validated, the design can be optimized for cost-oriented requirements. The price of each component in the cost estimation for prototyping is based on purchasing single unit from the distributor, which is roughly as twice as the unit price if 1000 units are purchased at one time and approximately multiple times more expensive than the price of mass production. The distribution of the cost for prototypes in terms of the function of the components is given in Fig. 6.1 to facilitate the optimization process in stage 3. By identifying the significant portion of cost from the pie chart, the relative optimization on those components can be performed to effectively reduce the cost in a targeted manner. The total cost for assembling one device is roughly $79, i.e. $39.5/cell. The decision for future improvements to reduce the cost can be summarized as sensing circuitry and passive components. Both of them take 63% of the entire cost, i.e. $49.8. However, the conclusion cannot be drawn solely by this. The cost of the batch production also needs to be analyzed, as the price of the passive components tend to drop significantly with the increased number of purchasing units.

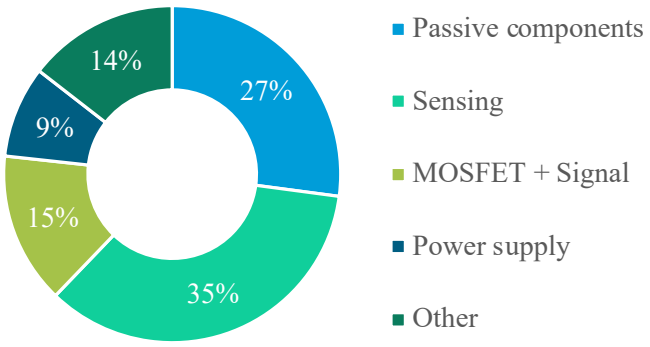



Figure 6.1: The DAHB cost breakdown of the electric components for prototyping

### 6.1.2 Batch production

Similarly, the cost breakdown can also be drawn by using the prices listed in bulk purchasing (e.g. 1000 units) from the distributors, as shown in Fig. 6.2. Both prototype and large-batch production share the similar proportions in terms of the categories of the components. However, the expense on the passive components is significantly reduced as the number of the unit increases.

As expected, for mass production, the cost for passive components would attempt to be cheaper and eventually could only posses around 10% or less of the total cost. Similarly, other components cost less as the scale of the production increases. The main cost still originates from the sensing circuitry. In particular, high-bandwidth electrically isolated current sensor posses a large portion of the sensing cost. The more cost-competitive solutions can be found to further make the BB-APM hardware accessible and cost-effective compared with the combination of BMS and APM (~ $4.2/cell). For example, the shunt-resistor and anolog-to-digital converter (ADC) can be used to replace the expensive but high-bandwidth hall-effect current sensors without sacrificing the performance of the circuitry.

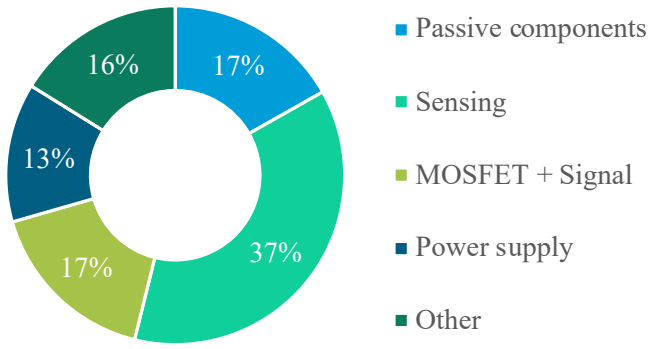



Figure 6.2: The DAHB cost breakdown of the electric components for large batch production

### 6.1.3 Optimized batch production

It is explained that the cost analysis on prototyping and batch-production projections benefits the design process achieving cost-friendly optimization. Given the distribution of the component cost in Figs. 6.1 and 6.2, the possible improvements should mainly focus on sensing. Also, the unnecessary devices for the ease of prototyping can be omitted in the optimized solution.

#### Sensing circuits

As can be seen from previous analysis, the majority of the prototype's cost is from sensing circuits. To reduce the cost without compromising too much performance, the current hall-effect

sensors can be replaced by a shunt resistor and a differential isolated ADC. An example of shunt resistor and isolated ADC is ULR1R001FLFTR and SI89xx from IRC/TT Electronics and Silicon Labs, respectively. The multi-channel ADC is preferred since the cost can be further reduced compared with single-channel version when there are more than one measurement needed.

On the other hand, the voltage sensing is realized by an isolated op-amp ACPL-C87X from Broadcom with extremely high isolation voltage (5,000 Vrms), which is acceptable for prototyping. In practice, a lower-rated alternative or an isolated ADC can also meet the isolation requirement in EV application but still deliver desired precision and lower cost. The aforementioned 3-channel isolated ADC SI89xx from Silicon Labs is also a cost-friendly solution to replace the voltage sensor at a price of 1/4 of ACPL-C87X.

**Other**

In category *other*, the pin headers and terminals are taken into account. But in batch/mass production, the terminals can be replaced by DC bus or pads, which is nearly free. On the other hand, the pin headers will be removed as the microcontrollers will be integrated on the modules instead of discrete which was originally designed purposely for the ease of debugging. Therefore, little effect will be observed to eliminate the cost under category *other* from the optimized batch production.

**Updated cost distribution**

After making modifications to the prototype based on previous analysis, the cost can be cut down to roughly $11/cell for small-batch production. The breakdown of the optimized batch production cost is illustrated in Fig. 6.3. In the updated design, the cost is roughly evenly-distributed among the various of components.

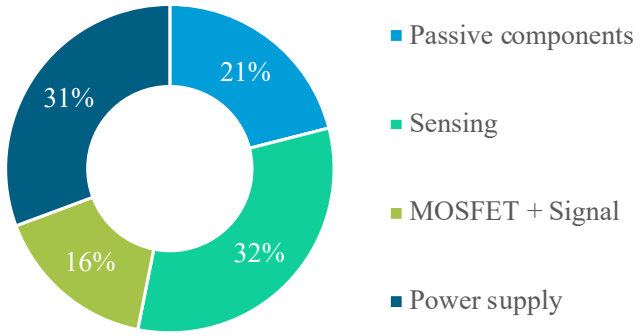



Figure 6.3: The DAHB cost breakdown for optimized batch production

### 6.1.4 Comparison between prototype and batch production

The cost comparison among the prototyping design with small and large amount of components purchased and optimized design is given in Fig. 6.4. By converting prototype to batch production, the cost is shrunk by more than 50% due to the significantly reduced component costs that are dependent on purchasing quantity. Furthermore, the cost of the optimized version is at around $4/cell, roughly 30% cost of the non-optimized design. Therefore, it can be seen that the cost can be brought down to a reasonable range after turning prototype into batch production and a certain level of optimizing on component selection. Note that the price is based on the lowest price that are available online for the selected components, e.g. the price when purchasing 5,000 units. It is believed that the unit price can be even lower with higher-volume purchasing.

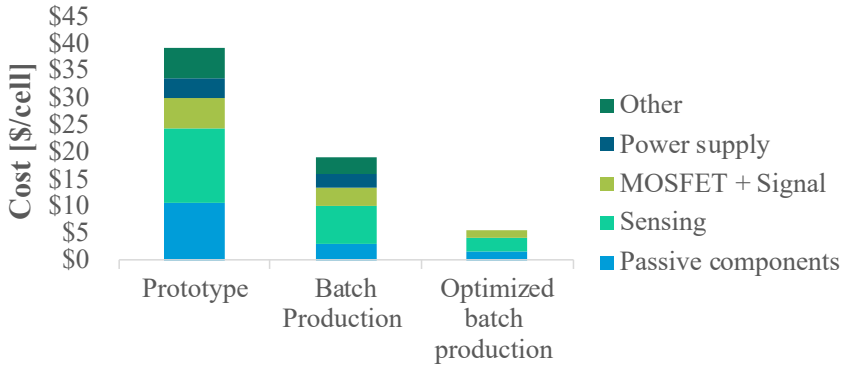



Figure 6.4: The DAHB cost comparison between prototype and batch production in terms of component category

### 6.1.5 Cost projection for mass production

Due to the limited information that is available online, the approximated cost for mass production requires some rule-of-thumb extrapolation. The production cost is known to exponentially decrease as the production volume increases [102]. Therefore, the production cost under mass production can be approximated by extrapolating the existing trend to tens of thousand up to million units by exponential function. The relationship between cost and production volume in terms of the number of EVs sold is illustrated in Fig. 6.5. The assumption in this figure is that each EV equips 96 cells or modules in series connection, which is a common configuration in commercial EVs such as Chevy Bolt [39] and Tesla Model S [103]. Therefore, BB-APMs are installed on every two cells/modules. The required number of BB-APM for one EV is thus 48 and approximated to be 50 for the ease of data representation. Correspondingly, the number of components is also scaled up to a one-EV basis. The cost of optimized batch production is initially plotted to extract

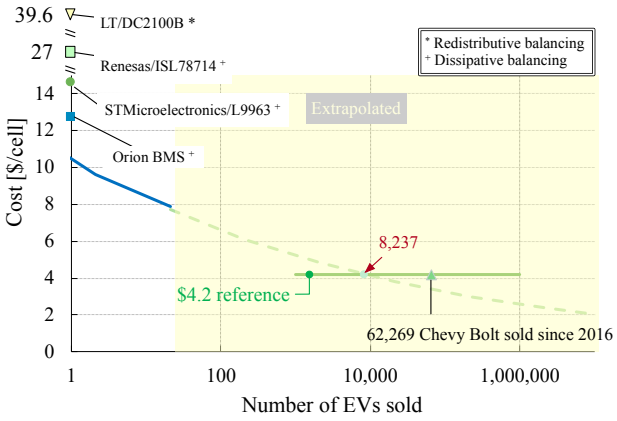



Figure 6.5: The production cost vs. number of EVs sold for the DAHB configuration

the parameters fitting the curve. Given the trend of existing cost curve, the result with larger production volume are approximated in the extrapolated area. With the number of the EV equipped with BB-APM reaching 8,237, it is not unlikely that the redistributive balancing becomes completely free of charge if the proposed topology were implemented in Chevy Bolt, as the state-of-art BMS + APM cost ~$4.2/cell according to Table 2.3. The 'break-even' point of 8,237 EVs sold is roughly 13% of the total market sales of Chevy Bolt since 2016.

It can also be observed that the optimized batch production is caught up by normal batch production at higher production volume, which is the result of the lack of cost information for cost-friendly sensing replacements when buying large amount. The author assumed the price is the same when buying 1000 and 1,000,000 sensing alternatives, even though it is not practically reasonable. Instead, it is expected that the optimized batch production would break even relatively sooner than the batch production without substituting sensing circuits if the price information for mass production is provided.

Nevertheless, the statement that the cost of the proposed concept is comparable with the cost of the combined but discrete APM and BMS system, is justified to a significant extent due to limited resources. It shows the proposed BB-APM has great potential of achieving redistributive balancing without extra cost, which is normally considered cost-unfriendly in OEMs.

## 6.2 Cost comparison with HFB and DAB

Given the analysis of the coreless version, the HFB variant is then analyzed by adding the cost of extra half-bridge module and the transformer. Similar with coreless DAHB, the evaluation of the cost for prototype, batch production and optimized batch production is given in Fig. 6.6. The extra cost is from the core material and another half-bridge module, which is around 10% of the entire prototype cost. As the production volume increases, the extent of the cost reduction for most components is high compared with the core material. Therefore, the cost percentage of the extra core material and half-bridge module still retains high for batch production. The cost breakdown analysis for the optimized batch production is drawn in Fig. 6.7. It can be seen that the extra cost due to the transformer core and additional half-bridge module is 18% of the total cost. Therefore, by turning the design into coreless and half-bridge configuration, the cost is reduced relatively significant. In addition, it is excluding the extra assembly cost due to the complex procedure of installing the cored transformer.

The same extrapolate technique is applied to the costs of HFB and DAB with cored transformer to see the cost comparison among DAB, HFB and DAHB, as shown in Fig. 6.8. It is assumed that

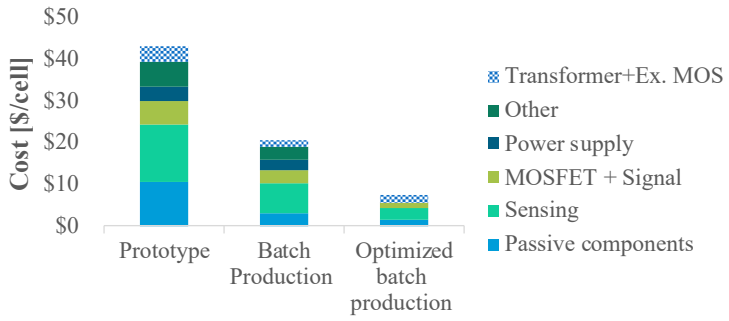



Figure 6.6: The cost comparison between prototype and batch production in terms of component category

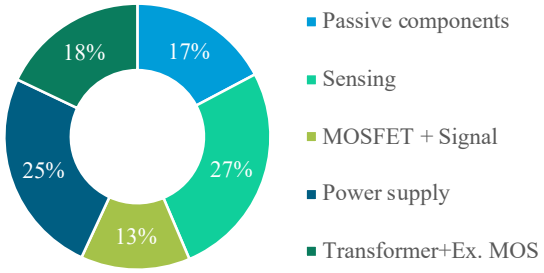



Figure 6.7: The HFB cost breakdown for optimized batch production for HFB

the transformer and MOSFETs used in DAB are identical to HFB and DAHB variants. It can be clearly seen that the cost of the DAB is almost as twice as the one of HFB as each DAB converter with 8 MOSFETs and 1 transformer can only manage one cell compared with the HFB equipping 6 MOSFETs and 1 transformer for 2 cells. On the other hand, DAHB even outperform the HFB due to the reduced number of MOSFETs and removal of the core, curtailing at least 15% cost before reaching 10,000 vehicles sold.

The DAB approaches the $4.2/cell budge with more than 1 million vehicle sold, which is hardly achievable for EVs currently. However, the redistributive balancing becomes complimentary if the proposed DAHB is adopted when 8,237 vehicles sold. It is more reasonable number for most of the OEMs. Even though the numbers are estimated, the author expects the cost would drop more significantly as most of the prices are extrapolated with no accurate price information. The HFB variant reaches requirement of $4.2/cell when around 50,000 vehicles are produced.

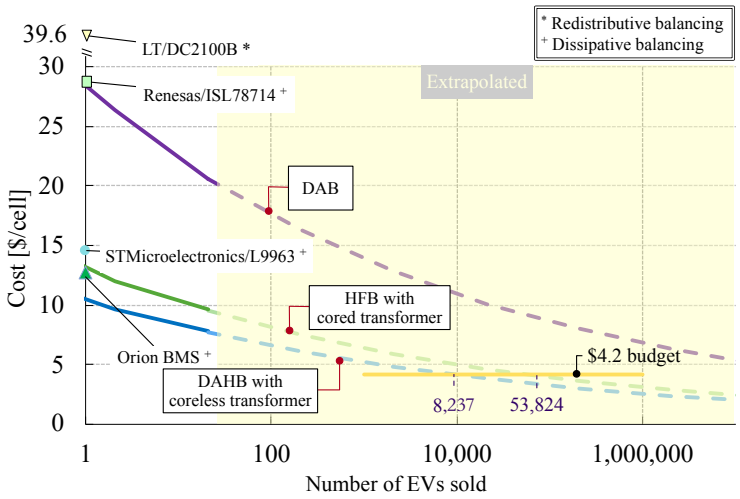



Figure 6.8: The cost difference among the HFB with core, coreless DAHB and the DAB configurations

## 6.3 Comparison with existing modular balancing approaches

As the modular design attracts more attention in battery balancing territory, there have been many researches discussed previously that utilize the modular design concept [17], [23], [24]. It would be beneficial to compare them with the proposed topology to highlight the features of proposed topology. The comparison for a battery system with 2n cells is listed in Table 6.1 in terms of components count, available balancing mode, balancing speed, converter efficiency, targeting power level and switching frequency. The balancing speed is concluded using the metrics proposed in [10]. Please note that the comparison between proposed topology and the counterparts that interact with HV-bus is pointless. The power loss is from 4.2 kW up to 26.6 kW for the HV-bus balancing topologies like the one proposed in [23], whereas the proposed topology only loses from

Table 6.1: Comparison among modular battery balancing topologies for a battery system with 2n cells

| Topology (MOSFET technology) | Components* | Balancing modes | Balancing Speed | Efficiency | Required power level | Switching frequency |
|---|---|---|---|---|---|---|
| Proposed DAHB (Si) | $4n/0$ | C2C + C2LV + LV2C | Fast (< 1)$^{+}$ | 80%$^{\#}$ | 2.4 kW | 200 kHz - 1 MHz |
| Proposed HFB (GaN) [86] | $6n/n$ | C2C + C2LV + LV2C | Fast (< 1)$^{+}$ | 86% | 2.4 kW | 200kHz - 1 MHz |
| DAB (Si) [17] | $16n/2n$ | C2LV + LV2C | Relatively fast (< 1)$^{+}$ | 92% | 1.2 kW | 200kHz |
| Inductive (N/A) [24] | $2n/2n$ | C2C | Slow (> 20)$^{+}$ | 86% | 0.5 - 2 KW | 100kHz |
| Buck-boost (Si) [23] | $4n/2n$ | C2HV+ HV2C | Relatively fast (< 1)$^{+}$ | 93% | 60 - 380 kW (HV bus) | 250kHz |

*Number of power switches/ferromagnetic cores

+Number of hours to balance for a 100-cell pack under same condition [10]

#The efficiency can be improved by utilizing MOSFETs with lower $R_{ds,on}$, refer to Appendix B

228 W to 456 W because of its lower power rating, assuming constant efficiency across the entire operation range. The benefits gained from redistributive balancing are reduced or even canceled out due to the additional power loss for HV-bus based balancing topologies.

In Table 6.1, it can be seen that the proposed topology outperforms the other counterparts in: (i) balancing speed: as the extra C2C path in addition to C2LV takes less time to balance same SOC difference compared with C2LV/HV-only techniques as shown in experimental validation; (ii) switching frequency: steps towards integration and higher power density; (iii) total power losses: it is significantly smaller compared with the series modular design that is directly connected to HV bus [23]. Besides, the proposed HFB have significantly less component count compared with DAB counterpart and is comparable with the other two topologies. Furthermore, DAHB reduces the MOSFET count by 50% compared with HFB and eliminates magnetic core while maintaining all balancing modes.

## 6.4 Conclusion

The detailed cost analysis is performed on the proposed HFB and DAHB. The DAB topology from the existing literature [17] is also included as a reference. Based on the cost breakdown of each function type, the alternative components for optimized cost are proposed with the negligible sacrifice on the accuracy, which yields an optimized cost for batch or mass producing.

The costs of three systems are estimated and projected to high-volume production based on available information from the large distributors. The results show the existing DAB is infeasible to achieve $4.2-budge within a reasonable number of EVs manufactured. However, the proposed HFB and DAHB topologies become complementary when 53,824 and 8,237 vehicles sold, respectively. Therefore, the proposed topologies are relatively cost-friendly with small batch production and become free of charge for higher-volume production, which could potentially accelerate the adoption of redistributive balancing. The proposed topologies are also compared with state-of-art redistributive balancing circuits in the literature, showing the advantages of the cost and balancing speed.

# Chapter 7: Conclusion and Future Works

## 7.1 Conclusion

This thesis presents two cost-effective topologies designed for the redistributive balancing technique in EV applications. The state-of-art battery balancing strategies are comprehensively reviewed, revealing the significant pack capacity gain of implementing the redistributive balancing compared with dissipative counterpart. According to multiple batch cycling data sets and self-collected data set, the redistributive balancing can prolong up to 35% lifetime and 10% pack capacity gain for a 80% EOL definition. The cost and technical requirements listed in the government-issued reports are summarized as a design reference. In order to meet these requirements while achieving advanced redistributive balancing, the BB-APM is proposed whose main functionalities are power conversion, battery gauging, and battery balancing.

The HFB with cored transformer variant is firstly proposed. The detailed circuit modeling applying average and small-signal modeling techniques reveals a commonly undesired VA-imbalance caused by the unbalanced input voltages, leading to a diverging transformer current on the primary side. An asymmetric duty cycle control algorithm is proposed to regulate the diverging transformer current to any arbitrary reference, which is the DC offset current between the adjoining cells in one link. By properly controlling the DC offset current, the C2C balancing mode can be achieved, enabling a faster balancing process, along with the conventional balancing modes The design procedures of the passive components are also given, including output filtering capacitor and the transformer. An iterative transformer design process is presented to fulfill the output power requirement. The digital controllers that regulate the output power and the C2C balancing current are designed based on the detailed models, with the fast response time and robustness. Along with the prototype transformer, the self-designed power stage is tested and four balancing modes are

validated using two NMC cells. The long-term simulation comparison between proposed topology and the conventional one is conducted showing that the balancing time can be reduced by 50%.

The further topological minimizations are achieved through replacing the full bridge on the secondary side with the half bridge, resulting in a further 33% reduction on the number of the active switches. In addition, the coreless transformer that removes the magnetic material is selected for higher circuit integration level and potential higher switching frequencies. Due to the elimination of the core, the coupling between windings is compromised, which invalidates the circuit model proposed for HFB. Therefore, a detailed circuit model considering the imperfect coupling coefficient and the effective turns ratio is developed. The updated power requirements are proposed to guide the characterization of the coreless transformer. As the coupling coefficient is preferred as high as possible, the geometry optimization of the winding layout is performed in FEA software ANSYS/Maxwell. It concludes a various of geometry preferences to achieve high coupling coefficient. The proposed DAHB topology with the integrated coreless transformer is built and validated showing the functional balancing modes.

At low-load conditions, both HFB and DAHB suffers from the dropped system efficiency compared with the nominal-load conditions, due to the loss of the soft-switching capability and high conduction loss. The conventional VFM that overcomes the low-efficiency issue requires a large LUT with all pre-calculated operating points and leaves the system operating in open-loop. Not only is the methodology computational-intense, but also it is not robust to any disturbance in the system. The comprehensive loss analysis on the DAHB and HFB shows that the conduction loss reduces as the switching frequency increases, while the switching loss maintains roughly constant. Therefore, an MPPA criteria aiming to maximize the ratio of the output power and the total RMS is proposed. The MPPA method yields an optimal operating phase shift that is proven to inherently guarantees the ZVS. The large LUT is not required to implement MPPA in embedded systems. Instead, only a linear equation that is a function of the measurable input and output voltages needs to be solved. The validation on the prototype shows that the MPPA-VFM outperforms the conventional VFM by 1-2 % with the robust yet simple closed-loop controller.

Lastly, the cost analysis is performed on the proposed topologies. The component cost for high-volume purchases is estimated using the available information from the large distributors and necessary extrapolations are performed. The single-unit cost is lower than the commercially available balancing solutions which only support dissipative balancing. The batch-production and mass-production costs are estimated based on the number of EVs sold. The 2020 target for the combined system of APM + BMS is $4.2/cell. The 'break-even' point where the redistributive balancing becomes completely complimentary is approximated to be 8,237 vehicles sold for DAHB configuration and 53,824 vehicles for HFB. The cost reduction from HFB to DAHB is roughly 20% over the entire projected range. Compared with the conventional DAB, the cost reduction reaches up to 170% thanks to the lowered number of the MOSFETs and removal of the core. The comparison among the proposed topologies and other state-of-art ones is summarized, in terms of the components, balancing speed and electrical properties.

## 7.2 Future works

The related topics which can be further investigated are listed below:

- The integrated half-bridge modules, such as EPC 9201/3 and SiC 789, are chosen for the fast prototype validation. In order to optimize the system efficiency and cost, the discrete MOSFETs with extremely low $R_{\mathrm{ds,on}}$ can be selected for the DAHB configuration with coreless transformer to improve the efficiency, combining with self-designed gate drivers.

- The proposed coreless transformer design unlocks the flexibility of the PCB design. However, the frame coreless transformer raises some limitations based on the specs of the main component board. For example, the number of layers are determined by the main component board. The fully-interleaved winding layout, which potentially improves the coupling of the transformer, for high turns ratio designs requires the relatively unnecessary PCB layer upgrade on the main component board. The discrete transformer, on the other hand, can be manufactured separately from the main component board, which can be explored more

deeply.

- The resonant converter topology for the coreless transformer configuration is discarded due to the blockage of the DC current path by the resonant capacitor, which eliminates the possibility of balancing adjoining cells in on link. If the neighboring cells are of imbalance, they will not be corrected by the resonant topology. However, this topology can loosen the demand of the high-coupling coreless transformer design, alleviating the requirements on the winding placement. The possible solution for this would be to either engage another low-cost balancing strategy between adjoining cells, e.g. bleeding resistor, or form a multi-level converter that bypasses the resonant capacitor. In exchange, the control is significantly complicated.

- For the DAHB with the coreless transformer, the main source of the losses is the conduction loss. In addition to the MOSFET optimization, the winding design can be improved, such as Litz-PCB, to reduce the AC resistance due to high-frequency operation. However, it is challenging to route the Litz-structure in the transformers with high number of turns.

- With the increasing number of the energy-consuming devices on the LV systems, such as autopilot and more powerful in-vehicle entertainment systems, the power rating of the APM gradually increases. This study proposes the 50-W link prototype which is equivalent to mostly common LV loads. A higher power rated converter can be developed in the future.

- A long-term evaluation of the redistributive balancing system can be performed to investigate the life and driving range improvements compared with dissipative balancing systems for both fresh and aged battery packs.

## 7.3 Publications

### 7.3.1 Accepted papers

- **W. Weizhong**, L. Zhou, M. Eull, G. Cen, and M. Preindl, "Comparison of Litz Wire and PCB Inductor Designs for Bidirectional Transformerless EV Charger with High Efficiency," in *IECON 2020 - 46th Annual Conference on IEEE Industrial Electronics Society (Accepted)*

- L. Zhou, M. Eull, **W. Weizhong**, G. Cen, and M. Preindl, "Design of Transformerless Electric Vehicle Charger with Symmetric AC and DC Interfaces," in *IECON 2020 - 46th Annual Conference on IEEE Industrial Electronics Society (Accepted)*

- **W. Weizhong** and M. Preindl, "Dual Cell Links for Battery-Balancing Auxiliary Power Modules: A Cost-Effective Increase of Accessible Pack Capacity," *IEEE Transactions on Industry Applications*, vol. 56, no. 2, pp. 1752–1765, 2020

- **W. Weizhong** *et al.*, "High-Fidelity State-of-Charge Estimation of Li-Ion Batteries Using Machine Learning," *arXiv preprint arXiv:1909.02448*, pp. 1–8, 2019. arXiv: 1909.02448

- **W. Weizhong** and M. Preindl, "Extended ZVS Modulation for a Dual Cell Link in the Demand of Faster Balancing," in *2019 IEEE/SICE International Symposium on System Integration (SII)*, 2019, pp. 147–152

- **W. Weizhong** and M. Preindl, "Design and Implementation of a Dual Cell Link for Battery-Balancing Auxiliary Power Modules," in *IEEE Transportation Electrification Conference and Expo (ITEC)*, 2018, pp. 898–903

- **W. Weizhong** and M. Preindl, "Modeling and Control of a Dual Cell Link for Battery-Balancing Auxiliary Power Modules," in *IEEE Applied Power Electronics Conference and Exposition (APEC)*, 2018, pp. 3340–3345

### 7.3.2 Patents

- M. Eull, L. Zhou, **W. Weizhong**, and M. Preindl, "A Non-isolated DC Fast Charger For Electric Vehicles," U.S. Patent No. 62/979,935, 2020

### 7.3.3 Under review

- **W. Weizhong** and M. Preindl, "A Condution-Loss Based Variable Frequency Modulation for Dual Active Bridge Converters in Battery Balancing Application," *IEEE Transactions on Industry Electronics (under review)*,

- **W. Weizhong** and M. Preindl, "Cost-effective Dual Cell Links for Battery-Balancing Auxiliary Power Modules with Coreless Transformers," *IEEE Transactions on Vehicular Technology (under review)*,

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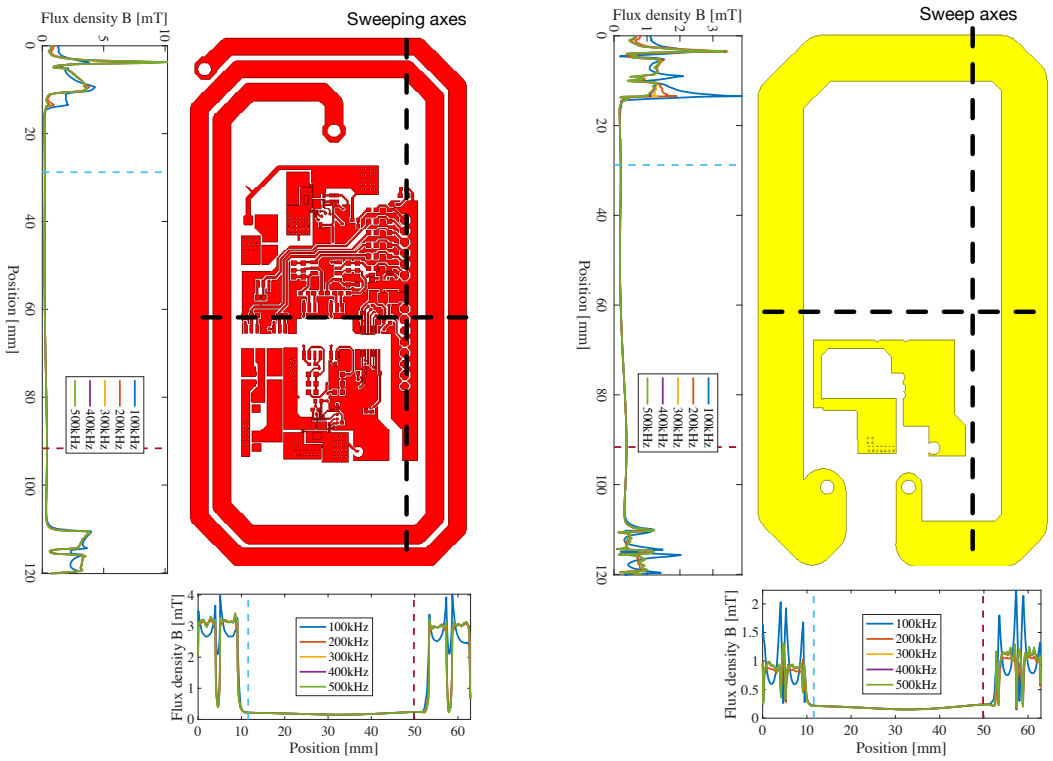
# Appendix A: Flux Density Distribution on the Prototype of Coreless DAHB

One of the concerns of adopting the coreless transformers is the electromagnetic interference generated from the transformer windings without the regulation of the magnetic materials. The high-fidelity ANSYS model, as shown in Figs. A.1 and A.2, is developed to investigate the magnetic strength around the transformer. The 50 A-turn excitations are injected to both primary and




(a) (b)

Figure A.1: The flux density distribution on (a) the top and (b) layer-2 PCBs

secondary windings, which is the peak current amplitude at worst condition for the coreless transformer designed in Chapter 4. It can be seen from both figures that the magnetic field is strong in the near proximity of the transformer traces. The intensity of the magnetic field in the main cir-

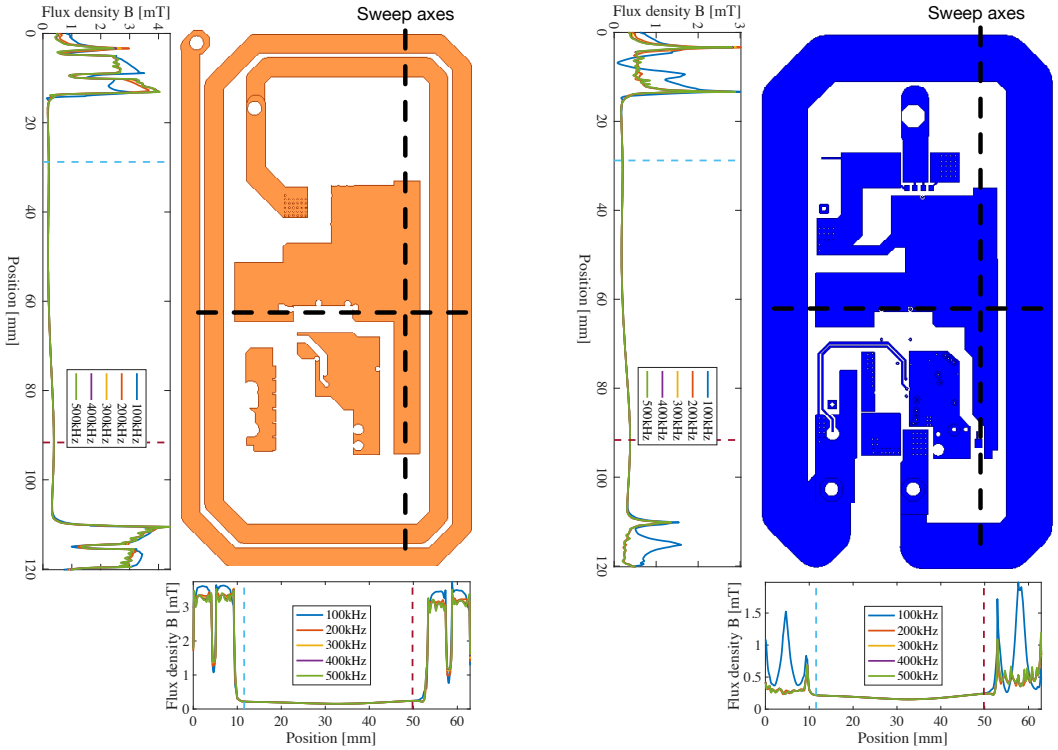



Figure A.2: The flux density distribution on (a) the layer-3 and (b) bottom PCBs

cuit area is significantly lower compared to the area of the transformer traces, which is considered negligible.

# Appendix B: Measurement of HFB with Coreless Transformer

The cored transformer on HFB is replaced by the coreless transformer designed in Chapter 4 to investigate the feasibility of drop-in replacement. The experimental setup is shown in Fig. B.1. The efficiency measurement is shown in Fig. B.2. It shows that the advanced MOSFETs

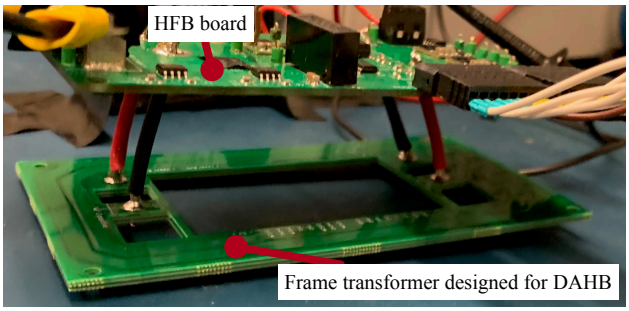



Figure B.1: The HFB with the frame coreless transformer on

with low $R_{ds,on}$ improves the system efficiency significantly. And it is feasible to replace the cored transformer with the coreless transformer with no software/hardware modifications.

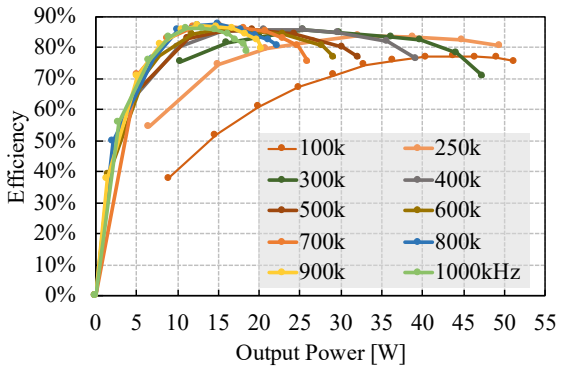



Figure B.2: The measured efficiency of the HFB system with coreless transformer