Optimal Frequency and Critical Soft Switching Control of DC/DC Converter

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Abstract− A critical soft switching technique is proposed to reduce the switching losses of a bidirectional DC/DC converter. The proposed method can improve the efficiency and the value of passive components will be largely decreased. The paper derives the boundary conditions of critical soft switching with the parameters of dead time and threshold current for existing typical SiC and GaN devices. Then, a controlling strategy is developed to estimate and optimize the total power losses of a synchronous DC/DC converter with variable frequency at the given average current and duty cycle. With the combination of critical soft switching and optimal frequency control, the efficiency can be largely improved in every operating point. A power loss curve comparison between the proposed method and hard switching shows that the proposed method can reduce the losses up to 40%. The theoretical results are verified in a rigorous testing procedure.

I. INTRODUCTION

SiC and GaN devices have attracted significant attention due to the high frequency operation capability. Specifically these devices support high performance DC/DC converter designs with high power density. [1-3] The pursuit of small volume can be achieved by reducing the value of passive devices. However, the current ripple should be constrained in a certain range. So, small inductor and high frequency are applied in the design of high power density converters [4-5]. In this paper, the critical soft switching technique is introduced to further improve the efficiency of the converter. The zero voltage soft switching (ZVS) is achieved by controlling the inductor current to satisfy the critical soft switching boundaries. The high turn-on losses are replaced by turn-off losses with critical soft switching. Also, the frequency is controlled to optimize the efficiency within the constraints of critical soft switching operation. In every sampling period, the controller will give the optimal frequency with the given information of average current and duty cycle. So, with the combination of frequency optimization and critical soft switching, the power loss can be decreased.

Some research has published the work of ZVS in DC/DC converters by applying a negative inductor current. [6-7] But the detailed boundary conditions of soft switching need to be further analyzed. This paper derives the critical soft switching conditions in function of dead time and peak/valley inductor current. And a frequency control method is proposed with the combination of critical soft switching technique and efficiency optimization. The paper is organized as follow. Firstly, the boundary conditions to achieve critical soft switching operation for the bidirectional DC/DC converter are derived with dead time and peak/valley inductor current by data sheet and integral equations. Secondly, the power losses of the converter are analyzed in the condition of soft switching operation. The function of power losses with frequency, average current and duty cycle is derived. Thirdly, the optimal frequency controlling method is given to optimize the efficiency. Finally, the theoretical results are verified in a rigorous testing procedure.

II. CRITICAL SOFT SWITCHING OPERATION BOUNDARIES

This section introduces the required critical soft switching conditions by applying the datasheet information of the typical wide band gap devices, SiC and GaN. The boundary constraints for achieving soft switching are derived based on the function of dead time and peak/valley inductor current. By applying the critical soft switching method, the larger turn-on losses of upper switch can be replaced by the smaller turn-off losses of lower switch.

The switching transition of turning-off M2 and turning-on M1 is shown in Fig. 1. The red line represents

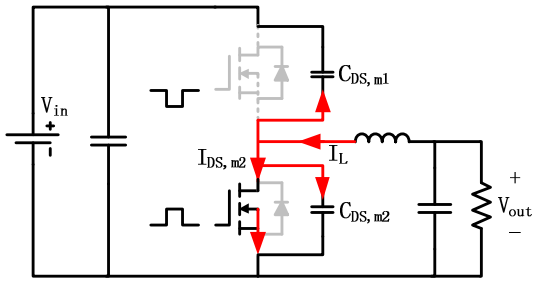

Fig. 1. The negative inductor current paths.

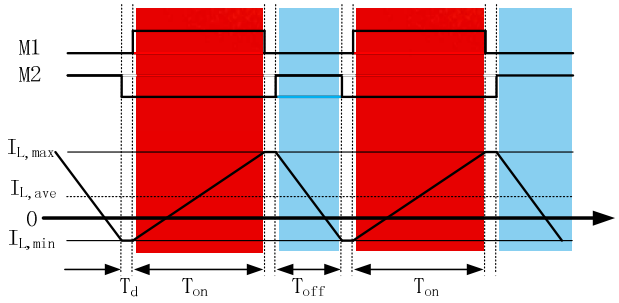

Fig. 2. Gate signals and inductor current for critical soft switching.

the inductor current flowing paths into the switches and drain-source capacitors. For the case of buck operation of the bidirectional DC/DC converter, the inductor current is negative direction in Fig. 1. To guarantee the critical soft switching operation, if the average inductor current is positive, the current ripple should be enlarged to make sure the negative minimum point of the inductor current is lower than a threshold current level. The gate signals and inductor current waveforms of soft switching operation are shown in Fig. 2 where the red areas represent the mode of upper switch ON and lower switch OFF, blue areas represent the upper switch OFF and lower switch ON. The threshold current level is one of the boundary conditions for critical soft switching. During the switching transition of turning-off the lower switch, as is shown in Fig. 1, one branch of the negative inductor current will flow through the output capacitor of upper switch, $C_{oss,m1}$. This current path has the function of discharging the $C_{oss,m1}$. The zero voltage switching operation of upper switch can be guaranteed if the $C_{oss,m1}$ is completely discharged before it turns on. Thus, the zero voltage soft switching of upper switch relies upon the dead time between the two switches and the minimum inductor current value (valley current). According to Kirchhoff laws and the current paths in Fig. 1, the inductor valley current can be expressed as:

$$I_{L,\min} = I_{DS,M2} + I_{coss,M1} + I_{coss,M2} \tag{1}$$

where $I_{DS,M1/2}$ is the drain current, $I_{coss,M1/2}$ is the current through the switch output capacitance, C_{oss}. Because

$$I_{coss,M1(2)} = C_{oss,M1(2)} \cdot \frac{dU_{DS,M1(2)}}{dt} \tag{2}$$

And ($U_{DS,M1}$+$U_{DS,M2}$) equals to the input source voltage, U_{in}, which is a constant value, then $I_{l,min}$ can be expressed as:

$$I_{L,\min} = I_{DS,M2} + (C_{oss,M1} + C_{oss,M2}) \cdot \frac{dU_{DS,M2}}{dt}$$
$$= I_{DS,M2} - (C_{oss,M1} + C_{oss,M2}) \cdot \frac{dU_{DS,M1}}{dt} \tag{3}$$

Similarly, the maximum positive value of inductor current is:

$$I_{L,\max} = I_{DS,M1} + (C_{oss,M1} + C_{oss,M2}) \cdot \frac{dU_{DS,M2}}{dt} \tag{4}$$

The above current equations can be further analyzed by the integral calculation over time and U_{ds}, respectively.

$$\int_0^{T_d} \left[I_{L,\min} - I_{DS,M2}(t) \right] dt$$
$$= \int_0^{U_{in}} \left[C_{oss,M1}(U_{DS,M2}) + C_{oss,M2}(U_{DS,M2}) \right] dU_{DS,M2}$$
$$\int_0^{T_d} \left[I_{L,\max} - I_{DS,M1}(t) \right] dt \tag{5}$$
$$= \int_{U_{in}}^{0} \left[C_{oss,M1}(U_{DS,M2}) + C_{oss,M2}(U_{DS,M2}) \right] dU_{DS,M2}$$

Assuming that I_{ds} is varying linearly with time, the left side of the above two equations in (5) can be calculated as:

$$\int_0^{T_d} \left[I_{L,\min} - I_{DS,M2}(t) \right] dt$$
$$= \int_0^{T_d} \left[I_{L,\min} - (I_{L,\min} - \frac{I_{L,\min}}{T_d} t) \right] dt = \frac{1}{2} I_{L,\min} T_d$$
$$\int_0^{T_d} \left[I_{L,\max} - I_{DS,M1}(t) \right] dt$$
$$= \int_0^{T_d} \left[I_{L,\max} - (I_{L,\max} - \frac{I_{L,\max}}{T_d} t) \right] dt = \frac{1}{2} I_{L,\max} T_d \tag{6}$$

So, the critical soft switching inequalities of $I_{L,min(max)}$ and T_d can be expressed as:

$$\frac{1}{2} I_{L,\min} T_d$$
$$\le \int_0^{U_{in}} \left[C_{oss,M1}(U_{DS,M2}) + C_{oss,M2}(U_{DS,M2}) \right] dU_{DS,M2}$$
$$\frac{1}{2} I_{L,\max} T_d \tag{7}$$
$$\ge \int_{U_{in}}^{0} \left[C_{oss,M1}(U_{DS,M2}) + C_{oss,M2}(U_{DS,M2}) \right] dU_{DS,M2}$$

Thus the minimum negative and maximum positive

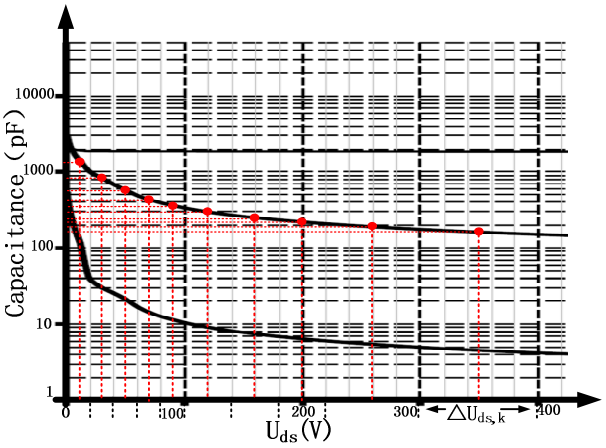

Fig. 3. The discrete points of output capacitance with U_{ds}.

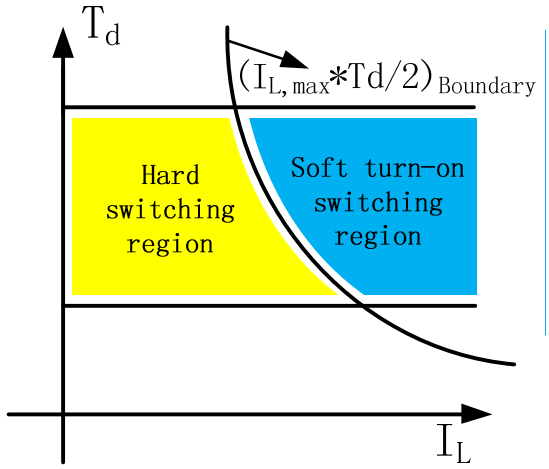

Fig. 4. The boundary conditions for critical soft switching.

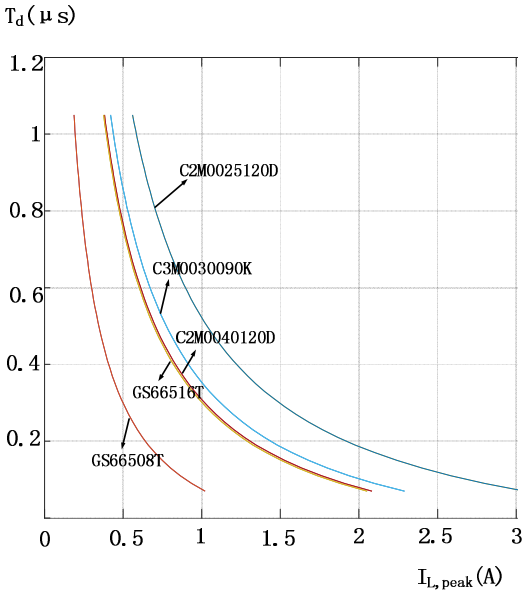

Fig. 5. The soft switching operation regions for different devices.

inductor current can be derived with the variables of dead time, T_d, and the integration of output capacitors with drain-source voltages. The design of the converter should satisfy the two inequalities to make sure the critical soft switching operation. The integration of switch output capacitance with drain-source voltages can be calculated by the datasheet provided by the manufacturer. Fig. 3 shows the relationship of output capacitance with drain-source voltages under the specific testing condition (T_j=25°C, V_{AC}=25mV, f=1MHz). So the integrations of (7) can be calculated by tracing several discrete voltage intervals multiplied by the corresponding capacitance value and then accumulate together. According to Fig. 3, the right side of (7) can be derived by tracing n points on the curve of C_{oss} and summing up the n intervals together:

$$\int_0^{U_{in}} \left[C_{oss,M1}(U_{DS,M2}) + C_{oss,M2}(U_{DS,M2}) \right] dU_{DS,M2} \approx 2\sum_{k=1}^{n} C_{oss,M2}(U_{DS,M2k}) \Delta U_{DS,M2k} \tag{8}$$

Then, the model of critical soft-switching method can be expressed with the function image in Fig. 4. It can be shown that the blue regions are the feasible soft switching range according to the constraints of (7) with the maximum and minimum dead time requirement. Also, the soft switching ranges of typical GaN and SiC devices are given in Fig. 5. During operating in the following sections, the dead time and peak/valley inductor current can be controlled within the critical soft switching region for the optimization of switching losses.

III. SOFT SWITCHING POWER LOSS CALCULATION

This section analyzes the power losses of the DC/DC converter in critical soft switching operation. The power losses mainly include five parts: switching losses, conduction losses, anti-paralleled diodes conduction losses, inductor losses and input/output capacitor losses.

A. Switching losses: the switching losses of the power converter mainly include the turn-off losses of the two switches because the critical soft switching ensures the ZVS of upper switch. So the turn-off losses can be expressed:

$$P_{off,M1} + P_{off,M2} = U_{ds,\max} \cdot I_{ave} \cdot (t_{ru} + t_{fi}) \cdot f_{sw} \tag{9}$$

where t_{ru} and t_{fi} are the voltage rising time and current falling time during the turn-off period, respectively.

B. Switch Conduction losses: the conduction losses of the two switches can be calculated as:

$$P_{con} = R_{ON} \cdot \left[{I_{ave}}^2 + (\frac{\Delta i_L}{2\sqrt{3}})^2 \right] \tag{10}$$

where the ripple current can be substituted by:

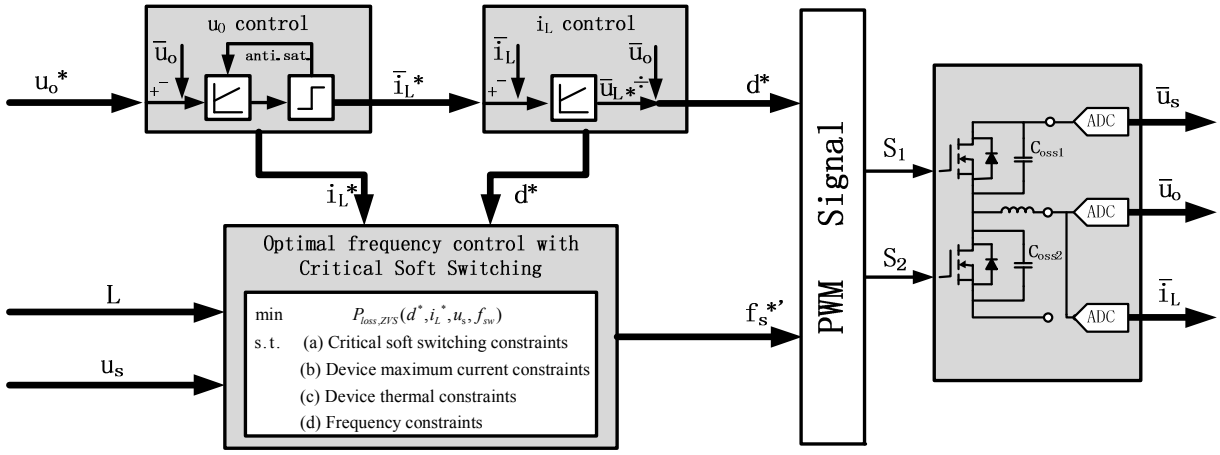

Fig. 6. The controlling blocks.

$$\Delta i_L = \frac{(1-d)\cdot d \cdot u_s}{f_{sw} \cdot L} \tag{11}$$

C. Inductor losses: the inductor losses include core loss and copper losses (AC and DC winding losses)

$$P_L = P_{L,core} + P_{L,DCR} + P_{L,ACR}$$
$$= K \cdot f_{sw}{}^{x} \cdot B^{y} + \left[I_{ave}{}^{2} + \left(\frac{\Delta i_L}{2\sqrt{3}}\right)^2 \right] \cdot R_{DCR} + \left(\frac{\Delta i_L}{2\sqrt{3}}\right)^2 \cdot R_{ACR} \tag{12}$$

where K, x, y are the core material constants and R_{DCR}, R_{ACR} are the DC and AC equivalent series resistance. To simplify, the inductor loss function with frequency can be derived by curve fitting after the type of inductor is predefined.

D. Anti-parallel diodes conduction losses during dead time:

$$P_{con,D} = P_{con,D1} + P_{con,D2}$$
$$= u_{sd} \cdot \left[T_{d,D1} \cdot \left(I_{ave} + \frac{\Delta i_L}{2}\right) + T_{d,D2} \cdot \left(I_{ave} - \frac{\Delta i_L}{2}\right) \right] \cdot f_{sw} \tag{13}$$

where $T_{d,D1}$ and $T_{d,D2}$ are the dead time of the two anti-parallel diodes.

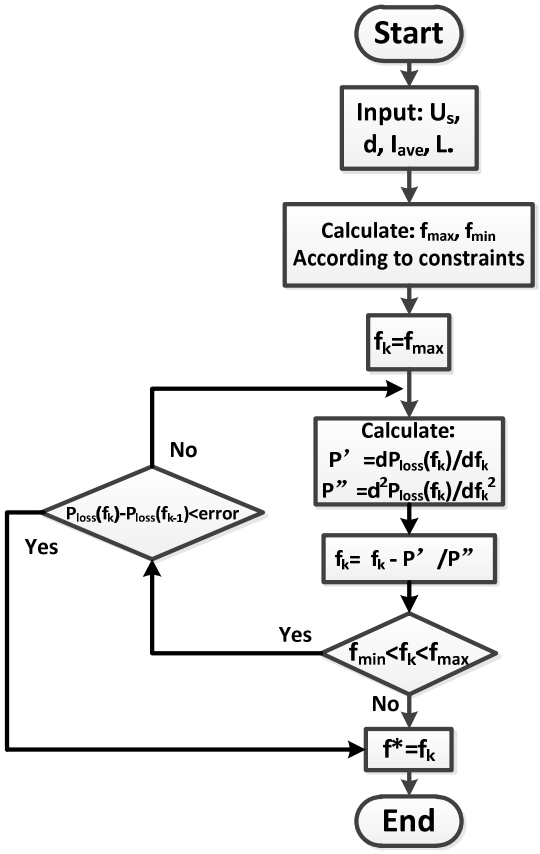

Fig. 7. The power losses optimization flow chart.

IV. VARIABLE FREQUENCY CONTROL FOR OPTIMAL EFFICIENCY

This section gives the controlling method for optimal efficiency. The proposed idea is based on the combination of critical soft switching technique and variable frequency control. By adjusting the frequency according to the given output voltage and current references, the total power losses can be minimized in the operation of soft switching. Because the power losses are the function of frequency, average current and ripple current and the ripple current can be expressed by duty cycle and frequency according to equation (11), the efficiency can be optimized by frequency within the operation ranges of duty cycle and average current. To work under critical soft switching the constraints of two threshold peak/valley inductor current should be added to the optimization according to the derivation of section II.

So the Power losses cost function can be expressed as:

$$\min \quad P_{off,M} + P_{con} + P_L + P_{con,D} \tag{14}$$

The constraints mainly include critical soft switching

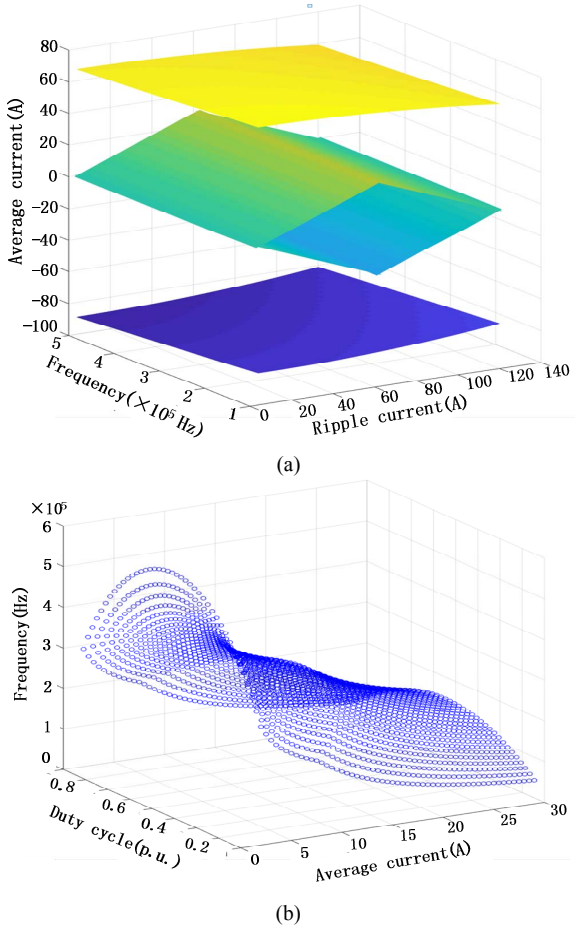

Fig. 8. The thermal, soft switching, frequency and device current constraints (a) of $\triangle i_L$ with the function of f_{sw} and I_{ave} (b) the optimal f_{sw} regions with relationship of duty and I_{ave}.

threshold current, I_{th}, maximum device current, I_{max}, maximum thermal rising, $P_{thermal,max}$ and frequency ranges:

$$
\begin{aligned}
s.t. \quad & I_{th} \le I_{p+} = I_{L,ave} + \frac{\Delta i_L}{2} \le I_{\max} \\
& -I_{\max} \le I_{n-} = I_{L,ave} - \frac{\Delta i_L}{2} \le -I_{th} \\
& P_{sw} + P_{con} \le P_{thermal,\max} = \frac{T_{j,\max} - T_{case}}{R_{th,J-C}} \\
& f_{sw,\min} \le f_{sw} \le f_{sw,\max}
\end{aligned}
\tag{15}
$$

So, within the constraints above, the controller will find the minimal power loss with the given duty cycle and current reference. And the controlling blocks of the DC/DC converter are shown in Fig. 6 where the optimal frequency under critical soft switching operation can be derived in every calculating round. In each calculating period, the optimal frequency is derived according to the cost function and constraints to achieve highest efficiency under critical soft switching operation. [8] For the purpose of fast convergence, the algorithm is based on Newton Method. By applying the 2nd order Taylor Expansion of the power loss function, the minimal point of frequency can be obtained with the iterative formula of 1st and 2nd power loss derivative in every calculating round:

$$
f_{sw,k+1} = f_{sw,k} - \frac{P'_{loss}(f_{sw,k})}{P''_{loss}(f_{sw,k})} \tag{16}
$$

The terminating conditions of the iteration are the constraints in (15) and the predefined error. The flowchart of the optimization method is given in Fig. 7.

V. RESULTS

The power losses calculation and frequency optimization are implemented in this section based on a typical SiC device, GS66516T. Fig. 8(a) shows the constraints of maximum thermal rising (70 ° C), soft switching peak/valley current threshold and maximum device current with the function of frequency, average current and ripple current. The constraint functions can be transferred to the parameters of duty cycle, average current and frequency according to (11). The optimal frequency regions can then be derived with the combination of the cost function and constraints which are shown in Fig. 8(c). For the optimal regions of frequency, every point is calculated by the Newton Method within the constraints of equation (15).

Also for the control of power converter, rigorous testing procedure is implemented with voltage and current steps. The circuit parameters are: input voltage 400V, output voltage 200V, inductor 10uH, operation time 3ms. Fig. 9(a) and 9(b) show the duty cycle, time period, inductor current and output voltage waveforms. Specifically, Fig. 9(a) is the condition of output voltage reference step from 200V to 250V. Fig. 9(b) is the condition of current reference from 2A to 8A. With the proposed controlling method, the frequency can be adjusted simultaneously with the variation of reference to achieve the optimal efficiency under soft switching operation (the upper and lower constraints of frequency are also shown in Fig. 9). Finally,

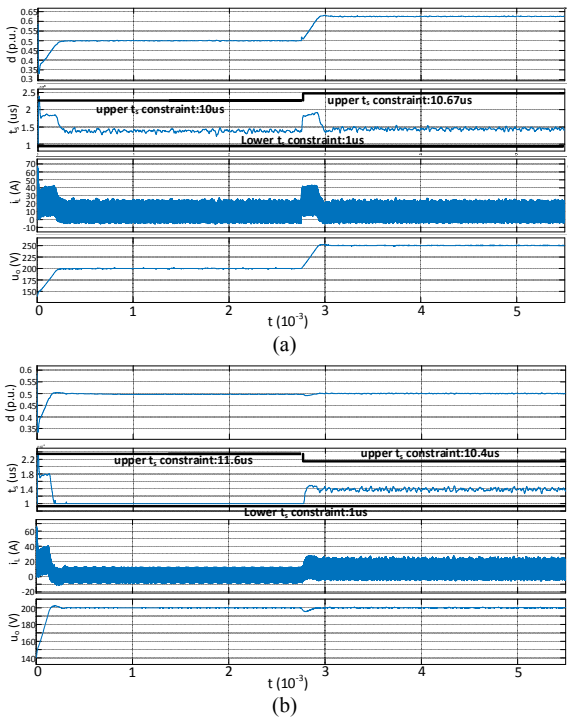

Fig. 9. The results with output voltage/current reference step.

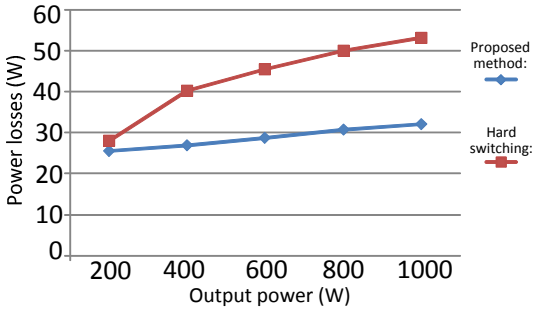

Fig. 10. Power losses comparison between proposed method and hard switching.

the comparison of total power losses between the proposed method and hard switching is given in Fig. 10 from 200W to 1000W. The loss curves show that the proposed method can reduce the losses up to 40%.

VI. CONCLUSION

This paper proposes a controlling method for DC/DC converter with the combination of critical soft switching and variable frequency control. The precise critical soft switching boundaries for DC/DC converter are derived with the parameters of dead time and peak/valley inductor threshold current. The total power losses are calculated in the operation of soft switching. The proposed controller can minimize the losses by adjusting the frequency with every duty cycle and current reference. For the optimization implementation, the algorithm is constrained by the ranges of soft switching operation, thermal, frequency limitation and device current tolerance. The results verify the validity of the theoretical analysis.

VII. ACKNOWLEDGEMENT

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