Zero Sequence Power Balancing Compensation for Third Harmonic Injection of Multi-Stage Grid-Tied Energy Conversion Systems

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***Abstract*—DC bus voltage utilization is a key parameter that highly influences the voltage rating of the devices when designing a grid connected inverter. Thus, the maximum voltage rating of devices should be taken into consideration which increases the cost of hardware components. An effective way to improve the DC bus utilization is third harmonic injection. This paper proposes a zero sequence power balancing compensation method for third harmonic injection (THI) through zero sequence reference frame. Compared to the traditional direct injection method in the duty cycle, the new idea adds the third harmonic component to the zero sequence voltage (ZSV) controller. Thus, the injected third harmonic part is controlled through zero sequence controller without introducing extra harmonics to the grid. Also, the zero sequence power balancing method is proposed to compensate for the DC bus oscillation caused by the THI in multi-stage grid connected system. With the zero sequence compensation method, the DC bus controller is further stabilized without generating oscillated harmonics to the current controller for the grid.**

I. Introduction

In a grid connected inverter, if DC bus is utilized close to 100%, duty cycle saturation issue may cause distortion on the grid side. Also the control loop will be deteriorated by the saturation of duty cycle [1]–[5]. A grid connected inverter may encounter the overvoltage issues in the grid side, which could result in saturation issues on the duty cycle [6]–[8]. Several papers have proposed the THI method to decrease the peak grid voltage value [9]–[11]. Most of the applications are implemented by directly adding the third harmonic component to the duty cycle [12]–[14]. The traditional direct THI methods have a main drawback of grid current distortion, because a third order harmonic is directly injected to the grid side [15]–[18]. Thus, the THD of grid current may violate the standard requirement.

Firstly, this paper proposes a zero sequence THI method through zero sequence reference frame. The controlling method is implemented based on the topology shown in Fig. 1. Different from traditional three phase inverter, this topology has the function of limiting the zero sequence current by connecting the common point of three phase LC capacitors and the negative terminal of DC bus which has been addressed in red line [19], [20]. A ZSV controller is implemented to bypass the zero sequence current at the aim of reducing the leakage current flowing through the parasitic capacitor. The principle is to control the zero sequence component of three phase LC capacitor voltage as Vdc/2 [21], [22]. The third harmonic voltage is added to Vdc/2 as the reference

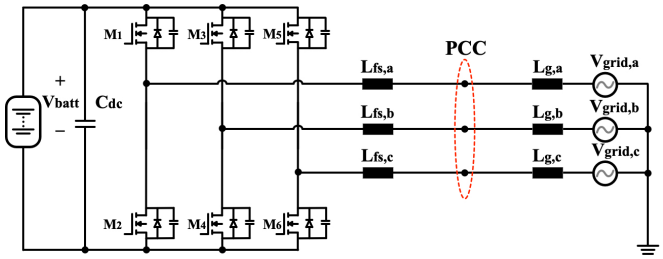

Fig. 1. Conventional single stage grid-connected L converter topology.

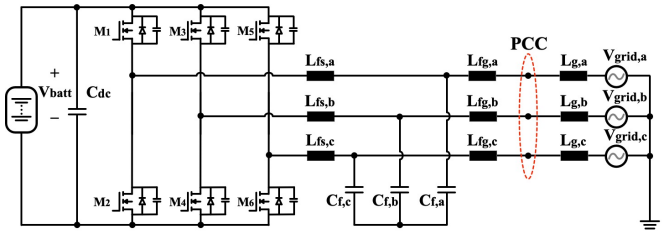

Fig. 2. Conventional single stage grid-connected LCL converter topology.

for the ZSV controller. By injecting the third harmonic into the zero sequence controller, the third order components will be restricted to circulate within the LC capacitors instead of being injected to the grid side. Thus, the grid current could be purified to achieve third harmonic injected grid voltage. Secondly, considering the two stage power conversion applications, the DC bus will be distorted by the injected third harmonic which could distort the DC bus controller and result in the distortion of grid current due to an oscillated current reference from the DC bus controller [23]–[25]. A zero sequence power balancing method is also proposed to compensate for the grid current distortion caused by the DC bus oscillation. A DC bus zero sequence voltage is derived through instantaneous zero sequence power balancing theory. This derived DC bus ZSV is calculated to compensate for the DC bus controller and correct the reference for grid current control.

II. Third Harmonic Injection Techniques for Modulation Index

Firstly, the traditional third harmonic injection techniques are studied in this section by evaluating the corresponding merits and existing issues. A typical third harmonic injection

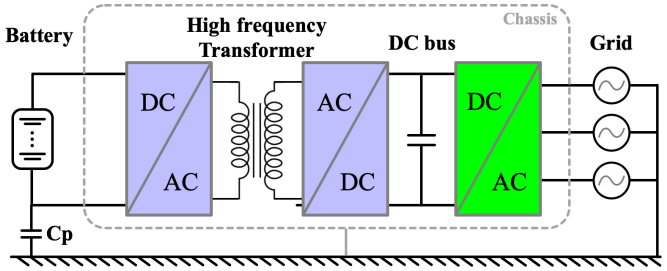

Fig. 3. Typical multi-stage grid-connected energy conversion system.

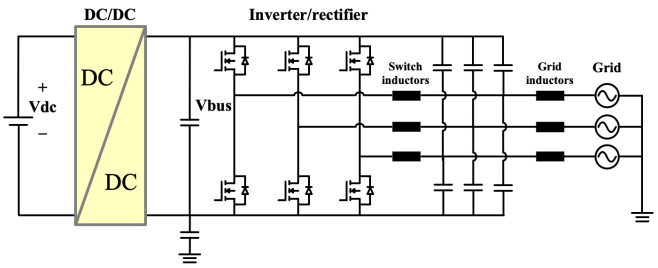

Fig. 4. Two-stage three-phase grid-connected converter topology for third harmonic injection zero sequence power balancing compensation.

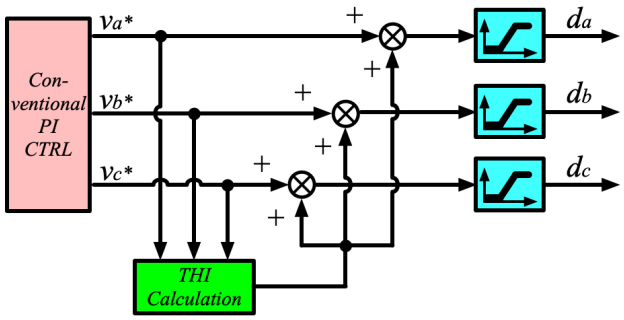

Fig. 5. Conventional third harmonic injection principle for gri-connected inverters.

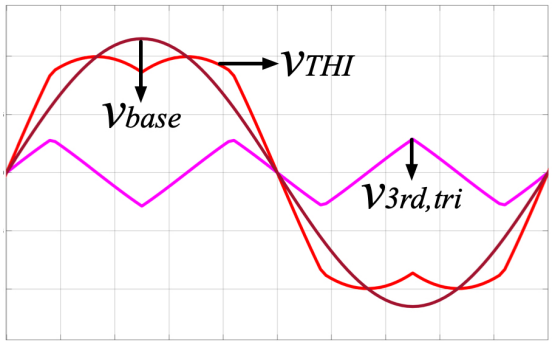

Fig. 6. Output voltage waveforms before and after third harmonic injection and the third order components for THI.

principle can be demonstrated in Fig. 5. The third order components of output voltage or duty cycles are extracted through the THI calculation equations. Then, the third order components are directly injected to the modulation for the improvement of modulation index. Specifically, the THI calculation equations can be derived as:

$$v_{3rd} = \tau_{coeff} \times [max(v^*_{o,abc}) + min(v^*_{o,abc})] \quad (1)$$

based on the extraction from output voltage references or

$$v_{3rd} = \tau_{coeff} \times [max(d_{abc}) + min(d_{abc})] \quad (2)$$

based on the extraction from three-phase duty cycles. τ_{coeff} represents the coefficient that determines the third harmonic injection depth. The output voltage waveforms before and after third harmonic injection have been shown in Fig. 6 where the black waveform is the output voltage without third harmonic injection and the red waveform is the output voltage with the third harmonic injection. The magenta waveform is the extracted third order components to be injected to the output voltage references or duty cycles.

To evaluate the effectiveness of a typical THI method, a voltage gain can be defined as the ratio of the fundamental component output voltage peak value, v_{base}, to the reference modulation waveform peak value, v_{THI},

$$G_v = \frac{v_{base}}{v_{THI}}. \quad (3)$$

The maximum voltage gain of the continuous THI methods can be derived at the $\pi/3$ when the third harmonic is at zero crossing point. Thus,

$$G_{v,max} = \frac{1}{sin(\pi/3)} \approx 1.155. \quad (4)$$

By leveraging the THI methods, the DC bus voltage can be reduced by a factor of 1.15 and the voltage stress, switching losses on the power switches can be decreased, accordingly.

Thus, the merits of the conventional third harmonic injection methods can be concluded as: (1) Improvement on the DC bus utilization to invert power from DC to AC with lower level of DC bus voltage; (2) Less requirement on the phase leg power switches voltage rating to reduce the switching losses; (3) Lower power switch device cost due to less rated voltage requirement from DC bus side.

However, besides the above mentioned merits, the conventional THI methods also have some issues that need be solved or optimized. Firstly, in a single stage power conversion system for the typical L or LCL filtering grid-connected inverters shown in Fig. 1 and Fig. 2, the injected third order components reduces the peak-to-peak values of the three-phase output voltages. In the meantime, the third harmonics are also added to the output currents. Thus, extra harmonics will be flowing into the grid. The quality of grid waveforms will be deteriorated. Accordingly, the total harmonic distortion (THD) will be increased which may violate the grid connection codes.

Secondly, in a multi-stage grid-connected power conversion system as is shown in Fig. 3, the last energy conversion stage of DC/AC inverter is directly interfaced with the grid. The DC link voltage is not a fixed value as the single-stage inverter. Since no DC voltage source is directly connected to the DC link to clamp the bus voltage as constant. Thus, in the multi-stage energy conversion system, when implementing a third harmonic injection, there exists a third order components fluctuation on the DC link which could deteriorate the output

waveform quality and modulation index. On one hand, the third order fluctuation on the DC link of multi-stage energy conversion system reduces may result in the overmodulation issue if the valley points of the DC bus voltage is lower than the peak value of output sinusoidal voltage. Extra distortion will then be reflected on the modulation and output current to be flowing into the grid. On the other hand, a high third order fluctuation ripple on the DC link will cause extra switch voltage stress. Accordingly, more switching losses will be induced.

III. Zero Sequence Third Harmonic Injection

A conventional single-stage grid-connected LCL inverter is shown in Fig. 2. Different from the traditional topology, in this paper as is shown in Fig. 4, the connecting wires between the common points of three-phase output capacitors and the positive/negative terminals of DC bus are configured to bypass the zero sequence leakage current by the ZSV controller. Specifically, ZSV of three phase LC capacitors are derived through Park and Clarke transformations. This ZSV can be controlled to half of DC bus to provide the zero sequence current reference for the latter zero sequence inductor current controller. In the mean time, The d and q components of the inductor current references are derived from the DC bus controller and reactive power controller, respectively.

The proposed THI method is added to the ZSV controller shown in the yellow and green blocks of Fig. 7. The ZSV third harmonic component is calculated from the three phase voltage references:

$$v_{0,3rd} = \tau_{coeff} \times [max(v_{g,abc}) + min(v_{g,abc})] \tag{5}$$

So, the sum of maximum and minimum three phase voltage in every sampling instant is applied to derive the third harmonic reference and added to the ZSV controller. To be noted that, the coefficient of τ_{coeff} determines the amplitude of third harmonic. Thus, the DC bus utilization is related to τ_{coeff} and PI gains of ZSV controller. According to the iterative test, a τ_{coeff} of 2 can achieve best performance of grid voltage adjustment.

IV. Zero Sequence Power Balancing Compensation in Multi-Stage System

For the multi-stage power conversion system, specifically two stage DC/DC+DC/AC topology, the DC bus is expected to be controlled to provide the reference for following cascaded current controller. In this application, a THI in AC side will cause the oscillation of DC bus [26]. Thus, the following current controller will be distorted by an oscillating current reference [27]. An instantaneous zero sequence power balancing method is proposed to compensate for the grid current distortion. Firstly, the general instantaneous power balancing for AC and DC side are:

$$v_{dc} \cdot i_{dc} = v_{abc}^T \cdot i_{abc} \tag{6}$$

where v_{dc}, i_{dc}, v_{abc} and i_{abc} are the DC, AC side currents and voltages, respectively.

So, the DC current can be expressed by duty cycles matrix, D_{abc}=[D_a, D_b, D_c], and AC current as:

$$i_{dc} = D_{abc}^T \cdot i_{abc} \tag{7}$$

For (2) and (3), the instantaneous power equation applies to the superposed components of active power and zero sequence power. So, only zero sequence component is considered to derive the compensation. The zero sequence current on DC side is expressed as:

$$i_{0,DC} = D_{abc}^T \cdot i_{0,AC} \tag{8}$$

where $i_{0,AC}$ represents the AC side zero sequence current matrix [$i_{0,AC}$; $i_{0,AC}$; $i_{0,AC}$] and $i_{0,DC}$ is the DC side zero sequence current.

Thus, the ZSV on the DC capacitors, $v_{0,DC}$, can be further derived from:

$$C_{DC} \cdot \frac{v_{0,DC}}{dt} = i_{0,DC} \tag{9}$$

And this calculated zero sequence component is used for the compensation of DC bus voltage controller. The controlling block of zero sequence power balancing has been shown in the red of Fig. 7.

TABLE I
System Parameter Configurations

Parameter	Value
Switching frequency	100kHz
Switch side inductor, L_{fs}	45μH
Grid side inductor, L_{fg}	45μH
Output Capacitor, $C_{f,up/low}$	12μF
MOSFET	C2M0025120D
Controller	LAUNCHXL-F28379D
Output Voltage THD	$<$ 2.0%
Output Current THD	$<$ 2.0%

V. Results

The testing system parameters of the proposed controlling algorithms are shown in Table I. Fig. 8(a) shows the PCC grid voltage with respect to the negative DC bus and the grid current waveforms in single stage DC/AC grid inverter. From 0.1s on, the THI is implemented. And the valley-peak range of grid voltage is reduced from (30V-820V) to (90V-760V) which improves the DC bus utilization by 15%. Fig. 8(b) shows the grid voltage and current in two-stage DC/DC+DC/AC grid inverter system. Before the time of 0.2s, the THI is implemented without the zero sequence power balancing compensation. The grid current is distorted due to the ZSV injection with a THD of 8%. Then, the compensation is added and the grid current is corrected with a THD of 1%. Fig. 9(a) gives the compensated, measured and derived zero sequence DC voltage. It can be seen the DC oscillation is compensated to 1/8. Thus, the current reference of Id is stabilized accordingly as is shown in Fig. 9(b). Fig. 10 shows the waveforms of switch side inductor current, output capacitor voltage, grid current, DC bus voltage and zero sequence third order injected component. Fig. 11 shows the transient waveforms of output capacitor voltage and zero sequence third order injected component after and before the THI implementation.

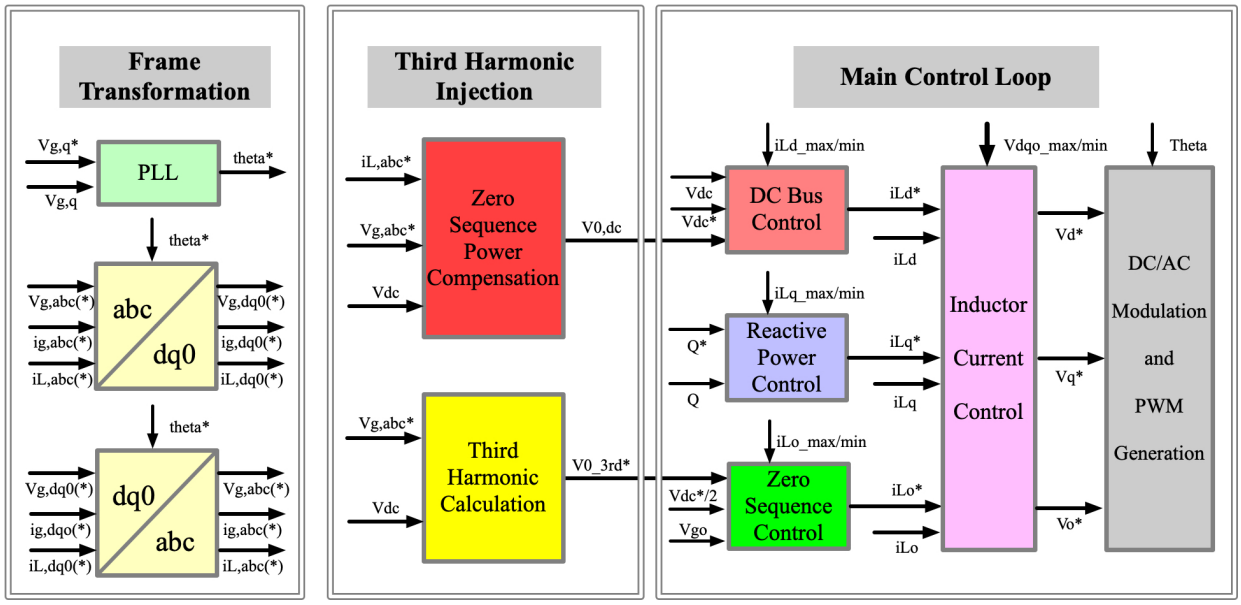

Fig. 7. Zero sequence power balancing for third harmonic injection control diagram.

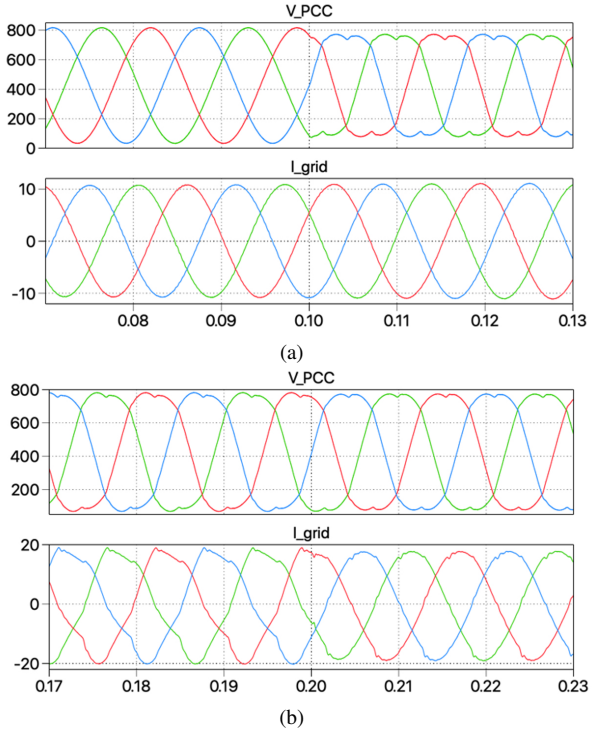

Fig. 8. (a) Single-stage and (b) two-stage grid-tied converters output voltage and current waveforms before and after third harmonic injection.

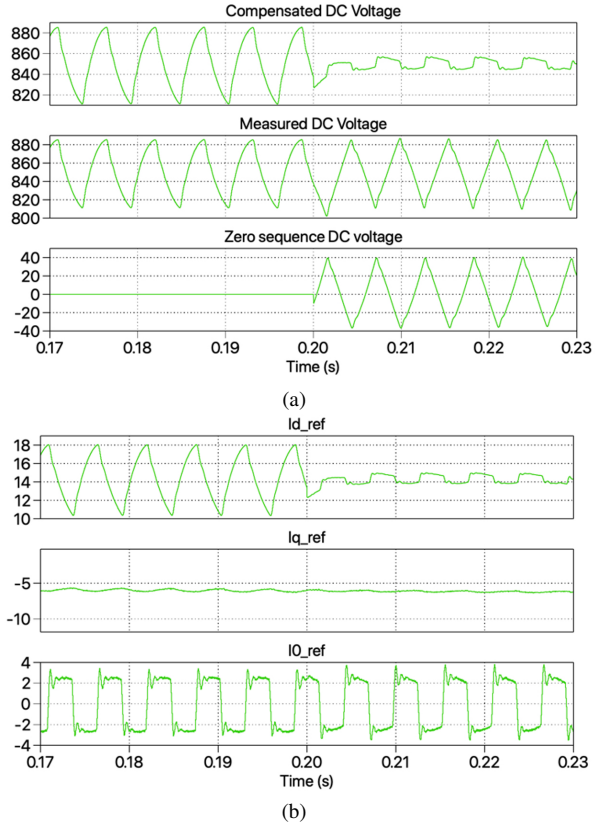

Fig. 9. (a) Compensated, measured DC voltage, zero sequence DC voltage and (b) $dq0$ sequences current references.

VI. Conclusion

This paper proposes zero sequence third harmonic injection and zero sequence power balancing compensation methods to improve the DC bus voltage utilization and reduce the grid current distortion. The THI is implemented through zero sequence voltage controller and bypassed by the negative connection path. So, no distortion will be injected to the grid current. Also, for the multi-stage systems, the distorted DC bus voltage is compensated by the zero sequence power balancing method to further improve the grid current quality. The DC bus ratio is increased by 15% and the THD of grid current is reduced from 8% to 1%.

Fig. 10. Experimental waveforms of output capacitor voltage, switch side inductor current, grid current, DC bus voltage and zero sequence THI voltage.

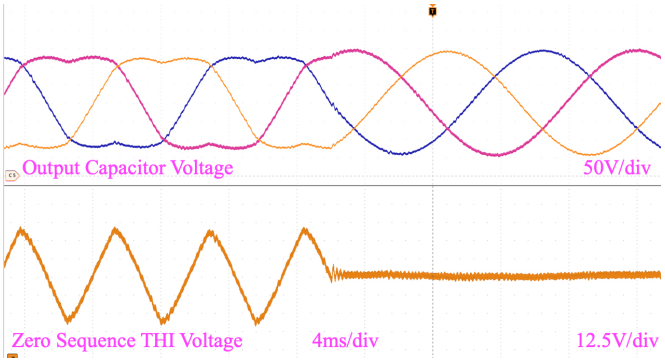

Fig. 11. Experimental transient waveforms of output capacitor voltage and zero sequence voltage after and before THI.

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