A Three-Phase Partial Power Processing Soft-Switched Inverter

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***Abstract*—This article presents a three-phase partial-power-processing inverter with provisions to soft-switch over the entire cycle of the grid. Each modular phase of the inverter is constructed from a reconfigured dual-active half bridge (DAHB) that has been folded across its galvanic isolation and its primary and secondary sides placed in series through stacking. The power processed through each stacked DAHB is less than its output power, with the ratio between processed and output powers defined by the voltage conversion ratio of the stacked DAHB. Analysis of the stacked DAHB is presented within the framework of the Manhattan topology, a multilevel converter topology defined by a set of series stacked capacitors where there exists a scheme to transfer power between capacitors. The capacitive power transfer mechanism in the proposed is a DAHB. This analysis shows that the stacked DAHB operates as a controlled current source. This feature is leveraged by configuring three stacked DAHBs as a three-phase grid-following inverter where the inverter is only responsible for injecting a current into the grid. Two control schemes are provided, one with a constant switching frequency that is susceptible to hard-switching and another that uses a variable switching frequency to maintain soft-switching over the cycle of the grid. A 3 kW prototype is constructed using GaN FETs and a switching frequency of up to 1 MHz. Experimental efficiency, current quality, transient, and power step results are provided for the two different control schemes.**

***Index Terms*—AC/DC, inverter, partial power, power converter, soft-switching.**

I. Introduction

PARTIAL power processing (PPP) converters are a unique category of power converters where the power processed internally to the converter is less than output power of the converter. This is enabled by allowing a portion of the output power to flow through the converter unprocessed, which can be visualized in Fig. 1. The amount of power that ultimately has to be processed by the converter is dependant on its voltage conversion ratio [1], which is a feature that can be leveraged in the design process.

PPP converters can provide an improvement of the power conversion efficiency [2]. As shown in Fig. 1, if the efficiency of the power processing converter is η' and the ratio of power processed to power output is α, the total system efficiency η can be found as

$$\eta = \frac{\eta'}{\eta'(1-\alpha)+\alpha}. \tag{1}$$

As α wll always be less than one, the total system efficiency η will always be greater than the processed power efficiency η', and in this way the PPP configuration can be used to improve efficiency. There is, however, typically an additional requirement of isolation placed on the power conversion block of the PPP converter [1] that must be considered as some efficiency can be lost in the implementation of this isolation [3]. Despite this, it can be shown that the VA requirements of the semiconductor and passive components of the PPP converter can be decreased when compared to their full power processing (FPP) counterparts [4]. PPP converters can also be used for power density improvements as a reduction in the required processed power can yield some reduction in volume of the power electronics components [5], [6].

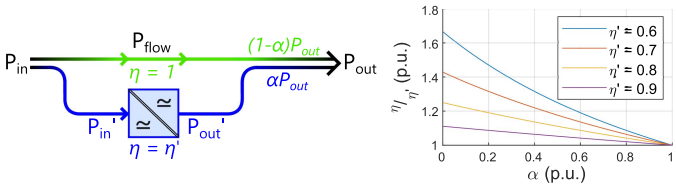

Fig. 1. Left: visualized power flow of PPP converters. Right: overall system efficiency improvement η/η' as a function of the ratio of total power to processed power (α) for different processed power efficiencies η'.

PPP converters have proven applications in the areas of photovoltaic integration [7], [8], [9], battery charging [10], [11], [12], and LED driving [13], [14], [15]. These are all dc–dc applications [16] where the PPP converter operates within a relatively limited range of voltage conversion ratio. This allows for the design to be optimized for operation within this range, convenient for dual-active-bridge (DAB)-based PPP converters [17], [18] as DAB performance can suffer at extremes of the voltage conversion ratio [19].

Applications of PPP converters to ac systems are limited. They are largely based around two-stage inverters where the PPP converter is used as a dc/dc stage and the ac interface is any variant of an FPP converter [20], [21], [22], [23]. [24] diverges from this norm and uses the PPP converter to create a quasi-dc link, but this is still a two-stage design. Lopez et al.'s [25] work is, to the best of our knowledge, the only application of PPP converters as an ac interface. It uses two flyback converters as

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the power processing units of a PPP single-phase ac interface but does not comment on how the internal operating point of the power-processing units change over the cycle of the grid nor does it provide experimental results.

This work shows a three-phase PPP ac inverter constructed from three phase-modular stacked dual-active half bridges (DAHBs) where each DAHB is a power processing unit. It is shown through both experimental results and theoretical calculations that the application of PPP converters to ac systems can be used to improve overall efficiency.

First, the phase-modular stacked DAHB is analyzed within the framework of the Manhattan topology [26], [27], [28], a multilevel converter topological family defined by a set of series stacked capacitors where there exists a scheme to transfer power between capacitors. Notably, the level voltages of this topology are intended to change with the the output voltage, which is atypical of multilevel converters. In the context of the proposed, the DAHB is used as the capacitive power transfer mechanism.

First, analysis of the inverter follows the change in operating points over one cycle of the grid, most notably the dynamic voltage conversion ratio of the DAHB and the performance characteristics that are defined by it. Two control schemes are provided and discussed, one with a constant switching frequency for hard-switched DAHB applications and another with a variable switching frequency. The variable switching frequency is used to keep the stacked DAHB within its soft-switching region over the cycle of the grid and its associated large range of required voltage conversion ratios. Other DAB-based PPP converters use different techniques to maintain soft-switching, such as Fu et al.'s [29] work, which uses a dual-phase shift modulation scheme and Anzola et al.'s [30] work, which operates the DAB in resonance.

Finally, a 3 kW experimental prototype is constructed using GaN FETs and a switching frequency of up to 1 MHz. Experimental efficiency, current quality, transient, and power step results are provided for the two different control schemes. It is important to note that optimization of the DAHB power processing unit is not within the scope of this article. Emphasis is placed on the performance improvement of the DAHB configured as a PPP converter. It is experimentally shown that the PPP configuration offers a $+++9\%$ efficiency improvement over the efficiency of the processed power and the soft-switching scheme offers a 2%–4% efficiency improvement over the hard-switched scheme.

II. Topology Description

A. Capacitive Power Transfer

The topology of the proposed PPP three-phase inverter can be seen in Fig. 2. It is grid-tied and consists of three phase-modular units that operate together to interface with the three-phase grid. Each phase-modular unit is a stacked DAHB and will be analyzed independently. Fig. 3(a) shows how each phase module of the proposed inverter is constructed from a reconfigured DAHB.

As previously mentioned, each stacked DAHB is analyzed within the framework of the Manhattan configuration [26], [27], [28], which begins by redrawing the circuit as a set of four

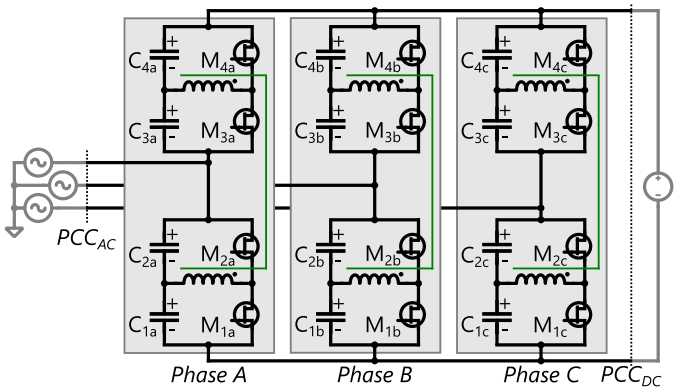

Fig. 2. Topology of the proposed three-phase PPP inverter constructed from three phase-modular stacked DAHBs.

stacked capacitors with obfuscated power transfer mechanisms between the capacitors. This transformation can be seen in Fig. 3(c), where the circuits of Fig. 3(b) and (c) are intended to be functionally equivalent. The DAHB is the power transfer mechanism between the four capacitors in the stack.

The input voltage V_s is applied across all four capacitors C_{1-4} between nodes V_4 and V_0. The output voltage V_o is taken at the center node between V_2 and V_0, across capacitors C_{1-2}. Node V_4 and V_0 are the nodes of highest and lowest potentials, respectively, and can be considered as a dc link equivalent. The *input* and *output* nomenclatures are used for convenience as each stacked DAHB is capable of bidirectional power flow, which is a necessary condition for their ac application.

The main capacitive power transfer mechanism is denoted as P_ϕ. P_ϕ transfers power between the set of upper capacitors C_{3-4} and the set of lower capacitors C_{1-2}. A nonzero value of P_ϕ is necessary to maintain capacitor voltage balance in steady-state for nonzero output power [26]. This is proven by analyzing the average currents through each individual capacitor during steady-state operation of the circuit, as drawn in Fig. 3(c), as

$$I_{C4} = I_s + I_{C\phi 4} \tag{2}$$
$$I_{C3} = I_s + I_{C\phi 3} \tag{3}$$
$$I_{C2} = I_s - I_o + I_{C\phi 2} \tag{4}$$
$$I_{C1} = I_s - I_o + I_{C\phi 1}. \tag{5}$$

I_s and I_o are the capacitor currents due to the externalities of the input and output currents, respectively. $I_{C\phi 1-4}$ are the individual capacitor currents due to the capacitive power transfer mechanism.

Maintaining voltage balance in steady state requires the average current through each capacitor to be equal to zero. This is done by using the capacitive power transfer mechanism to set $I_{C\phi 1-4}$ to values that cancel the capacitor currents due to I_s and I_o. The values of $I_{C\phi 1-4}$ are set such that

$$I_{C\phi 4} = I_s \tag{6}$$
$$I_{C\phi 3} = I_s \tag{7}$$
$$I_{C\phi 2} = I_s - I_o \tag{8}$$
$$I_{C\phi 1} = I_s - I_o. \tag{9}$$

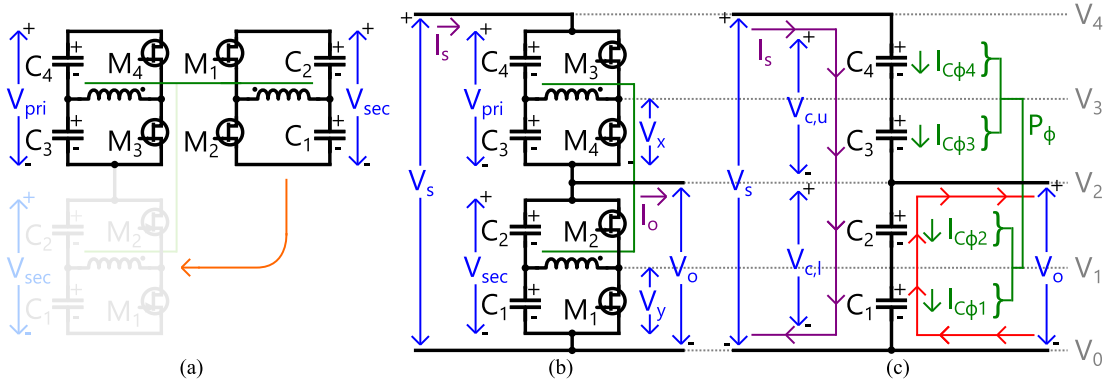

Fig. 3. (a) Reconfiguration of a DAHB into a stacked DAHB. (b) Resulting phase-modular stacked DAHB used in the proposed inverter. (c) Stacked capacitor and capacitive power transfer mechanism framework used for analysis. In these analyses, $V_{\text{pri}} = V_{c,u}$ and $V_{\text{sec}} = V_{c,l} = V_o$. P_ϕ is the power transferred over the inductive coupling of the DAHB.

A similar analysis can be done in the power domain. The values for $I_{C\phi 1-4}$ that need to be induced to maintain capacitor voltage balance in steady state can be considered as excess powers within C_{1-4} that need to be exchanged amongst each other as

$$P_{e,C4} = V_{C4} I_s \tag{10}$$

$$P_{e,C3} = V_{C3} I_s \tag{11}$$

$$P_{e,C2} = V_{C2}(I_s - I_o) \tag{12}$$

$$P_{e,C1} = V_{C1}(I_s - I_o). \tag{13}$$

$P_{e,C1-4}$ are found by taking the product of $I_{C\phi 1-4}$ and its respective capacitor voltage. $P_{e,C1-4}$ are then rearranged into the excess powers within the set of upper capacitors $P_{e,u}$, consisting of C_3 and C_4, and excess powers within the set of lower capacitors $P_{e,l}$, consisting of C_1 and C_2, as

$$P_{e,u} = I_s(V_{C3} + V_{C4}) = I_s(V_s - V_o) \tag{14}$$

$$P_{e,l} = (I_s - I_o)(V_{C1} + V_{C2}) = (I_s - I_o)(V_o). \tag{15}$$

When the constraint of conservation of energy $P_s = P_o$, explicitly written as $V_s I_s = V_o I_o$, is applied, (14) and (15) can be rearranged into the convenient result of

$$P_{e,u} = P_{e,l} = P_{\phi,ss} \tag{16}$$

where the amount of power that needs to be exchanged between the upper set of capacitors $P_{e,u}$ and the lower set of capacitors $P_{e,l}$ to maintain voltage balance in steady state is equal. This value is denoted as $P_{\phi,ss}$ and is useful in the context of the DAHB capacitive power transfer mechanism as this is equivalent to the power required to be transferred over the inductive coupling.

The first noteworthy observation of the internal power transfer between capacitors is that $P_{\phi,ss}$ is always less than the output power P_o. The relationship between $P_{\phi,ss}$ and P_o is a function of the voltage conversion ratio [26]

$$\frac{P_{\phi,ss}}{P_o} = \frac{V_s - V_o}{V_s} = \frac{I_s - I_o}{I_s}. \tag{17}$$

For all allowable voltage conversion ratios, where $V_o < V_s$, $P_{\phi,ss}$ will always be less than P_o.

The second noteworthy observation of the internal power transfer between capacitors is that it is not necessary to move power within the set of upper capacitors (C_3 to/from C_4) or within the set of lower capacitors (C_1 to/from C_2) for a given output voltage and current condition. It is only necessary to move power between the set of upper capacitors and the set of lower capacitors (C_{1-2} to/from C_{3-4}) [28]. This is convenient as it allows for a relatively simple control methodology, as described in Section IV. It also allows for the grouping of the upper capacitors and lower capacitors into their respective sets which can simplify design and analysis, as described in the following section.

B. Stacked DAHB Module

The capacitive power transfer mechanism for each module is made of a single DAHB where the primary side services the set of upper capacitors C_{3-4} and the secondary side the set of lower capacitors C_{1-2}. Fig. 3 shows these connections. The required power transfer to maintain capacitor voltage balance in steady state $P_{\phi,ss}$ is implemented by transferring power across the inductive coupling of the DAHB. This allows for the exchange of power between the set of upper capacitors and the set of lower capacitors.

The power transferred across the inductive coupling P_ϕ can be described with

$$P_\phi = K V_{C,u} V_{C,l} \zeta \tag{18a}$$

$$K = \frac{N_p}{N_s 8 f_{\text{sw}} L_{\text{Lk}}} \tag{18b}$$

$$\zeta = \phi(1 - |\phi|) \tag{18c}$$

where $V_{C,u}$ is the sum of the voltages across the upper capacitors (C_{3-4}) and can be considered the voltage of the primary side of the DAHB. $V_{C,l}$ is the sum of the voltages across the lower capacitors (C_{1-2}) and can be considered the voltage of the secondary side of the DAHB. ϕ is the phase difference between switching cycles of the primary and secondary sides of the DAHB normalized to one-half the switching period. f_{sw} is the switching frequency. L_{lk}, N_p and N_s are the leakage inductance,

primary turns number, and secondary turns number, respectively, of the DAHB transformer. This article assumes N_p and N_s are always equal for a unity voltage transformation. Equations (18a)–(18c) can be rearranged into a single equation which is the typical approach for DAHB analysis [31]. However, it is separated here for both readability and to preserve a linear relationship between P_ϕ and ζ. Maintaining this relationship as linear simplifies control design, which is described in Section IV. ζ is ultimately the term that is used to control P_ϕ.

In the scope of the proposed topology the duty cycles of both the primary and secondary sides of the DAHB are considered to always be set to a static value of 0.5. The capacitance values are set to always be equal with $C = C_1 = C_2 = C_3 = C_4$. This has the implication that the capacitor voltages and DAHB balancing currents on each side of the DAHB are equal, explicitly written as $V_{C1} = V_{C2}$, $I_{C\phi1} = I_{C\phi2}$, $V_{C3} = V_{C4}$, and $I_{C\phi3} = I_{C\phi4}$. The individual capacitor currents due to the DAHB capacitive power transfer scheme can then be found as

$$I_{C\phi1} = I_{C\phi2} = K(V_{C3} + V_{C4})\zeta \tag{19a}$$

$$I_{C\phi3} = I_{C\phi4} = K(V_{C1} + V_{C2})(-\zeta). \tag{19b}$$

The total capacitor currents, including the currents due to the externalities I_s and I_o, are then

$$I_{C1} = I_{C2} = K(V_{C3} + V_{C4})\zeta + I_s - I_o \tag{20a}$$

$$I_{C3} = I_{C4} = K(V_{C1} + V_{C2})(-\zeta) + I_s. \tag{20b}$$

Finally, the dynamic equations for the four capacitor voltages can then be found considering $C(dV_c/dt) = I_c$ and (20a)–(20b) as

$$\frac{dV_{C1}}{dt} = \frac{dV_{C2}}{dt} = \frac{1}{C}K(V_{C3} + V_{C4})\zeta + \frac{1}{C}(I_s - I_o) \tag{21a}$$

$$\frac{dV_{C3}}{dt} = \frac{dV_{C4}}{dt} = \frac{1}{C}K(V_{C1} + V_{C2})(-\zeta) + \frac{1}{C}I_s. \tag{21b}$$

As described previously, the capacitor currents due to the capacitive power transfer mechanisms must cancel the capacitor currents due to externalities I_s and I_o. When this condition is achieved the values for dV_{C1-4}/dt become zero. I_s and I_o are determined by the load condition and voltage conversion ratio and are therefore not controlled. Instead, ζ can be controlled to a value such that I_s and I_o are cancelled where $P_\phi = P_{\phi,ss}$. When this is the case, the relationship between ζ and I_o becomes

$$I_o = \zeta K V_s. \tag{22}$$

Notably, the output current I_o has no dependency on the output voltage V_o, instead only depending on the input voltage V_s, DAHB circuit parameters K, and control variable ζ. The output of each phase-modular stacked DAHB acts as a current-source, and when multiple are configured together as an ac interface, they act as a quasicurrent-source inverter. This is convenient for grid-following applications where the grid voltage is defined and the role of the inverter is to only provide current. The stacked DAHB as an ac interface is described in the following section.

III. Performance Characteristics

A. Ac Interface Operating Point Variations

The operating points that each stacked DAHB module traverses over one cycle of the grid can have significant variation. It is necessary to understand the range of operating points for component dimensioning. First, the output voltage V_o and current I_o of the stacked DAHB interfaced with a single phase of the grid can be defined as

$$V_o(\theta) = \tfrac{V_{\text{dc}}}{2} + \sqrt{2}V_{\text{grid}}\sin(\theta) \tag{23}$$

$$I_o(\theta) = I_{\text{grid}}\sin(\theta - \beta) \tag{24}$$

where V_{grid} is the RMS value of the line-to-neutral grid voltage and I_{grid} is the peak value of the line current. V_{dc} is the dc link voltage (equivalent to V_s in the previous analysis) and is considered to be a static value. It is assumed that the output voltage V_o averaged over one cycle of the grid, when referenced to the negative dc-link, is one-half the dc-link voltage. This is represented by the dc offset of $V_{\text{dc}}/2$ in (23). β is the phase difference between the grid current and voltage.

θ is the instantaneous value of the phase of the grid. In the context of this analysis, θ is swept with discrete values between $0 \leq \theta \leq 2\pi$ (one cycle of the grid). Each discrete value of θ can be considered a quasisteady-state operating point as the converter's switching frequency is much greater than the grid frequency.

$V_o(\theta)$ and/or $I_o(\theta)$ with a static value of V_{dc} of (23)–(24) can be can be substituted into (17) to give the required $P_{\phi,ss}$ over one cycle of the grid as

$$P_{\phi,ss}(\theta) = P_o(\theta)\frac{V_{\text{dc}} - V_o(\theta)}{V_{\text{dc}}} \tag{25}$$

where $P_o(\theta)$ is the instantaneous output power of one phase of the stacked DAHB modules and is equivalent to $P_o(\theta) = I_o(\theta)V_o(\theta)$. This aligns with the PPP theory of Section II-A, specifically (17). When averaged over the cycle of the grid, the ratio of P_ϕ/P_o is equal to \nicefrac12. This is true for all dc link voltages, grid voltages, and power levels, as long as the average grid voltage is equal to $1/2$ the dc link voltage [explicitly written as the $V_{\text{dc}}/2$ term in (23)]. In some applications it may be advantageous to shift the average grid voltage from $V_{\text{dc}}/2$ to another value, and for these applications the ratio of averaged processed power to output power P_ϕ/P_o will be equal to $1 - V_0/V_{\text{dc}}$, where V_0 is the average grid voltage.

Given the two equations for P_ϕ of (18a)–(18c) and (25) and the requirement of $P_\phi = P_{\phi,ss}$, the anticipated value of $\zeta(\theta)$ given ideal circuit operation can be calculated over one cycle of the grid as

$$\zeta(\theta) = I_o(\theta)\frac{K}{V_{\text{dc}}} \tag{26}$$

where $\zeta(\theta)$ is highly dependent on K, the DAHB parameters. It is not dependent on the output voltage $V_o(\theta)$ and aligns with (22), supporting the usefulness of this topology in grid following applications.

Fig. 4 shows the instantaneous grid parameters and their associated internal operating points of the stacked DAHB over

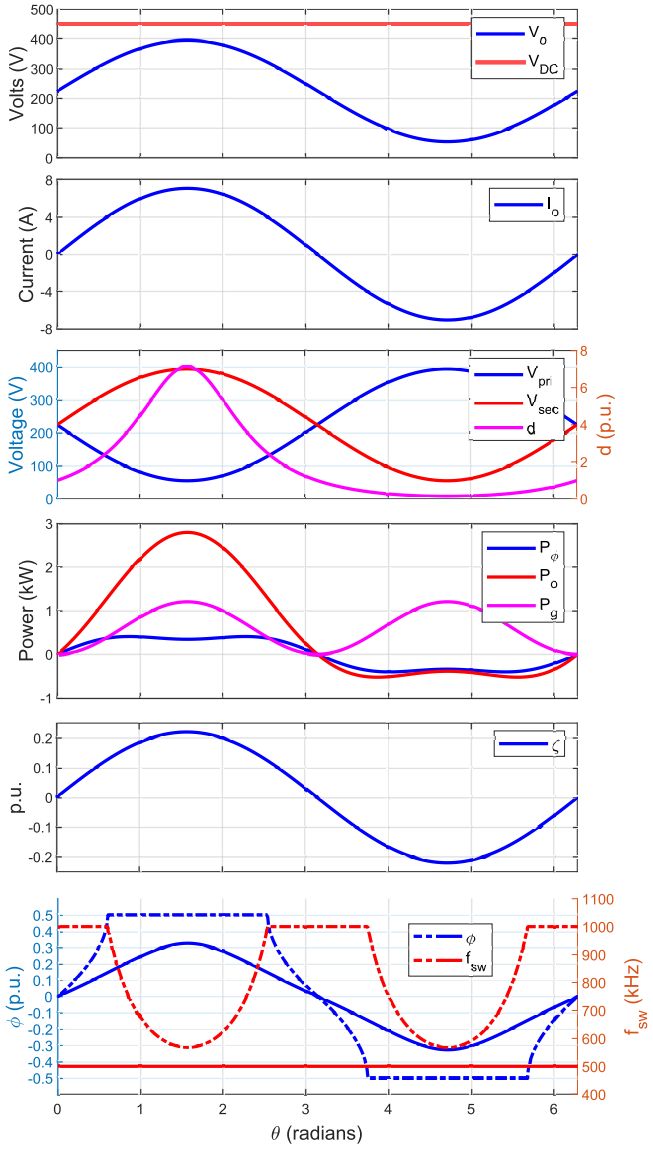

Fig. 4. Operating points of a single-phase module stacked DAHB with parameters $L_{\text{Lk}} = 3.5\ \mu\text{H}$, $V_{\text{grid}} = 120\ V_{l-n}$, $I_{\text{grid}} = 5.7\ A_{\text{rms}}$, and $V_{\text{dc}} = 450$ V over one cycle of the grid. P_g is the instantaneous power provided to the grid by a single phase of the inverter. ζ of the constant f_{sw} scheme is equivalent to $\zeta' f_{\text{sw}}$ of the variable frequency scheme. In the bottom plot, solid lines represent values corresponding to the constant f_{sw} scheme and dashed lines represent those belonging to the variable f_{sw} scheme.

one cycle of the grid. It can be seen that the DAHB primary to secondary voltage ratio d varies between extremes over the cycle of the grid. This is undesirable operation for DAHBs as deviating from a unity ratio (after the voltage transformation of the transformer turns ratio is applied) will result in excessively high currents and potential departure from the soft-switching region [32].

Using the techniques described in Kheraluwala et al.'s [33] work the soft-switching boundaries of ϕ as a function of ϕ and d for a DAHB under ideal operating conditions can be defined as

$$1 - 2|\phi| < \frac{V_{\text{sec}}}{V_{\text{pri}}} < \frac{1}{1 - 2|\phi|} \tag{27}$$

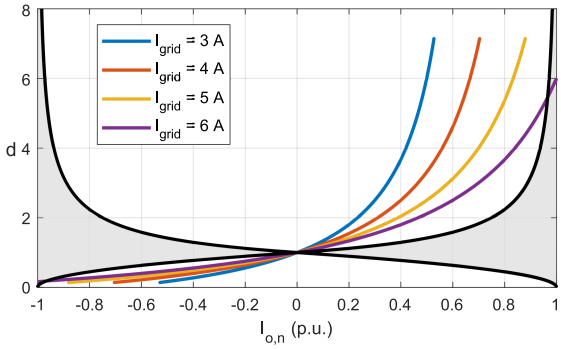

Fig. 5. Operating points the constant f_{sw} DAHB traverses over one cycle of the grid for different grid currents (colored lines) as they relate to the DAHB soft-switching boundaries (gray shaded region).

where the leftmost portion of the inequality represents the soft-switching boundary for the primary side switches and the rightmost represents the boundary for the secondary side switches. This soft-switching region can be visualized in Fig. 5 along with the path of operating points the constant f_{sw} stacked DAHB takes over one cycle of the grid. The same DAHB parameters used to generate Fig. 4 are used here. $I_{o,n}$ is I_o normalized to the maximum allowable output current the stacked DAHB can provide before it saturates.

It can be seen that this constant f_{sw} stacked DAHB always operates outside of the soft-switching region aside from from the relatively small portion of the grid cycle when the primary and secondary voltages are equal. Soft-switching has many benefits, such as lower semiconductor stresses, reduced switching losses, and improved electromagnetic interference performance [34], [35], and it is therefore advantageous to maintain the ability to soft-switch if desired. The following section describes a method to maintain soft-switching over the grid cycle by making the switching frequency of the DAHB dynamic.

B. *Variable f_{sw} Soft-Switching Stacked DAHB*

As shown in (27), Fig. 5, and in Donckere et al.'s [32] work, soft-switching can be maintained for all values of primary to secondary voltage ratio d if ϕ, the normalized phase difference between opposing sides of the DAHB, is held at a static value of either 0.5 or -0.5. For values of $|\phi| \leq 0.5$, the allowable region of d for maintaining soft-switching decreases. It is important to note that circuit nonidealities will affect the soft-switching region. The effective drain-source capacitance of the FETs will shrink the soft-switching region. Decreasing the magnetization inductance L_{mag} to leakage inductance L_{Lk} ratio will expand the soft-switching region. These effects are described in Kheraluwala et al.'s [33] work and can be used to dimension the transformer. For a generalized approach, it is advantageous to keep ϕ as close as possible to its extremes of ± 0.5 to maintain the widest soft-switching bounds over the cycle of the grid.

This can be done by adjusting the switching frequency f_{sw} to achieve the desired value of P_ϕ while keeping ϕ at or as close as possible to its extremes of ± 0.5. This is atypical operation for DAHBs but has been described previously in [36] and [37]. This variable frequency scheme is first expressed by adjusting

P_ϕ, K, and ζ in (18a)–(18c) to reflect that f_{sw} is dynamic

$$P_\phi = K' V_{C,u} V_{C,l} \zeta' \tag{28a}$$

$$K' = \frac{N_p}{N_s 8 L_{\text{lk}}} \tag{28b}$$

$$\zeta' = \frac{\phi(1-|\phi|)}{f_{\text{sw}}} \tag{28c}$$

by removing f_{sw} from the K term and inserting it into the ζ term to get K' and ζ'. The $'$ denotes parameters of the variable frequency environment. It can be seen that there exists a range of combinations of f_{sw} and ϕ that will produce a single value of ζ'. However, not all combinations of f_{sw} and ϕ for a given value of ζ' and d will be inside the soft-switching region.

One way to stay within the soft-switching region is to always operate at the greatest possible value of $|\phi|$ (where $\phi \leq 0.5$) for a given allowable switching frequency range. Mathematically, this can be expressed as

$$f_{\text{sw}} = \begin{cases} f_{\text{sw,max}} & \text{for} \quad |\zeta'| \leq \zeta'_x \\ (\phi_{\max}(1-\phi_{\max}))/|\zeta'| & \text{for} \quad \zeta'_x < |\zeta'| < \zeta'_y \\ f_{\text{sw,min}} & \text{for} \quad |\zeta'| \geq \zeta'_y \end{cases} \tag{29a}$$

$$\phi = \begin{cases} -\phi_{\max} & \text{for} \quad \zeta' \leq -\zeta'_x \\ (1-\sqrt{1-4 f_{\text{sw,max}} \zeta'})/2 & \text{for} \quad 0 \leq \zeta' \leq \zeta'_x \\ (-1+\sqrt{1+4 f_{\text{sw,max}} \zeta'})/2 & \text{for} \quad -\zeta'_x \leq \zeta' \leq 0 \\ \phi_{\max} & \text{for} \quad \zeta' \geq \zeta'_x \end{cases} \tag{29b}$$

where ζ'_x and ζ'_y are crossover points that define regions of constant or variable ϕ and f_{sw}

$$\zeta'_x = \frac{(\phi_{\max}(1-\phi_{\max}))}{f_{\text{sw,max}}} \tag{30}$$

$$\zeta'_y = \frac{(\phi_{\max}(1-\phi_{\max}))}{f_{\text{sw,min}}}. \tag{31}$$

$\phi_{\max}$ should be held at its maximum allowable value of 0.5 but is presented symbolically for reference. $f_{\text{sw,min}}$ and $f_{\text{sw,max}}$ are the minimum and maximum allowable switching frequencies, respectively, and are hardware defined parameters. Values of ζ' beyond $\zeta' \geq \zeta'_y$ represent an an area of operation where the output power of the stacked DAHB is saturated and these values of ζ' cannot be actuated. A more convenient visualization of the expressions of (29a)–(31) can be seen in Fig. 6, where ϕ and f_{sw} are saturated at their respective limits as a function of ζ'.

Fig. 4 shows the values of ϕ and f_{sw} over one cycle of the grid for a hypothetical DAHB with with $f_{\text{sw,max}} = 1$ MHz. Fig. 7 shows the operating point path that this variable frequency scheme of takes over one cycle of the grid in the context of the soft-switching boundaries of the DAHB. It can be seen that operation within the soft-switching region can be maintained over this grouping of power levels when interfacing the stacked DAHB with an ac grid. Section IV describes a closed-loop control scheme that can be used to interface with the ac grid for both the variable frequency and constant frequency schemes.

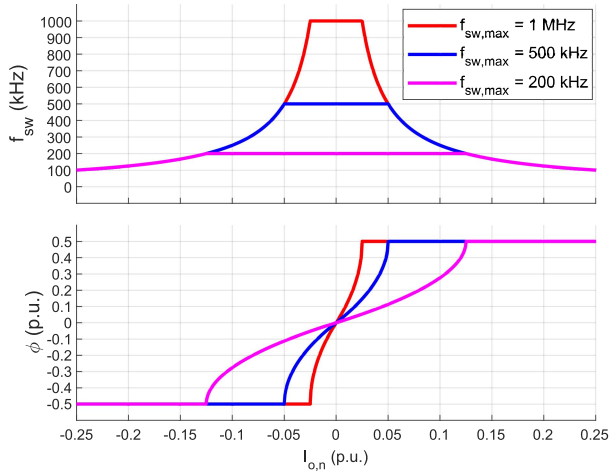

Fig. 6. Switching frequency f_{sw} and normalized phase difference ϕ as a function of the normalized output current $I_{o,n}$ for different values of $f_{\text{sw,max}}$.

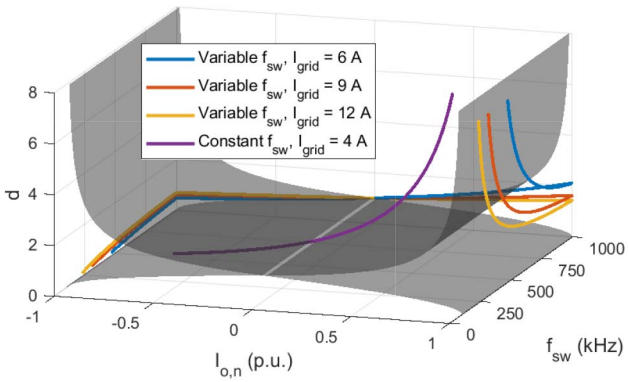

Fig. 7. Trajectories of both the variable and constant f_{sw} schemes over one cycle of the grid as they relate to the soft-switching boundaries of the DAHB. The soft-switching region is between the two black planes.

C. Design Considerations

1) $f_{\text{sw}}L_{lk}$ and C Dimensioning: The primary component that defines the performance of the stacked DAHB module is the transformer. Specifically, the leakage inductance-switching frequency product $f_{\text{sw}}L_{\text{Lk}}$ determines the range of power that can be transferred over the inductive coupling P_ϕ, with this relationship described in (18a) and (28a). As shown in (17), there is a direct relationship between P_ϕ and the output power P_o of a stacked DAHB P_o. Algebraic manipulation of (22) provides the minimum $f_{\text{sw}}L_{\text{Lk}}$ product required for a given maximum output current $I_{o,\max}$ as

$$(f_{\text{sw}}L_{\text{Lk}})_{\min} = \frac{N_p V_{\text{dc}}}{8 N_s I_{o,\max}}. \tag{32}$$

Notably, the grid voltage does not influence the dimensioning of the $f_{\text{sw}}L_{\text{Lk}}$ product. The individual values of f_{sw} and L_{Lk} can then be found given the converter's practical hardware limitations. The second set of components that needs to be dimensioned is the DAHB capacitors (C_{1-4} in Fig. 3). These capacitors are first responsible for absorbing the leakage inductance current ripple I_{Lk} and can be sized for this role using typical DAHB design techniques [38]. In this application, these capacitors also

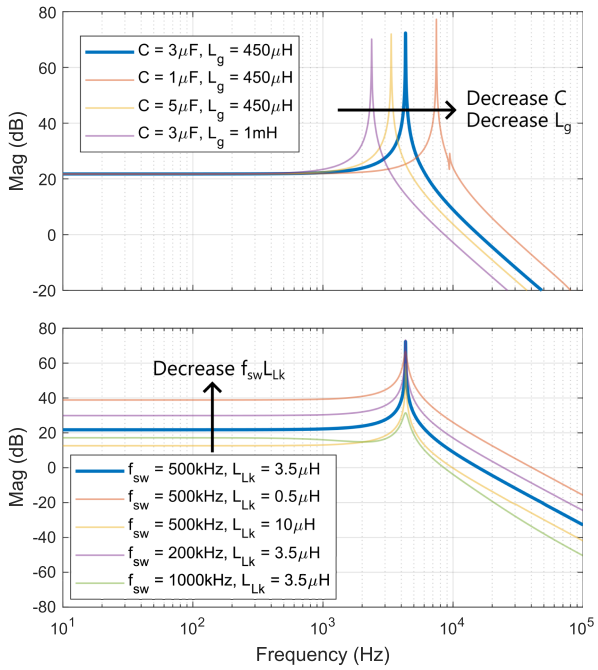

Fig. 8. Open loop bandwidth of the stacked DAHB for varying values of f_{sw}, C_{1-4}, and grid inductance L_g. The transfer function is defined as $^{I_o}/_{\zeta}$.

get charged and discharged with the varying output voltage V_o over the cycle of the grid. This has implications on the frequency response of the converter, as described in the following section.

2) Frequency Response: Both the $f_{\text{sw}}L_{\text{Lk}}$ product and capacitances C_{1-4} have significant effects on shaping the open-loop bandwidth of the converter. The open loop bandwidth is found using a transfer defined as $^{I_o}/_{\zeta}$. For this grid following inverter application, ζ is the input control variable and the current I_o is the output. The frequency response is found using a PLECS simulation and can be seen in Fig. 8.

The $f_{\text{sw}}L_{\text{Lk}}$ product determines P_ϕ as a function of ζ. As shown in (22), for a given value of ζ, a lower $f_{\text{sw}}L_{\text{Lk}}$ product results in higher I_o and vice versa. Therefore, a lower $f_{\text{sw}}L_{\text{Lk}}$ product will increase the open-loop gain and a higher $f_{\text{sw}}L_{\text{Lk}}$ product will decrease the open-loop gain. This can be seen in Fig. 8 where the $f_{\text{sw}}L_{\text{Lk}}$ product is varied and the open-loop bandwidth measured. It can be seen that the converter exhibits a frequency response similar to that of an *LC* filter and that the $f_{\text{sw}}L_{\text{Lk}}$ product only changes the overall gain and does not affect the cutoff frequency.

The cutoff frequency is largely a function of the impedance of the grid and the capacitance C_{1-4} value. This is also shown in Fig. 8 where both the value of C_{1-4} and the grid impedance are varied while the $f_{\text{sw}}L_{\text{Lk}}$ product is held constant. It can be seen that increasing the value of C_{1-4} and/or the inductance of the grid L_{grid} lowers the cutoff frequency, which is in line with the frequency response of an LC filter. As it is not practically feasible to control the impedance of the grid, the only method for controlling the cutoff frequency is through the value of C_{1-4}.

3) Component Mismatch: The analysis presented assumes that C_{1-4} all have equal values and that the L_{Lk} of the transformer for each stacked DAHB module is equal. In practical implementations component mismatch is to be expected and it is important to understand how it can impact the converter's performance.

As shown in (19a)–(21b), the capacitance values (if sufficiently sized according to the guidelines of Section III-C1) do not affect the steady state performance of the converter. Instead, they only effect the transient performance of the converter, specifically, during transient steps in the output voltage. Equations (21a)–(21b) can be modified for the case of $C_1 \neq C_2 \neq C_3 \neq C_4$ as

$$\frac{dV_{C1}}{dt} = \frac{1}{C_1}K(V_{C3}+V_{C4})\zeta + \frac{1}{C}(I_s - I_o) \tag{33a}$$

$$\frac{dV_{C2}}{dt} = \frac{1}{C_2}K(V_{C3}+V_{C4})\zeta + \frac{1}{C}(I_s - I_o) \tag{33b}$$

$$\frac{dV_{C3}}{dt} = \frac{1}{C_3}K(V_{C1}+V_{C2})(-\zeta) + \frac{1}{C}I_s \tag{33c}$$

$$\frac{dV_{C4}}{dt} = \frac{1}{C_4}K(V_{C1}+V_{C2})(-\zeta) + \frac{1}{C}I_s. \tag{33d}$$

Here, it can be seen that larger capacitors will charge slower than smaller capacitors and vice versa, and this will cause a degree of voltage level mismatch during the transient state that scales with the mismatch in capacitance values.

Mismatch in L_{Lk} values between stacked DAHB modules manifest as different relationships between ζ and I_o for different modules according to (18a)–(18c). Errors in the I_o of each module represent an additional burden for the controllers of Section IV, specifically the zero-sequence controller, and the tolerance to mismatch of L_{Lk} values will be set by the controllers ability to compensate for these mismatches.

IV. Control

The control scheme of the proposed inverter can be seen in Fig. 9. The three-phase grid current $I_{o,abc}$, three-phase output voltages $V_{o,abc}$, and the dc link voltage V_{dc} are measured. All voltages are measured with respect to the negative dc link. As this is a grid-following converter the only parameters that the controller actuates are the three-phase grid currents.

First, a phase-locked-loop provides the value of the instantaneous phase θ of the grid. This allows for the three-phase grid and voltage measurements to be transformed from the *abc* to the *dq*0 spaces. The measured zero voltage $V_{o,0}$ is used in an outer PI controller to provide the reference zero-current $I^*_{o,0}$ that the inner controller tries to actuate to achieve a zero-voltage equal to one-half the dc link voltage. The reference d and q currents, $I^*_{o,d}$ and $I^*_{o,q}$, respectively, are manually set. Similar control schemes may also use an additional outer-loop PI controller to set $I^*_{o,d}$ to achieve a desired dc link voltage [39]. In the scope of the proposed, the dc-link voltage is considered to always be set by an external dc source and this additional outer-loop controller is not included.

The inner-loop of the controller consists of three individual PI controllers, one for each component of the grid current in the *dq*0 space. The output of the I_{dq0} PI controllers are passed

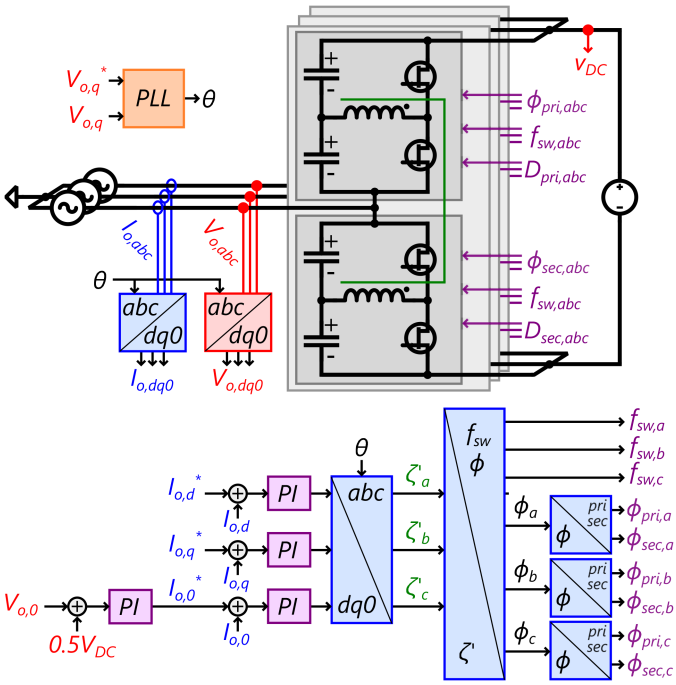

Fig. 9. Control topology of the proposed inverter.

through an inverse Park transformation to give values of ζ' in the *abc* reference frame.

These values of ζ'_{abc} are then converted into values of ϕ_{abc} and $f_{\mathrm{sw},abc}$ which can be actuated by the hardware. For the variable frequency case, ζ'_{abc} is converted into values of $f_{\mathrm{sw},abc}$ and ϕ_{abc} according to (29a)–(31). The constant f_{sw} case uses these same equations but the bounds of f_{sw} are set such that $f_{\mathrm{sw,min}} = f_{\mathrm{sw,max}} = f_{\mathrm{sw,constant}}$.

Practical controllers cannot implement negative values of ϕ. Positive values of ϕ correspond to phase delay of the secondary side of the DAHB. Negative values of ϕ correspond to a phase delay of the primary side of the DAHB. This is explicitly written as

$$\phi_{\mathrm{pri}} = \begin{cases} 0 & \text{for} \quad \phi > 0 \\ \phi & \text{for} \quad \phi \leq 0 \end{cases} \tag{34a}$$

$$\phi_{\mathrm{sec}} = \begin{cases} \phi & \text{for} \quad \phi > 0 \\ 0 & \text{for} \quad \phi \leq 0 \end{cases} \tag{34b}$$

where ϕ_{pri} and ϕ_{sec}, the individual phase delays for the primary and secondary sides of the DAHB, respectively, can be practically actuated. The final terms, $D_{\mathrm{pri},abc}$ and $D_{\mathrm{sec},abc}$, are the duty cycles in the *abc* frame of the primary and secondary sides and are set to a static value of 0.5.

V. Comparison

The proposed converter is first compared to current state-of-the-art converters with respect to hardware, control, and performance characteristics in grid-tied grid-following applications. A comparison in component quantities of the proposed to traditional two-level [39], T-type [40], and three-level neutral-point-clamped (NPC) [41] three-phase inverter topologies can be found in Table I. These quantities consider the two-level, T-type, and NPC topologies to all have an additional *LC* filter at the grid connection. The proposed topology does not need this additional *LC* filter as the output at the grid connection is already filtered by the leakage inductance L_{Lk} and capacitances C_{1-4}.

TABLE I
Component Quantity Comparison

Topology	Magnetics	Capacitors	Semiconductors
Two-level [39]	3	4	6
T-type [40]	3	9	18
Three-level NPC [41]	3	9	18
Proposed	3	12	12

The proposed topology controls the output current of each phase through control variable ζ as there is a predictable and linear relationship between ζ and I_o, as shown in (22). This is in contrast to the two-level, T-type, and three-level NPC, where the control variables define the output voltage [42], [43], and an additional complication is then necessary to relate the output voltage to output current. This relationship can depend on a multitude of things such as output filter parasitics and parameters of the grid [44], which are often not well-defined. Therefore, the practical controllability of the proposed topology, especially in grid-following applications, can be more straightforward than the other topologies. Theoretical limitations on controllability of the proposed topology can be found in Jahnes and Preindl's [28] work.

Performance characteristics of these selected topologies can then be compared. The proposed topology is the only topology with PPP properties, which can be leveraged to improve overall efficiency. All four topologies are capable of soft-switching without any additional auxiliary circuits given a suitable variable frequency range [39], [45], [46], which can give improvements for both light-load and full-load efficiencies. However, the inherent current output of the proposed topology can potentially offer improved reliability over grid-following voltage-source inverters. An improper control calculation of a voltage-source inverter can result in potentially damaging amounts of currents, whereas for the proposed topology the worst outcome from an erroneous control calculation is the maximum allowable current being actuated, which in a proper design the hardware should be sized to handle.

Finally, the topological family that this proposed inverter belongs to can be compared with the modular multilevel converter (MMC) and its variants. The MMC requires extra attention to maintain capacitor voltage balance as its output frequency approaches zero [47] for dc/dc operation. MMC submodule power transfer schemes such as those presented in [48], [49], [50], [51], and [52] can be implemented to maintain capacitor voltage balance as output frequency approaches zero and the inverter becomes a dc/dc converter. The authors in [48] and [49] moved power horizontally between phase legs but not vertically between upper and lower arms, the authors in [50] and [51] moved power vertically between upper and lower arms but not

horizontally across phase legs, and Chen et al. [52] moved power in both dimensions. They also all utilize a form of a DAB to execute the power transfer.

It is important to note that these types of schemes differ from the proposed. The most significant difference is that these MMCs have static level voltages over the cycle of the grid. In Diab et al.'s [48] work, this is leveraged to keep the power transfer DAHBs operating in the soft-switching region as their voltage transformation ratios are always 1:1 and soft-switching is maintained for any load condition. In the proposed, the level voltages vary over the cycle of the grid, which is different from MMCs and other multilevel topologies, and as a result the variable f_{sw} scheme of Section III-B is employed to maintain soft-switching.

The second significant difference is that these systems are all built around an existing MMC (active components), and the power transfer mechanisms are responsible for improving the performance of the MMC, not defining it. In the proposed, each phase leg of the inverter is built around a set of series capacitances (passive components), and the power transfer mechanisms define the performance. This results in less overall switching device VA requirements in the proposed system than the aforementioned MMC derived systems. The total switching device VA requirements of a single phase-leg of an HB-based MMC S_{MMC} (not including the additional balancing power transfer mechanisms of [48], [49], [50], [51], and [52]) can be found to be

$$S_{\text{MMC}} = 4I_o V_s \tag{35}$$

where I_o is the output current of the phase-leg and V_s is the dc-link voltage. This is found considering each phase leg must be sized to carry I_o and the voltage stress of each submodule is equal to the dc-link voltage divided by the number of submodules in an arm. In the systems of [48], [49], [50], [51], and [52] S_{MMC} can be considered the lower bound on the switching device VA requirements as it does not include the additional VA requirements of their respective balancing mechanisms. For the proposed system, the switching device VA requirements can be found to be

$$S_{\text{Manh}} = 4I_\phi V_s \tag{36}$$

where I_ϕ is the effective current transferred over the inductive coupling by the transformer into/from each HB of the DAHB, and is the current that the FETs of each HB must be sized to handle. I_ϕ can be found with

$$I_{\phi,p} = \frac{P_\phi}{V_{\text{pri}}} = I_o \frac{V_s - V_o}{V_s} \tag{37a}$$

$$I_{\phi,s} = \frac{P_\phi}{V_{\text{sec}}} = I_o \frac{V_o}{V_s} \tag{37b}$$

where $I_{\phi,p}$ and $I_{\phi,s}$ are the effective primary and secondary HB transformer currents, respectively. As shown in (17), P_ϕ will change over the cycle of the grid but will always be less than P_o. The worst-case scenario of I_ϕ occurs at the extremes of the voltage conversion ratio where $P_\phi/P_o = 1$ and $I_\phi = I_o$. This makes S_{Manh} equal to S_{MMC}, however, S_{MMC} does not include the additional VA requirements of the balancing system. The proposed topology is intrinsically balanced, and S_{Manh} includes all switch VA stresses. For this reason, the VA requirements of the proposed topological framework will at worst be equal to that of the MMC and will always be less than that of the MMC with additional active balancing links.

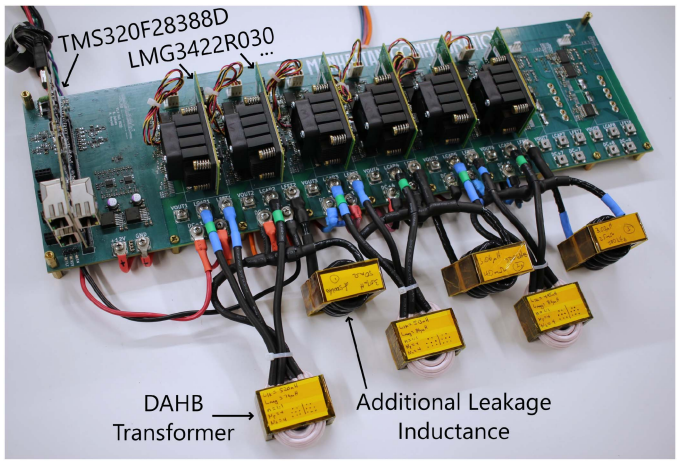

Fig. 10. Hardware prototype used for validation of the three-phase PPP inverter.

VI. Experimental Prototype

The experimental prototype used to validate the proposed inverter can be seen in Fig. 10. Each half-bridge is made from Texas Instruments LMG342xR050 integrated GaN FETs. The value of each capacitor within the stacked DAHB (C_{1-4} in Fig. 3) is 6 μF and TDK Ceralink ceramic capacitors are used in this application for their high ripple current handling capabilities. Due to the inherently balanced nature of this topology and the high switching frequency of the experimental prototype, it is not necessary to use large capacitances or capacitances that are closely matched in value, as described in Section III-C3, to maintain functionality.

The transformer is composed of two Ferroxcube E43/10/28 3F36 cores in an EE configuration along with four primary and four secondary turns of 2625/44 Litz wire. The resulting magnetization inductance L_{mag} and leakage inductance are 65 and 0.42 μH, respectively. An additional inductance of 3 μH is placed in series with the transformer to give a total leakage inductance L_{lk} of 3.5 μH. It is important to note that this additional leakage inductance is not fundamentally necessary and that a more optimized implementation can exclusively rely on the intrinsic leakage inductance of the transformer. A low leakage inductance transformer was chosen for this application so the total leakage inductance could be more easily experimentally varied.

A Texas Instruments TMS320F28388D microcontroller is used to actuate the gate PWMs, read the sensors, and execute the control with an update frequency of 50 kHz. The bandwidth of the current and voltage sensors are limited to 100 kHz, below the allowable switching frequency range, so neither the fixed nor variable switching frequencies noticeably effect control measurements. The zero voltage controller uses PI gains of

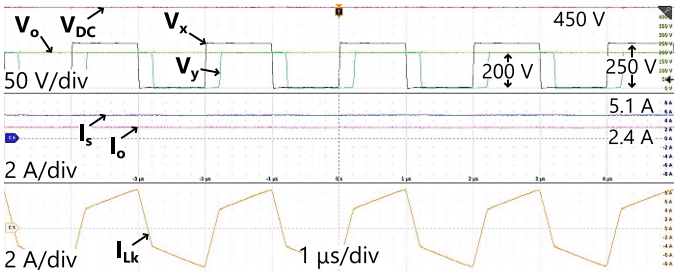

Fig. 11. Open-loop transient results with 450 $V_{\rm dc}$ link, $f_{\rm sw}$ of 500 kHz, $\phi = 0.2$, and V_o of 200 V.

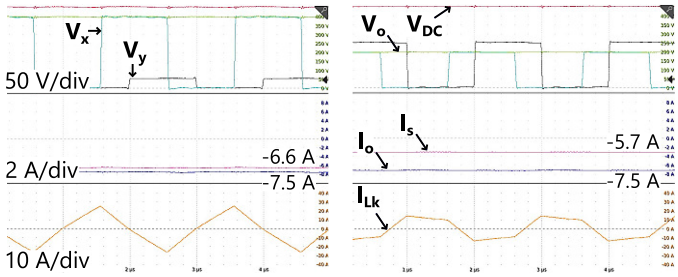

Fig. 12. Open-loop transient results with 450 $V_{\rm dc}$ link, $f_{\rm sw}$ of 500 kHz, and $\phi = -0.4$. V_o is set by an external dc power supply to 400 V (left) and 200 V (right).

$k_{p,zs} = 1$ and $k_{i,zs} = 3$ for the proportional and integral gains, respectively. The three $dq0$ current PI controllers have identical gains of $k_{p,\zeta} = 0.001$ and $k_{i,\zeta} = 1$. These gain values were found empirically and limit the bandwidth in the $dq0$ space to roughly 2Hz, as will be shown in the following section. It is important to note that this does not reflect the maximum grid frequency this inverter can interface with. Using the techniques described in Section III-C2, the open-loop bandwidth of the experimental prototype, when operating with a grid that has an inductance of 450 μH, can be found as roughly 4.5 kHz. This places an upper bound on the grid frequency this inverter can interface with.

VII. Results

This section details the experimental results of the proposed inverter. All ac results are found when interfacing with a 450 $V_{\rm dc}$ link and 208 V_{l-l} 60 Hz grid that has an inductance of $L_g = 450$ μH. Both constant $f_{\rm sw}$ and variable $f_{\rm sw}$ schemes have been experimentally validated. All output grid voltage V_o measurements are taken with respect to the negative dc link. A Tektronix MSO58 oscilloscope with IMDA power analyzer software, P5200A voltage probes, and TCP0030A current probes are used for all measurements unless otherwise stated. The inductor current $I_{\rm Lk}$ refers to the current measured through the series leakage inductance of the transformer. $I_{\rm dc}$ is the measured dc link current.

A. Switching Waveforms

The switching waveforms of the single stacked DAHB can be seen in Figs. 11 and 12. These results are found with the stacked DAHB configured as an open-loop dc/dc converter with a 450 $V_{\rm dc}$ link and $f_{\rm sw}$ of 500 kHz. An additional regenerative dc power supply is connected across the output V_o and is used to set the output voltage. Fig. 11 shows a switching waveform with where constant value of $\phi = 0.3$ is actuated with an output voltage $V_o = 200$ V.

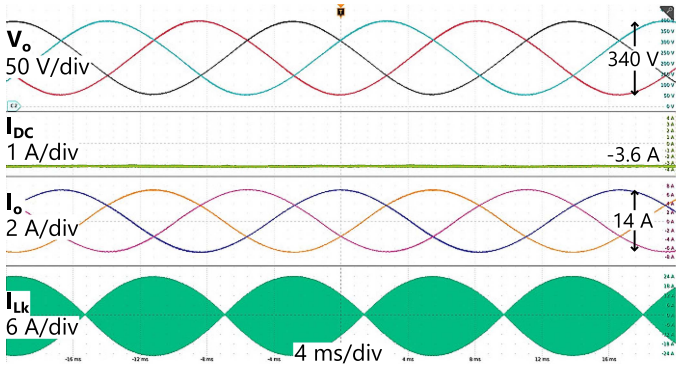

Fig. 13. Three-phase grid current I_o and voltage V_o, inductor current $I_{\rm Lk}$, and DC link current $I_{\rm dc}$ for constant $f_{\rm sw}$ control with $I_d = 7$ A and $I_q = 0$ A.

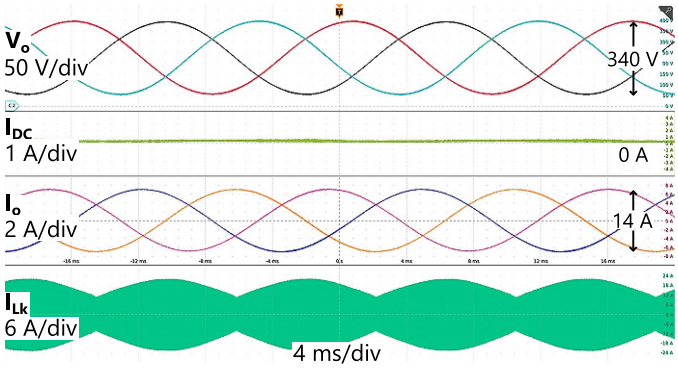

Fig. 14. Three-phase grid current I_o and voltage V_o, inductor current $I_{\rm Lk}$, and DC link current $I_{\rm dc}$ for constant $f_{\rm sw}$ control with $I_d = 0$ A and $I_q = 7$ A.

Typical DAHB operation can be noted in the inductor current and transformer voltages. Proper actuation of ϕ can be seen in the phase difference between V_x primary and V_y secondary nodes. Fig. 12 shows two test conditions, both with $\phi = -0.4$, but with different output voltages. It can be seen that the output current I_o is the same for both values of output voltage, which demonstrates the current source functionality of the proposed topology.

B. Constant $f_{\rm sw}$ Scheme

Experimental results of the constant $f_{\rm sw}$ control scheme can be seen in Figs. 13–18. All results in this section are found using a $f_{\rm sw}$ of 500 kHz. Figs. 13 and 14 show the proposed inverter providing 7 A of I_d and 7 A of I_q, respectively. Minimal distortion can be noted in the grid current and voltage waveforms. The dc current is also free of any strong harmonics. For the exclusively real power case of Fig. 13, the envelope of the inductor current pinches off to zero because the current provided to the grid at the zero crossing of the voltage and current is zero and the DAHB primary and secondary voltages are equal. This condition does not occur for the exclusively reactive power case of Fig. 14

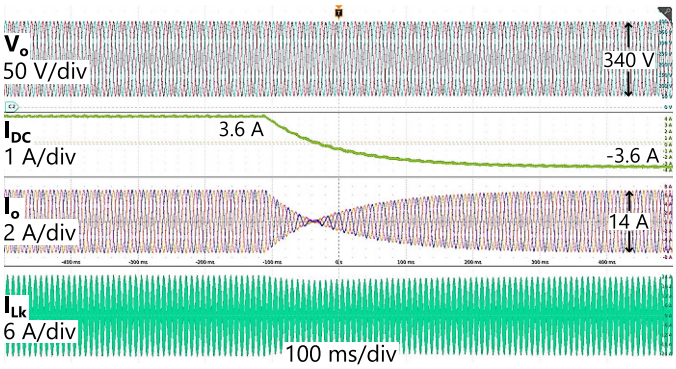

Fig. 15. Three-phase grid current I_o and voltage V_o, inductor current I_{Lk}, and DC link current I_{dc} for constant f_{sw} control with a –5–5 A I_d step.

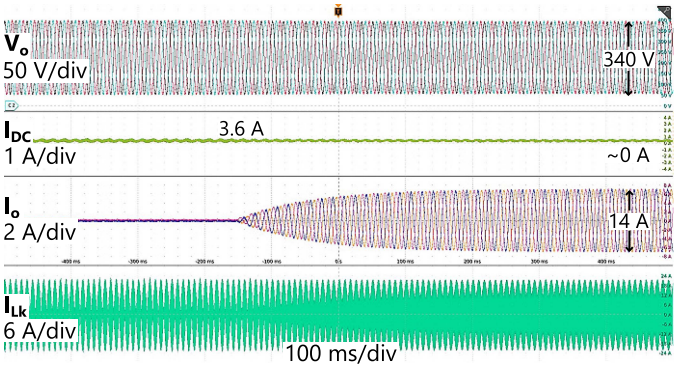

Fig. 16. Three-phase grid current I_o and voltage V_o, inductor current I_{Lk}, and DC link current I_{dc} for constant f_{sw} control with 0–7 A I_q step.

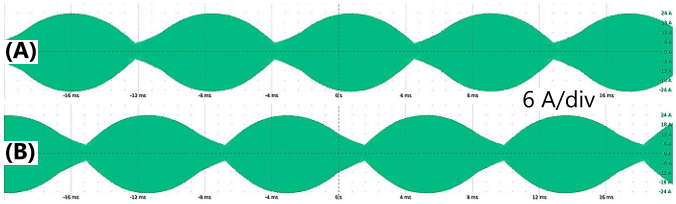

Fig. 17. Inductor current envelope for $I_d = 6$ A and (A): $I_q = -4$ A and (B): $I_q = 4$ A.

where the inductor current never pinches off to zero. Fig. 17 shows how the envelope of the inductor current changes with different proportions of I_d and I_q .

Figs. 15 and 16 show real and reactive power steps, respectively, of the proposed inverter. Bidirectional functionality is demonstrated. A rise time in d and q current of roughly 200 ms can be noted, which corresponds to a closed-loop bandwidth of 2 Hz in the $dq0$ space. It can be seen that the magnitude of the inductor current envelope during these steps does not change with the average output power. This is disadvantageous for efficiency as excessive currents during low power operation will drive excessive loss. The variable f_{sw} scheme presented in the next section takes steps to mitigate this.

Lastly, Fig. 18 shows the efficiency and THD-F measurements of the proposed inverter operating under the constant f_{sw} scheme. The maximum power is limited to 1.8 kW as this is the power level where the associated peak output current will

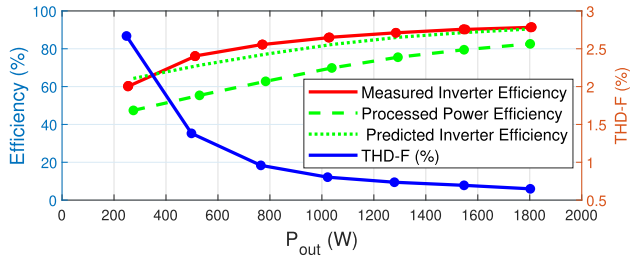

Fig. 18. Measured and predicted overall inverter efficiency and processed power efficiency of the constant f_{sw} scheme with grid current THD-F results. P_{out} is the total three-phase power provided to the grid.

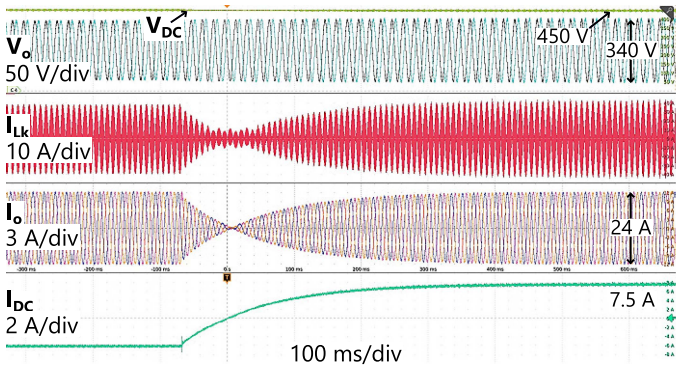

Fig. 19. Three-phase grid current I_o and voltage V_o, inductor current I_{Lk}, DC link voltage V_{dc}, and DC link current I_{dc} for variable f_{sw} control with a 14 to –14 A I_q step.

saturate ϕ. The processed power efficiency is calculated using a measured mapping of the efficiency of the DAHB module and the internally actuated ϕ operating at $f_{\mathrm{sw}} = 500$ kHz. The predicted efficiency is then found using this experimental DAHB efficiency mapping in conjunction with the relationship between efficiencies and the ratio of processed power to output power described in (1). An efficiency improvement of more than 9% for all power levels can be noted, in line with what is predicted using (1). The THD-F of the grid current is below 1% for output powers greater than 750 W.

C. Variable f_{sw} Scheme

Figs. 19–23 show the experimental results of the proposed inverter operating with the variable f_{sw} scheme. The allowable range of f_{sw} is up to 1 MHz. The most notable difference between the experimental results of the constant f_{sw} and variable f_{sw} schemes is the inductor current envelope for different output currents. Figs. 19 and 20 show I_d and I_q steps, respectively, of the variable f_{sw} scheme. It can be seen that the magnitude of the inductor current envelope changes as the output current changes, which allows light load efficiency improvements when compared to the constant f_{sw} scheme performance.

Fig. 22 shows a grid voltage sag of 120 V_{l-n}–20 V_{l-n} over four cycles of the grid. It can be seen that during this voltage sag event the grid current is unchanged aside from small distortions that can be attributed to common-mode grid voltage fluctuations. This demonstrates the current source performance of the proposed topology as functionality during this voltage sag event

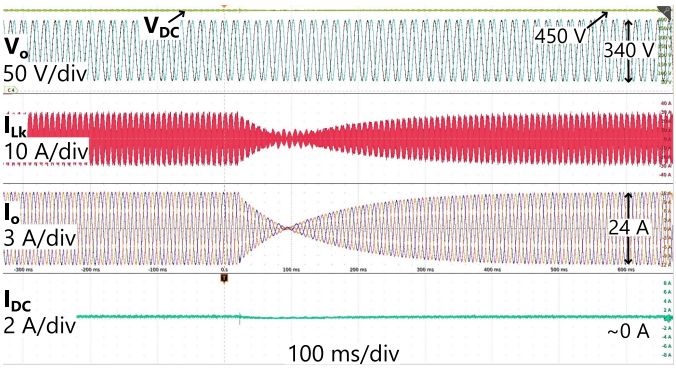

Fig. 20. Three-phase grid current I_o and voltage V_o, inductor current I_{Lk}, DC link voltage V_{dc}, and DC link current I_{dc} for variable f_{sw} control with a 14 to –14 A I_d step.

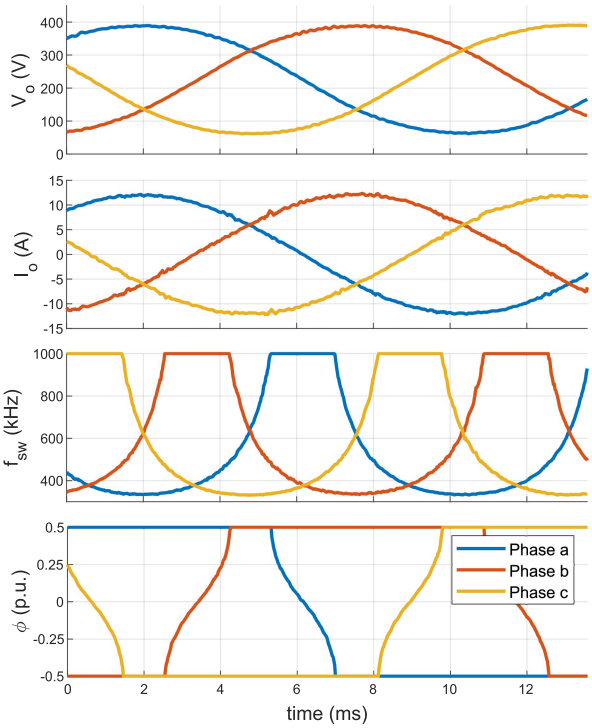

Fig. 21. $V_{o,abc}$, $I_{o,abc}$, $f_{\mathrm{sw},abc}$, and ϕ_{abc} as measured and actuated by the microcontroller.

can be maintained indefinitely with minimal interruption to the grid current.

Fig. 21 shows the f_{sw}, ϕ, I_o, and V_o as actuated and measured by the microcontroller over one cycle of the grid with I_d of 12 A. The relationship between f_{sw}, ϕ, and output current aligns with the theory presented in Section III-B. Noise in the V_o and I_o measurements can be attributed to nonidealities of the physical hardware sensors.

Lastly, Fig. 23 shows the efficiency and grid current THD-F of the variable f_{sw} scheme over a range of output power. The THD-F is less than 2% for output power greater than 500 W. Unlike the constant f_{sw} scheme, the maximum output power for the variable f_{sw} scheme is not limited by the saturation of ϕ, allowing for a significant increase in the allowable output

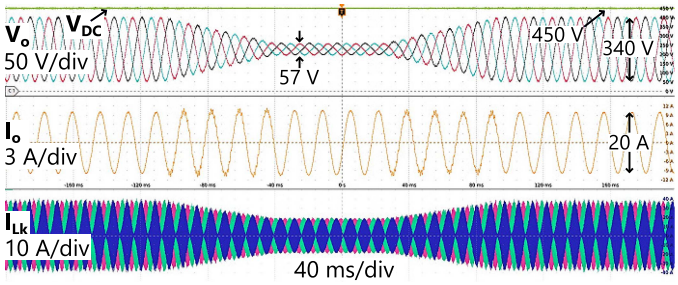

Fig. 22. Three-phase grid current I_o and voltage V_o, inductor current I_{Lk}, and DC link voltage V_{dc} during a grid voltage sag of 17% the nominal value.

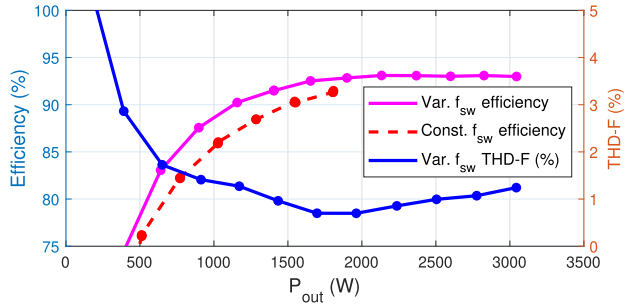

Fig. 23. Efficiency and grid current THD-F of the variable f_{sw} scheme. Constant f_{sw} scheme efficiency included for reference.

power. An efficiency improvement of 2%–4% and an increase in maximum output power of roughly 90% over the constant f_{sw} scheme can be noted.

VIII. Conclusion

This work shows a three-phase PPP inverter where each phase of the ac grid is serviced by a stacked DAHB. Analysis of the stacked DAHB in the context of the Manhattan topology as well as the influence of the dynamic operating points over the cycle of the grid are presented. It is shown that the PPP configuration of the stacked DAHB improves the overall efficiency, even as an ac interface, when compared with the efficiency of just the DAHB over these same operating points. Provisions for maintaining soft-switching of the DAHB over the cycle of the grid are provided and experimentally validated with two control schemes. Further work for this topic would include developing a method for optimizing the design of the power processing DAHB for this application.

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