Software-Defined Power Electronics: Interconnection and Coordination of Power Modules

Liwei Zhou, *Member, IEEE*, Boya Wang, Zong-Han Lin, *Student Member, IEEE*, Matthias Preindl, *Senior Member, IEEE*

***Abstract*——This paper proposes a concept of software-defined power electronics (SWD-PE) to abstract design and development of power electronics systems. Key motivations of SWD-PE include standardizing the design procedures of key energy conversion components and abstractly generalizing the power electronic system to fit different types of electrified load/source applications. The proposed software-defined power electronics architecture is composed of three layers: (1) application function layer for open access of different electrified load/source interfaces and the corresponding control function library; (2) interconnection layer for the high level coordination and management of the power electronics system; (3) physical layer for the desired type/number of standardized power modules equipped with current/voltage source local controller. The proposed software-defined power electronics architecture is mainly featured with three merits: (1) generalized design procedures to reduce the repetitive power electronics design processes; (2) reconfigurable architecture to form different power converter topologies with the corresponding control functions; (3) wide application interfaces to be applicable for various types of electrified load/source. Compared to the previous work, the proposed SWD-PE achieves more generalized power electronic design procedures with more robust energy conversion control performance.**

***Index Terms*—Software-defined power electronics, reconfigurability, power module, design and control.**

I. Introduction

POWER electronics design and development are typically specialized field for different types of electrified energy conversion systems [1]–[3]. The design of the power electronics devices is always application-oriented since the requirements of different electrified load/source may vary [4], [5]. The traditional power electronics design procedures can be generally summarized as five steps, namely, converter configuration, hardware design, software/control design, experimental validation and standard compliance. Since the first step of power converter configuration depends on the interfaced load/source characteristics, rated input/output voltage/current level and power demands, the subsequent procedures will be largely diverse. The specific parameter configuration requirement should firstly be comprehensively analyzed. On one hand, for the hardware part, the rated voltage/current/power requirements determine the device selection and PCB board design [6], [7]. The power converter topologies can also vary and are largely dependent on the interfaced load/source. Different types of interfaced load/source would also require disparate sensing circuits. This approach is shown in Fig. 1(a). On the other hand, for the software part, various types of applications need different number of sampling information, I/O channels, control function algorithms and so on [8], [9]. The different detailed configuration requirements of various industrial products make the power electronics design an application-oriented profession [10]. This approach is shown in Fig. 1(b).

A concept of power electronics building block (PEBB) has been proposed to standardize the hardware components for stackable energy conversion systems [6], [11]–[19]. The PEBB concept is more focusing on the physical components design to generalize the hardware power modules with extensible voltage/current capacity. A T-type PEBB is developed for the aircraft electric-propulsion drives with high current capability ($>$100 A) by leveraging the hybrid insulated gate bipolar junction transistor (IGBT) and silicon carbide switches [12]. Another two-level PEBB has also been designed for the more electrical aircraft applications with all SiC [6]. A direct AC/AC PEBB is demonstrated for medium-voltage grid connected applications which can be applied to the grid utility of 13 kV, 1 MVA [13]. Similarly, the three-level neutral-point-clamped PEBB is designed for the AC transmission system application [16]. The PEBB concept can also be leveraged to form typical circuitry topologies such as matrix converters and modular multi-level converters (MMC) [15], [19], [19].

Besides the PEBB for the hardware reconfigurability, some studies have also developed power electronics control architectures in a high level perspective to cover various applications [20]–[25]. Except for generalized hardware and software control architecture designs for power electronics, some research developed modular concept for power converters to further generalize the power electronics design procedures [26]–[28]. Other technical concepts studied the building of universal platform or infrastructure for the real-time power electronics testing and design [29]–[31].

Renewable energy resources are playing increasingly crucial roles in the energy system due to the urgency of zero emission. A typical microgrid system can be interfaced with various types of renewable energy resources such as solar energy, wind power and storage facilities, and it requires different kinds of power converters for the energy conversion and grid connection due to the diverse requirements on voltage, current and power ratings [32], [33]. As a consequence, the design procedures for various types of the power converters can be time-consuming and less cost-effective [34], [35]. Fortunately, ideas of SWD-PE can decrease these costs.

For the research and applications of power electronics design automation and modularity, several studies have presented the efforts on the software and hardware flexibility. A generalized tool is designed for fast and virtual prototyping of power

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converters in multiple domains [36]. The 3-dimentional parameters of the power converters are covered for the automated design in the hardware perspective. The study has also focused on the software side of the power conversion control algorithms design automation [37]. This study developed a model-free controller design methodology for the purpose of simplifying the software side design complexity. Another power electronics design automation technology has been developed by leveraging the multi-level computational architecture [38]. This study is especially focused on the harsh environment applications of the energy conversion. Additionally, an automatic data extraction method is designed to flexibly analyze the parameters and data from the MOSFET datasheets in order to accomplish the power converter hardware automated design procedures [39]. A model is proposed from the power converter hardware cost perspective to optimally manufacture the power electronic system from chip to converter levels [40]. The manufacturability of power electronics is developed for the applications of power supply [41]. Another study proposed the configurable power electronics for wireless power transfer application with functional execution procedures [42]. The future trends of additive manufacturing and automation for the power electronic hardware components is studied with more design flexibility and convenience for mass-production [43]. The magnetic components design automation methods have been addressed for the power electronic system to achieve the target of high coil efficiency [44]. The core of digital signal processor is studied to optimize the power operation in the embedded systems [45]. The generalized design method for the multiple port filter power dividers is proposed for the industry application [46].

SWD-PE coordination structure, as proposed in this work, differs from previous methods. The proposed strategy is based on a simplified three-layer stack which has covered different aspects of the typical power electronic system such as control, communication, power module, and interfaced applications. This new approach and its merits are shown in Fig. 2.

Contributions of the paper are:

- A three-layer power module interconnection structure considering reconfigurability and redundancy is developed to interface different types of loads and sources.
- We validate these SWD-PE concepts experimentally via various types of applications.

This paper is organized as follows. Firstly, the SWD-PE architecture is introduced by demonstrating the functions and tasks of the three-layer hierarchical structure. Secondly, the merits and characterizations of the proposed SWD-PE are analyzed in four aspects to show the capabilities of reducing repetitive power electronics design processes, reconfiguring various power converter topologies, wide application interfaces. Finally, six design cases are shown based on the developed SWD-PE architecture to experimentally validate the feasibility of the proposed concept. The design cases include DC/DC converter with resistive load, DC/AC grid-tied inverter, DC/DC interleaved operation on variable load, two-stage grid-interfaced EV charger, battery charging and isolated DC/DC converter.

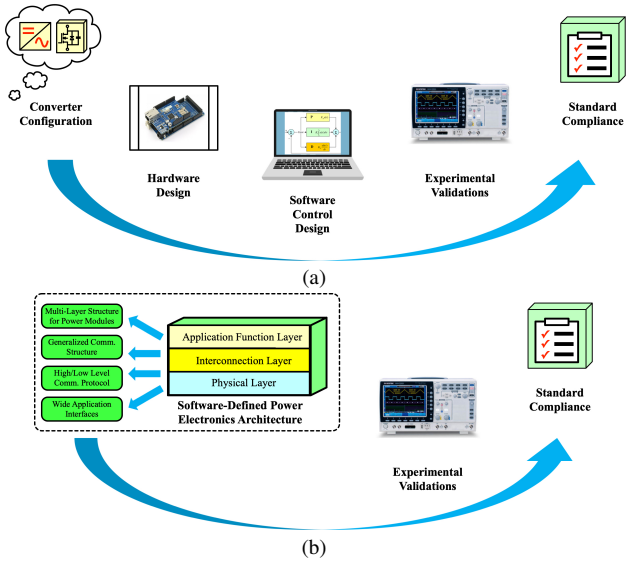

Fig. 1. The design procedures for (a) conventional power electronics system and (c) software-defined power electronics architecture.

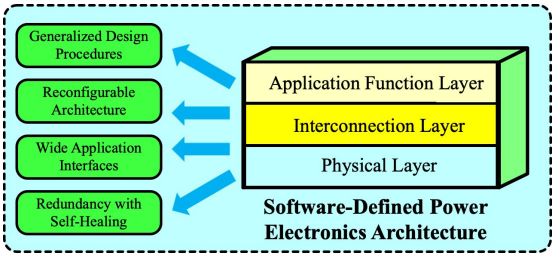

Fig. 2. The characteristics and holistic structure of the software-defined power electronics.

II. Conceptual Architecture

This section demonstrates the functions and the interconnection among the three layers of the SWD-PE architecture. Approach is shown in Fig. 3.

A. Application Function Layer

The application layer manages both the application power code and the information processing to be interfaced with 3 different types of applications. The application power code allows changing the function by setting the parameters of the application layer through the programmer, or a remote update. The information processing allows users to connect to a remote front-end on the network to have access to aggregated information that enable observe and control functions taylored to the applications.

The application power code is decentralized with each module to be embedded with corresponding control functions. The application control is composed of libraries that contextualize the use of a system. At a high level, it contains the designed state machine as well as control algorithms related to the use of the converter. The time constraints related to these control algorithms is managed by the operating system, as its scheduling capabilities can handle a multitude of functions.

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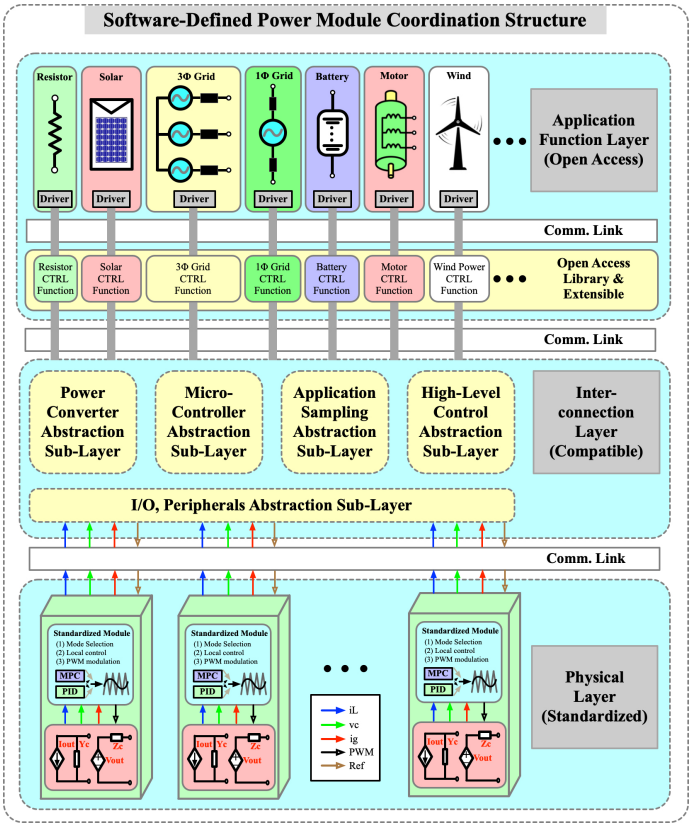

Fig. 3. Detailed implementatiion of the software-defined power electronics coordination structure.

The voltage/current/power control functions use a open access library to configure the function to be implemented.

The application function codes are composed of several types of modules bundled together to provide a higher level function, typically driven by a state machine.

The open access library is used to explicitly list the available functionalities of the voltage/current/power control and digital calculations. It also describes both the features of the power hardware, i.e. its operating limits and available measurements. The library also contains a description of the features of the digital hardware such as its microcontroller, its peripherals and other associated digital applications.

The information processing contextualizes the raw information of the system. State variables, such as measurements, control or calculations, are treated and aggregated to provide system observability. Communication via complex protocols that are supported by the operating system is possible via the deployment of dedicated libraries. Thus the converter communicates with the outside world through standard stacks that expose an application on a network, allowing its remote control or observation.

The data storage for the control functions describes the available data objects and the way they must be processed by the information processing block. Some data objects cor respond, for example, to events that need to be communicated as soon as possible, while other objects correspond to data that is broadcast in order to perform monitoring. Finally, this library is designed to be standard and thus allows for sharing and communication. Only certain pre-defined formats of the data objects can be transmitted on the communication bus, but all the available objects can be transferred into to the unified formats based on the application function needs.

At the application function layer the data is written to the local controller from the other layers and treated via the information processing. Once processed, the information can be written back to the controller, sent to the application control or to the front end. All data coming from either the front-end or the application power code is also treated by the information processing prior to be written to the controller.

B. Interconnection Layer

The interconnection layer manages the abstraction between upper and lower layers and handles the time-critical functions of the system. The abstraction is made by the Real-Time Operating System that drives the peripherals of the microcontroller which in turn drive the power hardware that interact with them. The time-critical functions are divided into a fast control and a data acquisition system that operate in lockstep.

The Embedded OS drivers provide the abstraction between the application power code and the physical layer. It contains drivers for the digital and power hardware that are called by the OS during compilation according to the power manifest.

Time critical components are still completely abstracted from the hardware. These algorithms have a much faster timing than their slow counterparts. They receive input pa rameters from the application layer, which are used to handle the measurement received from the data acquisition system. Fast control provides fast feedback to the digital hardware.

The interconnecton layer provides a double interface. On one hand, time critical functions provide the control signals to the digital hardware peripherals that drive the power hardware. On the other hand, the data acquisition system post processes the raw information collected by the analog peripherals of the digital hardware and write them to the data manifest to be later used by the application layer [47].

C. Physical Layer

The physical layer includes the power and digital hardware. The power hardware controls the flow of electricity through some form of conversion (DC-DC, DC-AC). The digital hardware is composed of a microcontroller, its integrated peripherals and other peripherals through which the microcontroller communicates with the outside.

The digital hardware is made of the microcontroller that embeds the software stack and all of its peripheral drivers. It receives information from the fast control to update the PWM signals that drive the power hardware. It also receives sensor signals from the power hardware through its analog block that automatically converts them into digital values that are sent to the data acquisition system. It can also receive data from the RS485 fast bus or synchronization signals via the Sync bus.

A low level communication is made of three sub blocks or buses, namely RS485, Analog and Sync. They allow each module to exchange data objects necessary to coordinate actions within a group of the multiple modules:

- A fast RS485 bus is used to share fast digital information, either fast control setpoints, or common measurements that should be broadcast at low level, such as a motor position.
- The Analog bus shares one real time measurement across multiple modules, and is typically used for equal current sharing.
- The Sync block allows several hardware modules to share accurate timing of their PWM generators.

The power hardware is designed to be flexible for wide application of various types of load and source. The interleaved buck topology is leveraged to minimize the stress on the passive components while allowing application flexibility at the module level. The objective is to maximize the application spectrum while minimizing complexity and cost. The same module can be used to perform buck, boost and single-phase inverter conversion. The implemented module is shown in Fig. 5.

In the end, hardware for low level communication protocol such as a CAN bus or SPI is implemented onboard and is mainly used for slow telemetry as described in the application layer paragraph.

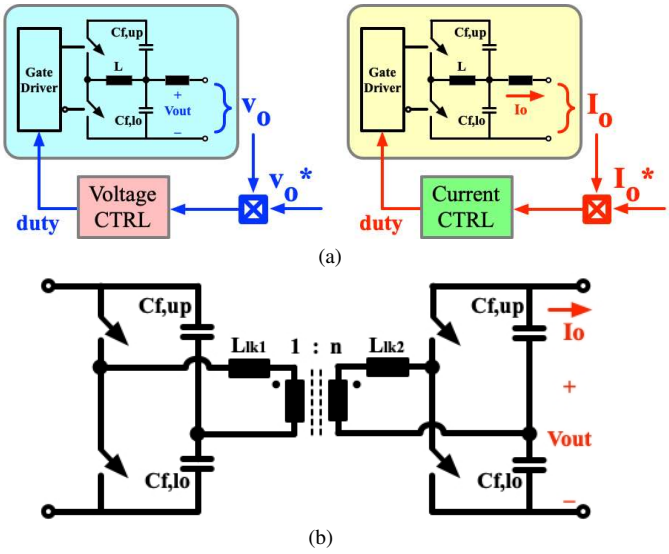

Fig. 4. Standardized (a) non-isolated power modules (b) isolated power module.

III. Practical Implementation

The merits and characterizations of the developed software-defined power electronics architecture include three aspects: (1) generalized design procedures without redundant extra design cost; (2) reconfigurable architecture that can be reconstructed for different circuitry topologies; (3) wide application interfaces for the coverage of various types of electrified load/source.

To achieve the above-mentioned four aspects of merit, the software-defined power electronic hardware prototype and the corresponding power module design could follow the following practical procedures.

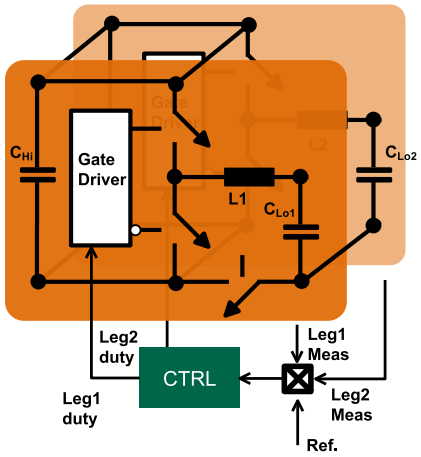

Fig. 5. Standardized two-phase non-isolated module.

A. Application Function Layer Implementation

For the practical implementation of the application function layer, it is mainly responsible for the definition of the targeted types of applications to be interfaced and development of the corresponding source and load sides functions. The desired interfaced loads and sources include single-phase, three-phase grid, solar panel, wind turbine, battery, electric motor, DC resistive load and so on.

1) Defining the targeted applications: The first step to implement the application function layer is defining the targeted application. Specifically, various types of the load and source are expected to be connected with the software-defined power electronic system for power delivery. The power rating, voltage level, current limit of the interfaced load/source will be quantified and pre-configured to guide the power module design in the physical layer. Besides the power/voltage/current levels, the open access application library is pre-designed which includes the application-oriented control functions.

2) Developing source/load side functions: The second step to implement the application function layer is developing the detailed source/load side functions. Specifically, the corresponding types of the control functions in the open access application library will be leveraged to deliver the power between the interfaced load/source and the power converter modules. This application-oriented control function is configured as the high-level control block. It typically generates the control signals as the tracking reference for the local power modules to follow.

The demonstrated design cases of the application function layer implementation have been shown in Fig. 6 and Fig. 7. Specifically, in the battery charger energy conversion system to interface with the grid utility, the application function layer includes the reference frame transformation, PLL, grid side current control, DC bus voltage control, battery constant current control, battery constant voltage control and so on.

B. Interconnection Layer Implementation

For the practical implementation of the interconnection layer, it is mainly responsible for power converter topology

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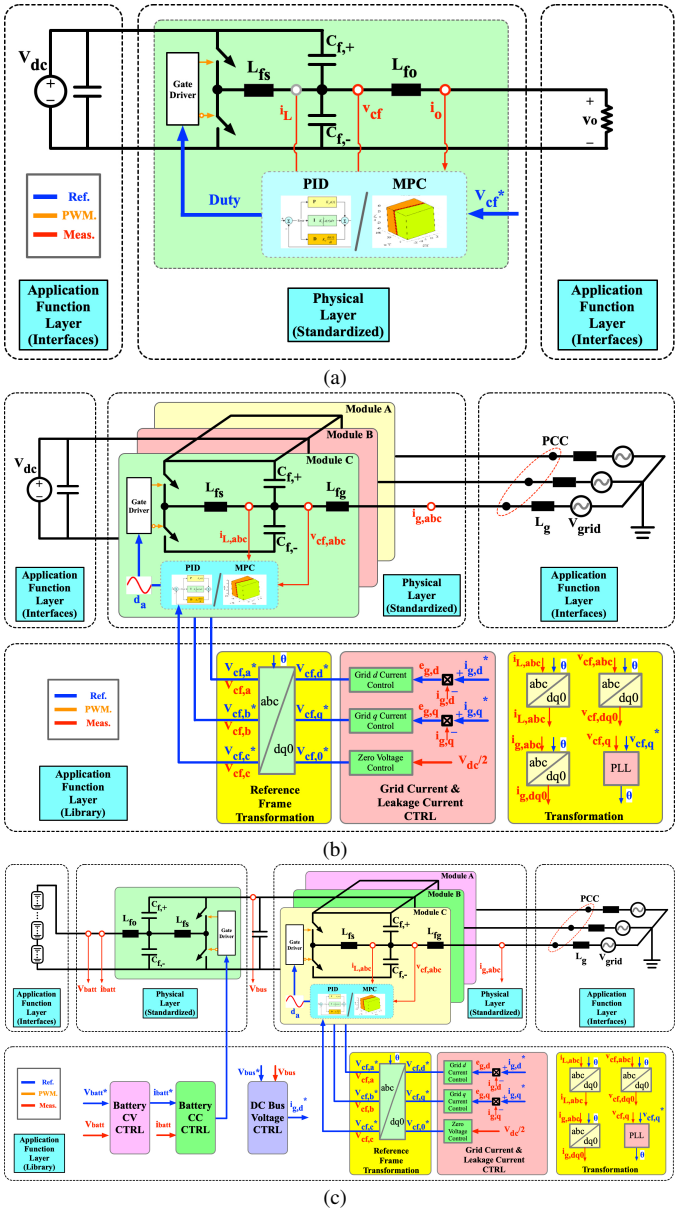

Fig. 6. Design cases for single-stage (a) DC/DC converter with resistive load (b) DC/AC three-phase grid-tied inverter and (c) two-stage electric vehicle DC charger interfaced with the grid based on non-isolated local power modules.

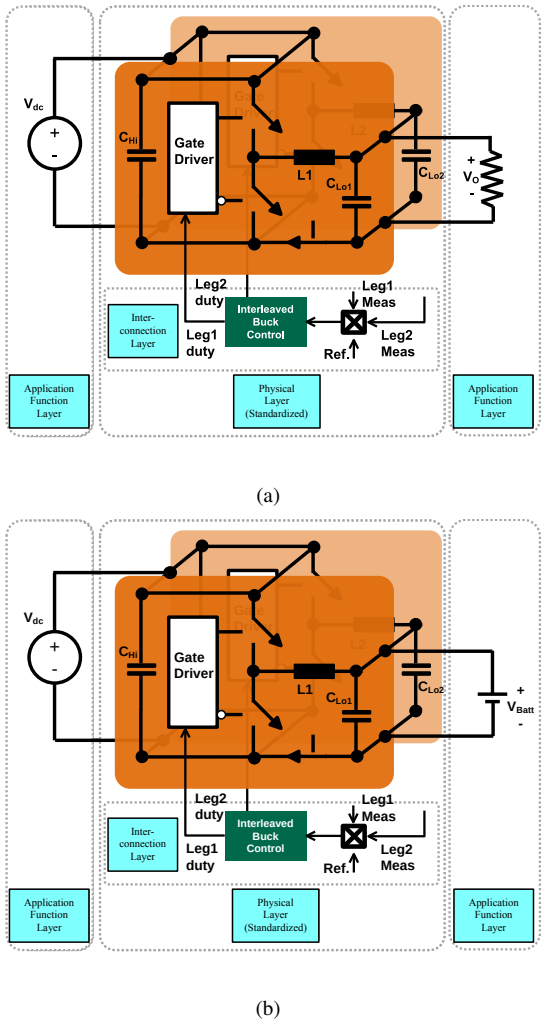

Fig. 7. Design cases of single-stage for (a) an inverleaved Buck converter with resistive load and (b) an inverleaved Buck converter as a battery charger.

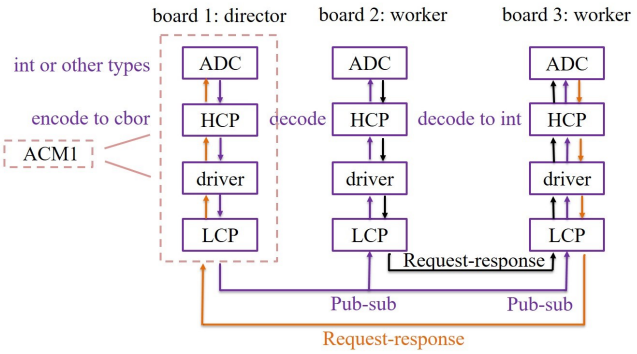

Fig. 8. HCP daisy chain on board structure.

design, control/sampling/switching alignment and communication protocol development. This layer is functioned as a supervisor to guide on how to organically integrate the various types of the load/source and the local power modules for the desired power delivery.

1) Designing power converter topologies: The first step to implement the interconnection layer is designing the power converter topologies. The desired power converter circuit is based on the demand from the application function layer. Different types of load/source require various power converter circuit topologies to meet the energy conversion target. Specifically, the number of input and output ports, the number of modules per port, isolated or non-isolated module selection, filter circuit structure and parameter need to be configured to guide the formulation of physical layer power modules.

The demonstration of the design case in Fig. 6 illustrates the formulation of the power converter topology guided by the interconnection layer. For the three-phase grid-tied inverter application, three power modules are configured on the AC side to interface the three phases of the grid. For the two-stage EV DC charger application, one power module is configured on the battery side to deliver the constant current and constant

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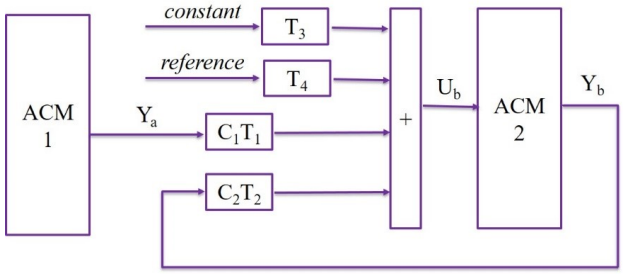

Fig. 9. Linking structure between two boards.

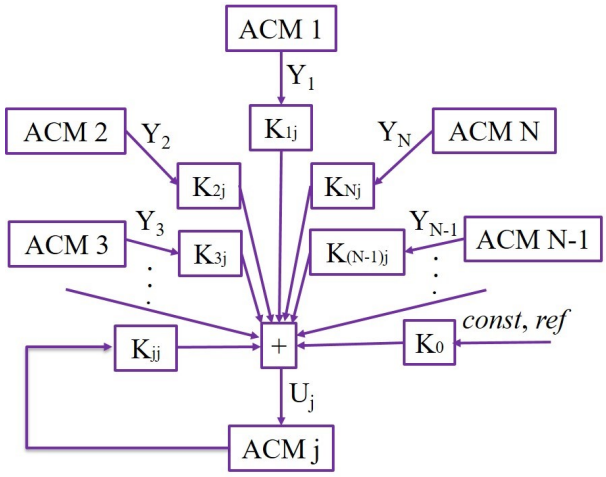

Fig. 10. Linking structure between N boards.

voltage charging and discharging processes. Three modules are connected to the grid to deliver the DC battery power from or to the three-phase grid.

2) Determining control/sampling/switching alignment: The second step to implement the interconnection layer is determining control/sampling/switching alignment for the specified power converter topology. The control algorithms and sampling parameters should be aligned to the switching periods for accurate power operation and voltage/current management. To be noted, in the interconnection layer, the alignment among the control, sampling and switching is mainly for interlinking the upper application function layer and the lower physical layer. The control algorithms are not created or designed in the interconnection layer. Rather, the interconnection layer is managing the control algorithms from the upper and lower layer to ensure the upper control and lower control are properly aligned and cascaded for desired power/voltage/current control targets.

For the alignment of control, sampling, and switching, the corresponding frequency synchronization is the primary target. Specifically, in each control period, the DSP (digital signal processor) should synchronize the interrupts among the control, sampling and switching loops to ensure no mismatch is happening in the whole energy conversion periods. The time scales can be different for the control, sampling and switching periods. However, the relationship among the three frequencies should follow the integer multiple times. For example, if the control frequency is f_{ctrl}, the sampling frequency, f_{sample}, could be configured as Nf_{ctrl}, where N is an integer. And the switching frequency, f_{switch}, could be configured as Mf_{sample}, where M is also an integer. The pulsed-width modulation (PWM) of the three signals should also be synchronized with the same starting instants. Doing so, the accuracy and alignment of the proper power/voltage/current control and computation can be ensured.

3) Developing communication protocols: The third step to implement the interconnection layer is developing communication protocols among different number of the power modules in the physical layer. A generalized High-level Control Protocol (HCP) provides a standardized and generalized way to observe, configure and control resource-constrained devices via various communication interfaces. It identifies top layers of the OSI model. The payload data is independent of lower layer protocol or interface, such as SPI, CAN, USB, LoRa, WiFi, Bluetooth, UART and so on.

Typically, a generalized HCP defines two types of corresponding models including requests-responses model and publish-subscribe model. For request-response model, request is sent from client server, and the server is expected to answer by a response containing a status code and optional payload. In contrast, for publish-subscribe model, statement will be sent without expecting any response. It can be sent to a particular device or broadcast through the network to be received by any interested device. One dedicated application can be the plug-and-play control of multi-energy sources in renewable energy systems. Fig. 8 shows an instance of HCP on board structure. There are three boards in figure, where board 1 is called director (leader), others are called worker (follower). In this structure, board 1 adopts publish function to broadcast data, and other boards subscribe it. Board 2 and 3 send request to get ADC data and encode it into CBOR. The data is sent to board 3 and 1 with responses.

Inspired by PEBB, each HCP on board structure is defined as auto configurable module (ACM). Since HCP and LCP adopts different data type in the aspect of bit number, a software driver is needed to convert the data before sending.

Advantages of this HCP on board structure are: (a) It is a generalized structure which is applicable for different kinds of boards. In other words, HCP is considered as a generalized protocol, which can be connected with various lower level protocol or interface like CAN, USB, WiFi, UART(serial) and so on; (b) A generalized HCP can be integrated with a few other application layer protocols such as HTTP, CoAP and MQTT; (c) HCP is a code library that defines request-response and publish-subscribe function, together with readable data type. In other words, it is a user-friendly and flexible protocol.

Because of generalization, star structure is required as topology to create any possible links. Fig.9 shows the linking structure between two boards (this figure shows the way to link ACM 1 to ACM 2 as an instance). In this figure, each ACM can be represented by basic state-space function with input U and output Y. In this way, input of board 2 can be linked with four sections including entries in output of board A, entries in output of board 2 (for feedback control), constant, and references.

Based on Fig.9, linking equation of ACM 2 is:

$$\begin{bmatrix} u_{b1} \\ u_{b2} \\ . \\ . \\ . \\ u_{br} \end{bmatrix} = \boldsymbol{C_1 T_1} \begin{bmatrix} y_{a1} \\ y_{a2} \\ . \\ . \\ . \\ y_{an} \end{bmatrix} + \boldsymbol{C_2 T_2} \begin{bmatrix} y_{b1} \\ y_{b2} \\ . \\ . \\ . \\ y_{bn} \end{bmatrix} + \boldsymbol{T_3}[const]^{\mathrm{T}} + \boldsymbol{T_4}[ref]^{\mathrm{T}} \tag{1}$$

where the input set for board 1 is denoted as $U_a = [u_{a1}, u_{a2}, \ldots, u_{ap}]^{\mathrm{T}}$, with output set $Y_a = [y_{a1}, y_{a2}, \ldots, y_{an}]^{\mathrm{T}}$. For board 2, $U_b = [u_{b1}, u_{b2}, \ldots, u_{br}]^{\mathrm{T}}$, $Y_b = [y_{b1}, y_{b2}, \ldots, y_{bn}]^{\mathrm{T}}$. The parameters of T in the equations are for element selection and dimension changes for different vectors based on graph theory, and C represents weights. $\boldsymbol{C_1}$, $\boldsymbol{T_1}$, $\boldsymbol{C_2}$ and $\boldsymbol{T_2}$ connect the control parameters to be leveraged for assignment, $\boldsymbol{T_3}$ and $\boldsymbol{T_4}$ consider the constants and the references. For instance, if the first k element in U_b is contributed by their counterpart in Y_a, and the rest $r-k$ element is contributed by last part of Y_b, suppose all weights equal to 1 (contributed equally), then,

$$\begin{aligned} \boldsymbol{C_1 T_1} &= \begin{bmatrix} I_{k\times k} & 0_{(n-k)\times k} \\ 0_{(r-k)\times k} & 0 \end{bmatrix} \\ \boldsymbol{C_2 T_2} &= \begin{bmatrix} 0_{k\times k} & 0_{(n-k)\times k} \\ 0_{(r-k)\times k} & I_{(r-k)\times(r-k)} \end{bmatrix}. \end{aligned} \tag{2}$$

By expanding it to N-board structure as in Fig. 10, the input of any ACM j is

$$U_j = \sum_{i=1}^{N} K_{ij} Y_i + K_0[const, ref]^{\mathrm{T}} \tag{3}$$

where K_{ij} is linking matrix from ACM i to ACM j, or from node i to node j in graph theory. Based on linking equations, HCP can use request-response or pub-sub function to achieve any links based on different needs. Advantages of this strategy include: (a) generalized strategy for any kinds of topology; (b) applicable for any PE environment with any kinds of control, since the basic state-space function is leveraged for representation.

C. Physical Layer Implementation

For the practical implementation of the physical layer, it is mainly responsible for designing local control algorithms and configuring module switching strategy. This layer is functioned as an implementor to operate the hardware power module and energy conversion for power delivery.

1) Designing local control algorithms: The first step to implement the physical layer is designing the local control algorithms. Each power local power module is configured as a power delivery unit which is at the forefront to deliver power for various types of the load and source. The power module is designed to be standardized and reconfigurable to form different types of power converter topologies based on the guidance in the interconnection layer. Each power module is also configured with the corresponding local control algorithms to regulate the output voltage and current. Two types of control modes can be selected for local power module control: model predictive control (MPC) and proportional-integral-derivative (PID) control. MPC has better dynamic performance during the transient period but the computation burden is high. On the other hand, PID is simple to implement without consuming too much computation resource but the high frequency signals could result in oscillation and spikes in transient. The local MPC/PID controllers receive the high level tracking references and command from the application function layer to regulate the output voltage and current of each local power module and generate the duty cycles for PWM operation and switching signal generation.

2) Configuring module switching strategy: The second step to implement the physical layer is configuring the module switching strategy. Specifically, the soft switching operation is configured for each power module to reduce the switching loss and improve the energy efficiency. Based on the power rating and current reference commands, the switch side inductor current waveforms are reshaped by adjusting the switching frequency in real-time. The high turn-on loss can be mitigated by the soft-switching turn-on with time-varying switching frequency and bi-directional switch side inductor current ripple envelope.

IV. Experimental Validation

Based on the two proposed software-defined power electronics implementations, various types of applications are validated in this section including grid-connection, battery and resistive load. The multi-layer control diagrams of the design cases are shown in Fig. 6 and Fig. 7. The prototype and the parameter information have been shown in Fig. 11 and Table I, respectively. The corresponding experimental validations are shown in Fig. 12 to Fig. 17.

A. Validation of communication part

ThingSet (TS) [48] is leveraged as an instance of HCP. CAN and Serial peripheral interface (SPI) are used as instances of LCP. The signals are sent based on a differential structure to attenuate disturbance. The average latency for sending one 32-bit data with CAN running at 500 kbit/s is 236 µs, and is 3.2 µs with SPI running at 25 Mbit/s. As this communication is used for generating references for inverter control, typically, the time scale for this level is 10ms [49], which indicates latency less than 1ms will not affect stability.

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B. DC/DC Converter with Resistive Load

The control diagram of DC/DC converter with a resistive load for both implementations is shown in Fig. 6(a) and Fig. 7(a). The non-isolated voltage source power module is leveraged to control the output voltage of the resistive load with PID for both implementations or MPC for the AUTOSAR-based one. Fig. 12 shows the output current/voltage and inductor current results and the zoomed waveforms.

C. DC/AC Grid-Tied Inverter

The control diagram of DC/AC three-phase grid-tied non-isolated inverter is shown in Fig. 6(b) based on the SWD-PE architecture. Three non-isolated voltage source power modules are leveraged as the physical layer to form the power converter portion. In the application function layer, grid current/leakage current control and reference frame transformation functions are configured to assign references for the local power modules. As in reference , dc-ac converter If we consider director and workers separately, linking equation for director is

Fig. 13 shows the corresponding inductor current, output capacitor voltage, grid current and DC bus voltage waveforms.

D. Interleaved Operation on Variable Load

The control diagram of a DC/DC power converter delivering power to a variable resistive load is shown in Fig. 7(a) based on the SWD-PE Zephyr-based implementation. The two legs of a single power module are interleaved and the power flow is managed by a single PID. This PID tracks the current on leg 1 to 1A up until the voltage reaches 14V, after which the converter delivers a constant voltage. Fig. 14(a) shows the corresponding waveforms. The difference in currents shows that interleaving requires a more complex control algorithm to guarantee the current sharing between the two legs.

E. Two-Stage Grid-Interfaced EV Charger

The control diagram of two-stage grid-interfaced EV charger is shown in Fig. 6(c) based on the SWD-PE architecture. The system is composed of a DC/DC converter on battery side and a DC/AC inverter on grid side. One and three non-isolated voltage source power modules are leveraged as the physical layer to form the battery side DC/DC portion and grid side DC/AC portion, respectively. In the application function layer, battery CC/CV control, DC bus voltage control, grid current/leakage current control and reference frame transformation functions are configured to assign references for the local power modules. Fig. 15 shows the corresponding grid current, battery current/voltage and grid voltage.

F. Battery Charging System

The control diagram of an interleaved battery charger system is shown in Fig. 7(b) implemented on the Zephyr-based SWD-PE architecture. Fig. 14(b) shows the corresponding results of this implementation. The battery is charged by both legs with a single PID control based on leg1 measurements. The charger is in constant current mode until the voltage reference is reached, after which it switches to constant voltage mode. The difference is current shows that a current compensation algorithm is necessary to make both legs share the same current.

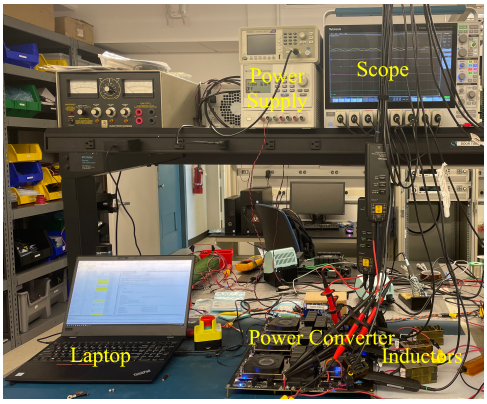
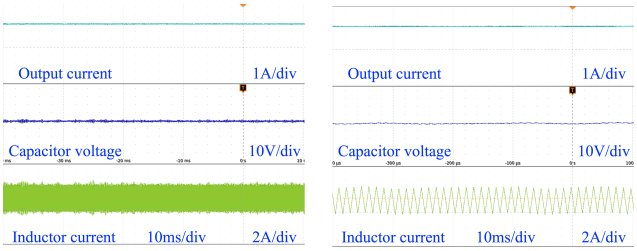


Fig. 11. Prototype for the experimental validation.



(a) (b)

Fig. 12. Experimental results of (a) output current, capacitor voltage, inductor current for DC/DC converter application with resistive load based on non-isolated local power modules and (b) the corresponding zoomed waveforms.

G. DC/DC Converter Based on Isolated Power Module

Besides the non-isolated power modules to be leveraged for the construction of SWD-PE architecture, the isolated DAHB power module in Fig. 4(b) is also validated. Fig. 17 shows the experimental waveforms of leakage inductance current, primary/secondary transformer voltages based on the voltage source type of isolated local power module in physical layer.

H. Comparison with State-of-the-art

To demonstrate the merits of the proposed software-defined power electronic system, we have compared the proposed

TABLE I
EXPERIMENTAL SETUP PARAMETERS

Parameter	Value
Grid voltage of DC/AC	120 V
DC voltage of DC/DC	10 to 100 V
Switching frequency	100 to 200 kHz
AC inductor of DC/AC	45 μH
DC inductor of DC/DC	15 μH
AC capacitor of DC/AC	30 μF
DC capacitor of DC/DC	30 μF
MOSFET	C3M0021120K
Controller	LAUNCHXL-F28379D

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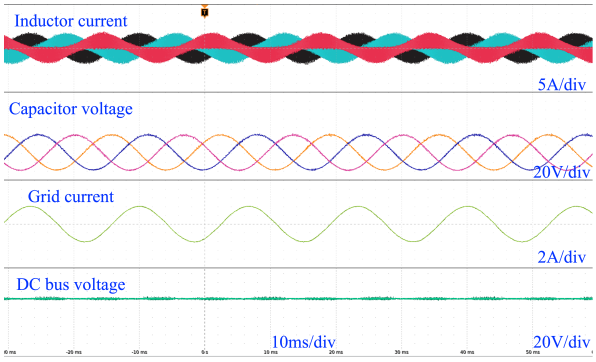
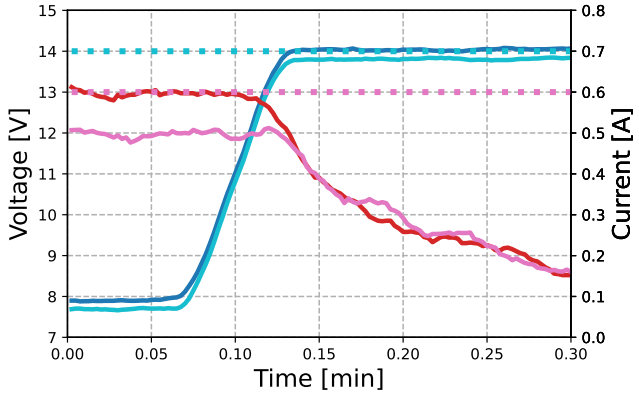
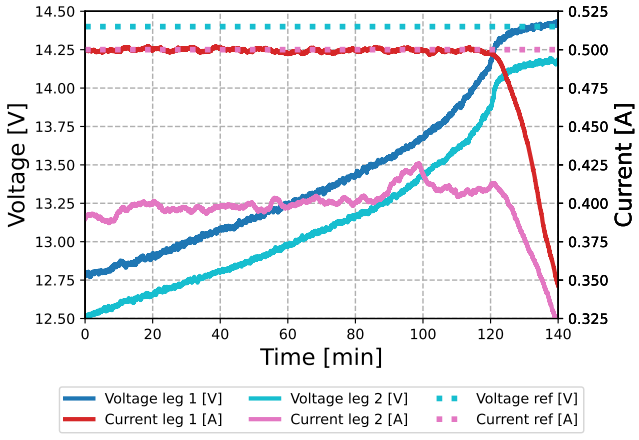


Fig. 13. Experimental inductor current, capacitor voltage, grid current and DC bus voltage waveforms of grid-interfaced three-phase DC/AC inverter based on non-isolated local power modules.



(a)



(b)

Fig. 14. Experimental validation of the reprogrammable functionalities of the Zephyr-based implementation for two cases. (a) Variable resistive load behavior: converter operating with fixed current reference of 1 A until 14 V are reached. Once reached, the converters tracks a 14 V voltage reference. Interleaving behavior shows differences in leg currents. (b) Battery charging behavior: converter operating in constant current mode 0.5A per leg until 14.4 V are reached. Once reached, the converters switches to constant voltage mode with a 14.4 V. Interleaving behavior shows differences in leg currents.

method with the state-of-the-art power electronic design au-

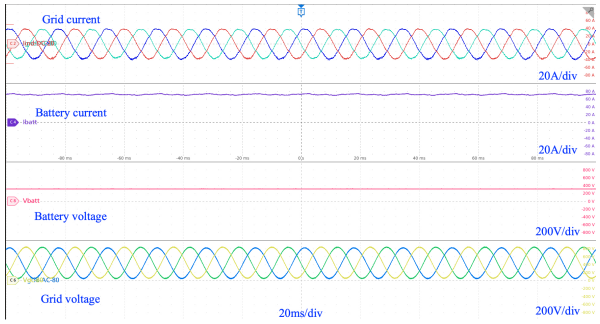
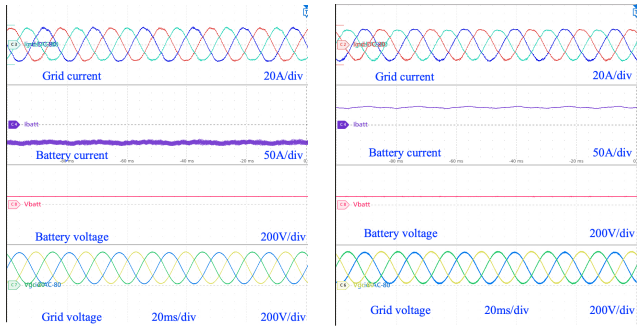


Fig. 15. Experimental grid current, battery current, battery voltage and grid voltage waveforms of two-stage converter level electric vehicle charger based on non-isolated local power modules.



(a) (b)

Fig. 16. Experimental grid current, DC current/voltage, grid voltage waveforms of (a)first and (b) second grid-interfaced distributed inverters.

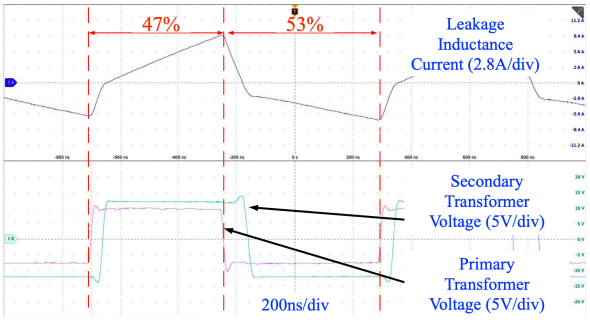


Fig. 17. Experimental leakage inductance current and primary/secondary transformer voltages waveforms of DC/DC converter based on isolated power module.

tomation techniques in the aspects of hardware cost, software complexity, energy efficiency, dynamic performance and power density. The comparison has been demonstrated in Table II. Based on the analysis in [40], the cost of 600V EV application of the three-phase power converter can be $1200 and $2300 at the power levels of 20 kW and 200 kW, respectively, with the product number of 100 units. However, if the product number is increased to 10,000, the cost will be decreased to $260 and $1300, respectively. The quantitative data of our proposed software-defined power electronic method is also shown in this section. Firstly, in the aspect of hardware cost, taking advantage of the proposed power electronics design method, the unit cost per kilo-watt is around $25/kW for the application of a 50 kW EV DC charger which is 30 % less than

the existing commonly used technologies. Secondly, in the aspect of software complexity, the total digital signal processor (using Texas Instruments C2000 processor) execution time at a complete control period is less than 15 μs which is 50 % less than the execution time for the typical three-phase grid-connected inverter control algorithms by leveraging model predictive control method. Thirdly, in the aspect of energy efficiency, the proposed method can achieve more than 99 % for a bidirectional power flow operation at 30 kW which is 0.5-1 % higher than the state-of-the-art EV charger applications. Fourthly, in the aspect of power density, a 30 kW three-phase inverter can achieve more than 12 kW/L volumetric power density which is 40 % higher than the conventional power converter design methodology.

For the design procedure cost reduction by applying the proposed software-defined power electronics, a more detailed analysis is demonstrated as follows. The state-of-the-art industrial power electronic design is typically specialized and case by case. Thus, it is difficult to utilize one set of power electronic design procedures, e.g., schematic design, PCB design, circuit topologies, voltage and current control algorithms, application-oriented control functions, programming development environment configuration, for other applications. For a more thorough breakdown analysis, the typical power electronic design stages mainly include (1) preliminary design involving power level, voltage/current requirements, converter topology; (2) schematic design involving circuit design, component selection and interconnection; (3) PCB layout involving components placement, signal and power traces routing; (4) prototyping involving physical power testing and validation. Firstly, for the preliminary design stage, [50] suggested that the costs can range from $1,000 to $5,000. Secondly, for the schematic design stage, [51] concluded that the cost of creating the electrical schematic diagram of the circuit can range from $2,000 to $8,000. Thirdly, for the PCB layout stage, [52] estimated that for designing the physical arrangement of components on the PCB, the costs can range from $2,000 to $9,500 or $12,000. Fourthly, [53] found that the cost of creating physical prototypes of the circuit board to test and validate the design can range from $2,500 to $7,500 per iteration. In the proposed software-defined power electronic design method, taking the advantage of reconfigurable and multi-layer generalized design architecture, the above-mentioned first three stages of preliminary design, schematic design and PCB layout can be significantly saved for various types of load and source applications. The corresponding repetitive design cost can be reduced by 60-80 %.

I. Broad Application Interfaces

The applicability and adaptability of the proposed method in high-voltage/high-power scenarios (e.g., above 10 kV) and high-frequency topologies (e.g., LLC resonant converters) is discussed in this section. Firstly, for the applicability in high-voltage and high power scenarios, the future developing direction can be focused on the vertical and horizontal extension of the standardized power module. On one hand, the vertical connection of the power modules can expand the voltage capacity for the applications of medium or high voltage power systems. On the other hand, the horizontal connection of the power modules will expand the current capacity for the applications of low voltage and thick cabling power supply systems. Both directions of the extension require more reliability-oriented design consideration, since more power modules connection can result in less safer energy conversion performance. Thus, the power device selection, hardware layout spacing, robust control algorithms and fast protection mechanism should be studied, accordingly.

V. Conclusion

A SWD-PE architecture is proposed for the abstraction of electrified energy conversion system design and development procedures. The SWD-PE architecture is composed of three layers, application function layer, interconnection layer and physical layer.

The SWD-PE concept has been validated with various applications such as isolated/non-isolated DC/DC converter, grid-tied inverter, battery charger and motor traction inverter to show the feasibility. The merits of the SWD-PE have been verified experimentally in four aspects: (1) generalized design procedures without redundant extra design cost; (2) reconfigurable architecture that can be reconstructed for different circuitry topologies; (3) wide application interfaces for the coverage of various types of electrified load/source.

To be noted, the proposed software-defined power electronic system is not unlimited in the aspects of power level, topology complexity and application variation. The open access library in the upper application function layer is extensible with the pre-configured control functions. However, the power limitation is restricted by the power module capability and number of modules to be connected. The topology complexity is also based on the circuit structure of each power module. Thus, for the forward-looking development plan, more effort should be focused on more functional flexibility enhancement in application layer and power capability/circuit complexity enhancement in the physical layer.

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TABLE II
Comparison with State-of-the-art

	Hardware Cost	Software Complexity	Energy Efficiency	Dynamic Performance
[36]	High	N/A	Low	High
[37]	Low	High	N/A	Low
[38]	High	N/A	Low	High
[39]	Low	Low	Low	Low
[40]	High	Low	N/A	N/A
[41]	Low	N/A	Low	High
[42]	High	N/A	High	Low
[43]	N/A	High	Low	High
[44]	High	Low	N/A	High
[45]	High	N/A	High	Low
[46]	Low	N/A	Low	Low
Proposed	Low	Low	High	High

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