A General Fully Distributed Control Scheme Considering Time Delay Compensation for Three-phase Grid-tied Power Inverter Systems

Boya Wang
Dept. of Electrical Engineering
Columbia University
New York, USA
bw2788@columbia.edu

Matthias Preindl
Dept. of Electrical Engineering
Columbia University
New York, USA
mp3501@columbia.edu

Abstract—**A general fully distributed control (FDC) scheme considering time-delay compensation (TC) was firstly designed for three-phase grid-tied power inverter systems. Theoretical analysis was derived to show that this strategy could largely increase the control bandwidth of the system compared with using centralized control strategies, especially when an advanced but time-consumed local level controller (LLC) is used to achieve better power qualities (e.g., increment can be at least 50% if computation time for LLC is 10µs). It was also proved that this strategy could decrease the theoretical minimum required value of the communication bitrate (when one controller sending data to the other controller) to 50% of 'FDC without TC' and 37.5% of central-distributed control, without decreasing output power quality. Besides, the optimization based TC strategy we used will not increase LLC calculation time. Proposed strategy was validated by simulation with supported data provided by experimental test.**

Keywords—Fully distributed control (FDC), time delay compensation, control bandwidth

I. INTRODUCTION

Three-phase inverter plays a significant role when DC voltage sources, such as renewable energy resources (RES) or EV batteries, are connected with power grids. In order to get way better efficiency and power qualities, advanced and accurate control strategies are necessary. However, because these strategies need a lot of computations, it can delay the control process, too.

Reference [1] designed a two-layer control structure containing central and local level for the grid-connected three-phase inverter systems, where an explicit model predictive control (MPC) was used in its local control in order to largely boost its transient process. However, calculation in one MPC controller needs 4µs, so 12µs will be needed in one control period in three phases, given the fact that only one DSP control card was used for hardware validation and all calculations need to be done in serial [1]. As a consequence, the highest control bandwidth (BW) will be largely decreased. Reference [2] used an optimization-based estimation (OBE)-MPC for the identical grid-connected structure in order to largely attenuate noise and oscillation, however, calculation of one OBE-MPC needs 11µs,

adding up to 33µs in one control period when doing hardware test, and it will significantly decrease control BW.

A high control BW is essential in control because it can allow systems be more stable, enhance power quality further, and be enabled to see high frequency disturbance or resonance [3], [4]. In order to increase BW, distributed control can be a good strategy because calculations in local controller can be done in parallel. Reference [5] designed a central-distributed control structure based on separate control card for the central and every local controller respectively, it can indeed increase BW because calculation in every local controller can be done in parallel. However, there is still space to enhance because when central controller delivering or receiving data from each local controller, and this part is in serial.

Recent references designed fully distributed control structures for RES in micro-grid or power grids to get rid of the central controller [6]. Because RES are far from each other in distance, local controller has to be adopted for each one. In order to use droop control and decide the power references [7], each local controller needs voltage or current info from others, where fully distributed control strategies are used. Besides, these papers also considered the effects of time delays and revised droop control to attenuate it. Delays can be variables or constants, and it is hard to calculate [8].

As for attenuating delay's effects, reference [9] found another way. An optimization model was derived together with a new objective function considering delays based on H-infinity control. Even though this strategy is accurate, yet, because the new objective function contains state variables in previous time steps, it will largely increase the calculation time, which is contrary to the general idea of accelerating the control process. Reference [10], [11] and [12] use the state observer to predict delays or disturbances, yet, it needs a lot of previous data and cannot guarantee accuracy. Hence, we choose to suppress delays based on a real-time connections topology change of the three local controllers in three phases, we call it connection rescheduling (CR).

Inspired by above references, this paper designed a general fully distributed control (FDC) scheme considering time delay compensation.
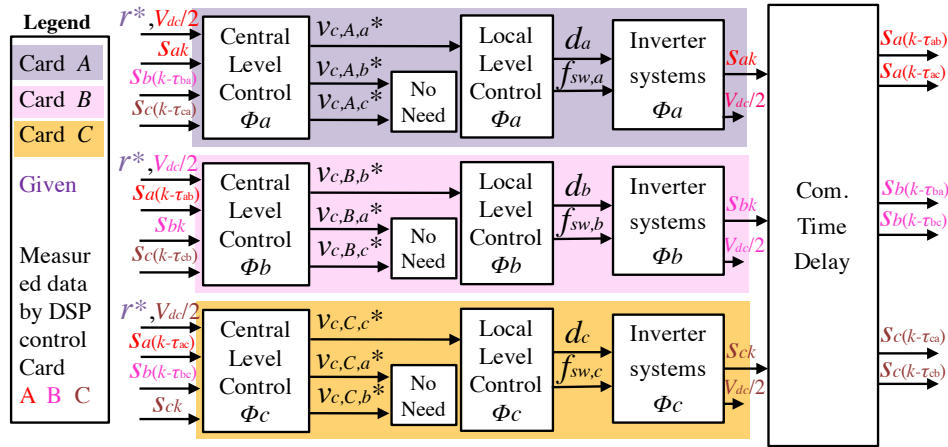
Fig. 1.   General FDC control scheme

Contributions of this paper are:

(1) Firstly designed a general fully distributed control scheme with connection rescheduling (FDC-CR) for the three-phase grid-tied power inverter systems to largely increase BW and compensate delays.

(2) Validated it by simulation, based on supported data provided by experimental test.

II. GENERAL FULLY DISTRIBUTED CONTROL SCHEME

The non-isolated three-phase inverter grid-tied system is shown in Fig. 2, for which [1] provided a detailed introduction. $i_{g,abc}$ is grid current, $v_{c,abc}$ is capacitor voltage, and $i_{L,abc}$ is inductor current. These three variables can show properties of control.
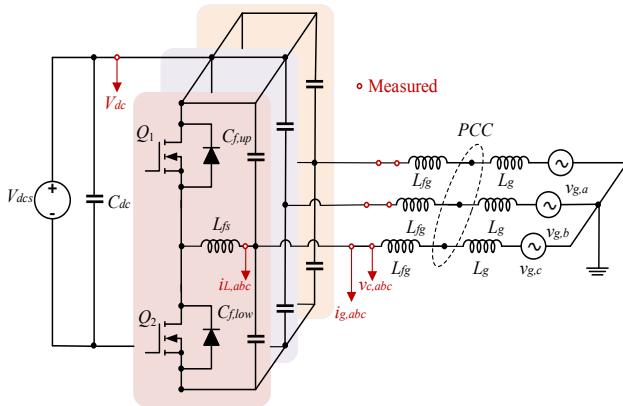

Fig. 2.   Topology of three-phase inverter system

Fig. 1 describes a general FDC scheme for it, variables in different colors denote the corresponding control cards they belong. Unlike centralized control in [1], in this structure, each phase needs a separate low-cost DSP control card (control card A, B, C for phase a, b, c) to allow calculations in local level done in parallel. And control of each phase contains two layers as in [1], central level control and local level control. Central level control collects its own measured data and the key data from the other two phases by communication, and then passes the needed

voltage references to its own local level. Afterwards, local level calculated the duty cycle d and switching frequency f_{sw}, and sends these to switches Q in corresponding phases of inverter. f_{sw} is calculated based on variable frequency soft-switching (In Fig.3, VFCSS) [13].

In Fig.1, different background color denotes the place where control occurs. For instance, purple background shows the control on control card A.

Take phase n ($\Phi n = \Phi a$ or Φb or Φc, and this phase is controlled by DSP control card N) as an instance, detailed control strategies are shown in Fig.3. Central level is based on PI control described in [1] to allow measured data (in red color) tracking references (in purple color), where references in purple color are given. Before that, three-phase measured data needs to be transformed to $dq0$ data.

In Fig.3, red background color denotes central control, and yellow background color denotes local control. Q represents switches. Phase θ can be got from phase-locked loop (PLL).
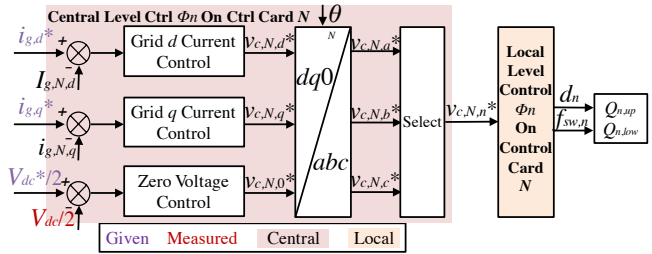

Fig. 3.   Detailed control strategy for Φn

4313

In Fig.1 and Fig.3, local level control can be any control strategies, so it can be seen as a generalized FDC scheme.

Key data of Φn at the kth control period is denoted as $\boldsymbol{S}_{nk}$, where

$$\boldsymbol{S}_{nk} = (i_{g,n}(k),\ v_{c,n}(k),\ i_{L,n}(k))^T \tag{1}$$

$\boldsymbol{S}_{nk}$ are selected based on the variables needed for calculation of duty cycle and switching frequency.

The data Φn receives from Φj considering delay τ will be denoted as $\boldsymbol{S}_j(k-\tau_{jn})$ as input side in Fig.1, where

$$\boldsymbol{S}_j(k-\tau_{jn}) = \boldsymbol{S}_{g,n}(k-\tau_{jn}(k)) \tag{2}$$

and $\tau_{jn}(k) = 0$ if $n = j$.

Central level of Φn collects data and combines it as $i_{g,N,abc}(k)$, $v_{c,N,abc}(k)$, $i_{L,N,abc}(k)$, where each of them contains non-delayed data from its own phase and 'delayed' data (τ_{jn} can be 0) from the other two phases. State-space equation of Φn can be derived by substitution [9],

$$\begin{cases} z_n(k+1) = \mathbf{A}'_n z_n(k) + \mathbf{B}'_n u_n(k) \\ y_n(k) = \mathbf{C}'_n z_n(k) \end{cases} \tag{3}$$

Where new state

$$z_n(k) = (x_n(k),\ u_n(k-\tau_{up}),\ u_n(k-\tau_{up}-1),\dots,\ u_n(k-1))^T \tag{4}$$

Input $u_n(k)$ contains reference $r(k)^*$, $V_{dc}(k)/2$, $\boldsymbol{S}_{nk}$, and delayed data form other two phases. In it,

$$r(k)^* = (i_{g,d}(k)^*,\ i_{g,q}(k)^*)^T \tag{5}$$

Based on equation (3), it is unnecessary to know all delays, we only need to know upper bound of all delays, τ_{up}, then we can design corresponding control strategies. $\mathbf{A}_n'$, $\mathbf{B}_n'$, $\mathbf{C}_n'$ can be derived by original $\mathbf{A}_n$, $\mathbf{B}_n$, $\mathbf{C}_n$ as in reference [9], where original equation is

$$\begin{cases} x_n(k+1) = \mathbf{A}_n x_n(k) + \mathbf{B}_n u_n(k) \\ y_n(k) = \mathbf{C}_n x_n(k) \end{cases} \tag{6}$$

Reference [1] provides a specific instance for state equations of three-phase inverter systems, where $\mathbf{A}_n$, $\mathbf{B}_n$, $\mathbf{C}_n$ can be derived. If $\tau_{up} = 2$, equation (3) can be written as

$$\begin{bmatrix} x_n(k+1) \\ u_n(k-2+1) \\ u_n(k-1) \end{bmatrix} = \begin{bmatrix} \mathbf{A_n} & \mathbf{B_n} & \mathbf{0} \\ \mathbf{0} & \mathbf{0} & \mathbf{I} \\ \mathbf{0} & \mathbf{0} & \mathbf{0} \end{bmatrix} \begin{bmatrix} x_n(k) \\ u_n(k-2) \\ u_n(k-1) \end{bmatrix} + \begin{bmatrix} \mathbf{0} \\ \mathbf{I} \end{bmatrix} u_n(k) \tag{7}$$

where

$$\mathbf{A}'_n = \begin{bmatrix} \mathbf{A_n} & \mathbf{B_n} & \mathbf{0} \\ \mathbf{0} & \mathbf{0} & \mathbf{I} \\ \mathbf{0} & \mathbf{0} & \mathbf{0} \end{bmatrix},\ \mathbf{B}'_n = \begin{bmatrix} \mathbf{0} \\ \mathbf{I} \end{bmatrix},\ \mathbf{C}'_n = \mathbf{C}_n \tag{8}$$

III. CONNECTION RESCHEDULING AND CONTROL BANDWIDTH ANALYSIS

Connection rescheduling (CR) is based on ideas that data from some phases are not necessary in certain control periods, so only part of data will be sent in order to decrease communication delays and theoretical communication bitrate requirement for the systems, which can decrease time delays. Besides, connection topology changes will be used to compensate the effects of lacking these data, without increasing local level calculation time. Typically, vital data is the variables needed for calculation of duty cycle and switching frequency, which is $\boldsymbol{S}_{nk}$ in this paper.

Fig.4 describes three connection topologies of the 3 control cards. Fig.4(a) is FDC without CR, so in every control period, 2 sets of paralleled transmissions will be needed. Yet, Fig.4(b) shows FDC-CR strategy, control card on each phase will only receive updated data from one of the phases (except itself) in one control period, and data from the other phase is based on previous control period. In this case, only one set of transmissions is needed in one control period. In other words, corresponding delays can be half. Fig.4(c) is Central-distributed control in [5].

As for FDC-CR, in odd and even control period k_o and k_e. Take Φa as an instance, input

$$\begin{cases} u_a(k) = (r*(k),\ \boldsymbol{S}_a(k),\ \boldsymbol{S}_c(k-1),\ V_{dc}(k)/2)^T, & k = k_o \\ u_a(k) = (r*(k),\ \boldsymbol{S}_a(k),\ \boldsymbol{S}_b(k-1),\ V_{dc}(k)/2)^T, & k = k_e \end{cases} \tag{9}$$

Suppose delay for sending or receiving one single float data by every channel is equal and fixed, denoted as τ_0. τ_0 consists of packet transmission latency and node-to-node (n2n) latency, because n2n latency is typically in ns [5], which can be neglected, so

$$\tau_0 \approx 32\,/\,\mathrm{BR} \tag{10}$$

where BR is the communication bitrate when one controller sending data to the other controller.

(a) FDC (b) FDC-CR

4314
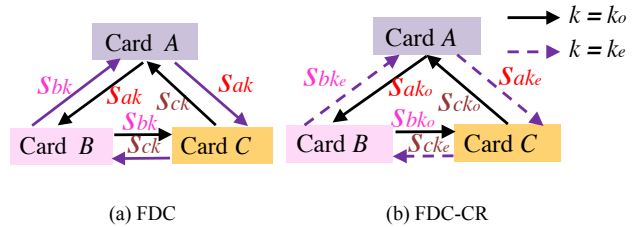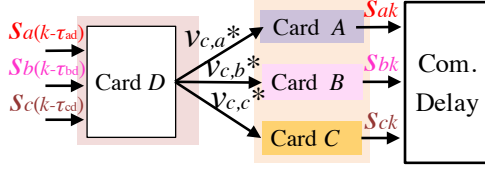
(c) Central-distributed control

Fig. 4. Connection topologies for different control strategies

Let t_{cl} and t_{lc} denote time for central and local level control. Suppose well synchronized, in each control period, total calculation time and BR requirements for different control topologies are:

$$\begin{cases} t_{cen} = t_{cl} + 3t_{lc} + 3t_{ADC} \\ t_{cen-dis} = t_{cl} + t_{lc} + t_{ADC} + 16\tau_0 \\ t_{fdc} = t_{cl} + t_{lc} + t_{ADC} + 12\tau_0 \\ t_{fdc-cr} = t_{cl} + t_{lc} + t_{ADC} + 6\tau_0 \end{cases} \quad (11)$$

and

$$\begin{cases} 16 \times 32/BR_{cen-dis} \leq 1/f_{crtl_{cen-dis}} - (t_{cl} + t_{lc} + t_{ADC}) \\ 12 \times 32/BR_{fdc} \leq 1/f_{ctrl_{fdc}} - (t_{cl} + t_{lc} + t_{ADC}) \\ 6 \times 32/BR_{fdc-cr} \leq 1/f_{ctrl_{fdc-cr}} - (t_{cl} + t_{lc} + t_{ADC}) \end{cases} \quad (12)$$

Let t_{fdc-cr}, BR_{fdc-cr} and $f_{ctrl_{fdc-cr}}$ denote total calculation time, BR and control frequency when using FDC-CR. Based on above equations, centralized control (t_{cen}) only uses one control card to control all [1][2], and everything needs to be done in serial, so it can be time-consuming; Central-distributed control ($t_{cen-dis}$) [5] in Fig. 4(c) needs 4 control cards, one card more than FDC, and $t_{cen-dis}$ is always larger than t_{fdc}, so we prefer FDC than central-distributed control; FDC (t_{fdc}) in Fig.4(a) and FDC-CR (t_{fdc-cr}) can save cost of one card because it only needs 3. Since BW equals to $1/t$, BW of FDC is always higher than central-distributed control. If t_{lc} is large (e.g. 10μs), FDC will be better than centralized control. Besides, based on above equations, FDC-CR can decrease delays and BR lower bound to 50% of FDC and 37.5% of central-distributed one.

By the way, if we use the strategy in [9] to attenuate delay, i.e. writing a new objective function considering delays based on H-infinity control, it will not work well because the new objective function will contain $z_n(k)$ in equation (4) rather than just $x_n(k)$, which will largely increase the difficulties of calculation. It can show the advantages of CR, too.

IV. VERIFICATION

An experimental test for the centralized control described in reference [1] was finished to get supported data. It is based on one TMS320F28379D microcontroller, showing t_{cl} = 15μs and measured time t_{ADC} = 0.39μs. Study cases below adopts OBE-MPC as an instance of local level control, t_{lc} = 11μs [2].

A three-phase inverter system is built in Simulink to verify above strategies, where V_{dcs} = 800V, d axis gird current reference $i_{g,d}*$ is a step function starting at 0.04s with amplitude 166.7A, which can reflect input active power. q axis gird current reference $i_{g,q}*$ = 0, which can reflect input reactive power. Inverter control is enabled at 0.02s.

Control results of four strategies are shown in Fig.5.
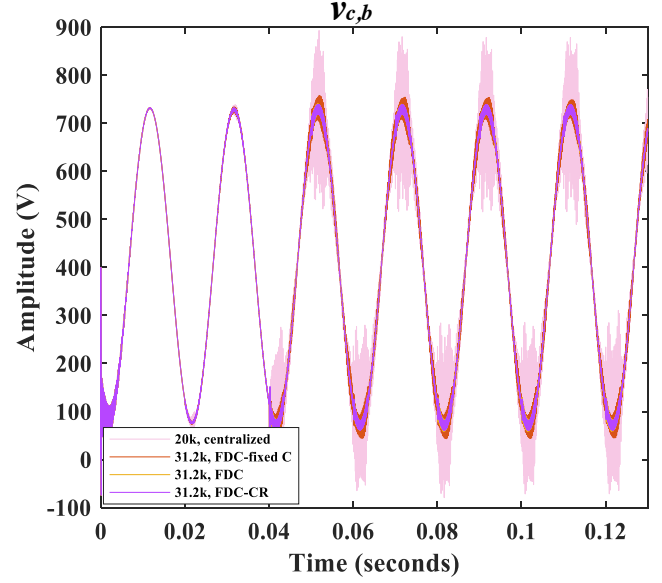
(a) capacitor voltage Φb
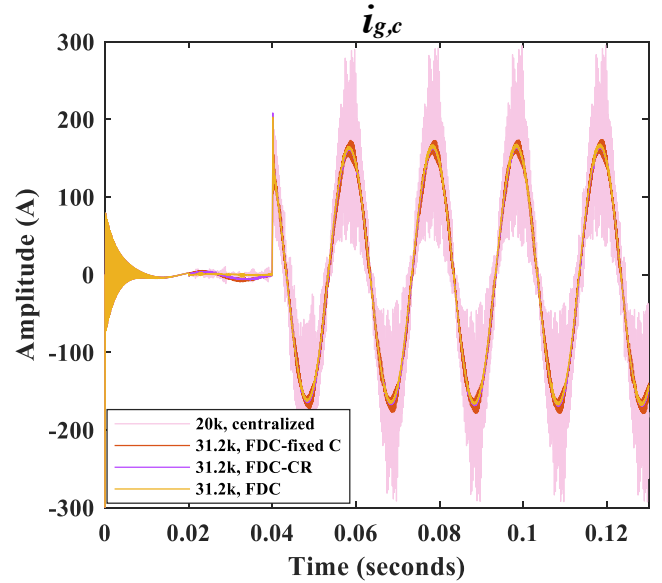
(b) grid current Φc

Fig. 5. Control results

Detailed simulation parameters are shown in Table I, notations are consistent with Fig.2.

4315

Name	Notations	Values(unit)
DC side capacitor	C_{dc}	20μF
Filter inductor	L_{fs}	5.4μH
Filter capacitor	C_f	40μF
Grid side filter inductor	L_{fg}	5μH
Grid side inductor	L_g	20μH
Grid frequency	f_g	50Hz
Grid voltage (RMS)	V_g	400V
Upper bound of switching frequency	$f_{sw,up}$	500kHz

Based on previous theoretical analysis in equation (11), (12) and data in first two paragraphs in this section, control BW for centralized control is 20kHz, for FDC is 33kHz. We choose 20kHz and 31.2kHz as control frequency f_{ctrl} for each. BR for FDC-CR, FDC (no delay), and central-distributed (no delay) need to be larger than 46 Mbit/s, 92 Mbit/s and 123 Mbit/s respectively. BR of SPI bus can be up to 50 Mbit/s, which is feasible for FDC-CR. Considering SPI bus is easy to be interfered by noise and disturbance, a differential structure can be used.

Average total harmonic distortion (THD) of grid current $i_{g,abc}$ and capacitor voltage $v_{c,abc}$ for FDC-CR is 1.0% and 2.1%, for FDC is 0.9% and 2.1%, for FDC-fixed C is 3.9% and 4.3%, which are less than 5%, satisfying requirement for power qualities. Yet, for 20kHz centralized control, THD is above 10%, showing the control is not stable, which indicates the shortage of lower BW.

FDC-CR can increase control BW by 50% compared with centralized control, and can decrease BR lower bound required by communication to 50% of FDC's and 37.5% of central-distributed one without decreasing output power quality, because 'FDC-CR' and 'FDC' gets nearly identical voltage and current output, their figures overlap in Fig.5. Besides, compare 'FDC-CR' with 'FDC fixed C', it shows real-time connection topology rescheduling can largely decrease THD and well suppress delays' effects. Last but not least, the system is stable and no steady-state errors are shown in capacitor voltage and grid current when using FDC-CR, so this control strategy works well.

Even though two extra control cards are needed when using FDC-CR contrary to central control, yet, because FDC can get way get better power qualities, which is the priority of this control, so these costs are worthy.

V. CONCLUSION

In this paper, a general FDC-CR scheme was firstly designed for the three-phase grid-tied power inverter systems. Theoretical analysis and simulation results based on supported data provided by experimental test had verified that this strategy could increase control BW by at least 50% compared with centralized control, if a time-consumed (i.e. calculation time is 10μs) local level controller is needed to get way better transient process and

power qualities. Besides, this strategy can always well attenuate delays' effects and decrease the theoretical minimum communication BR required by the system to 50% of FDC's and 37.5% of central-distributed one, without decreasing any output power qualities (this paper focuses on control strategy for grid-tied power inverter systems considering delay compensation, it does not research on detailed techniques or strategies about communication itself).

In future, the DC voltage source in Fig.2 can be replaced by RES. Two or three of these inverter systems can be connected in parallel and then connected with power grids. Droop control can be added as a local control strategy and energy storage units can also be considered. As a result, it can save more energies.

REFERENCES

[1] L. Zhou, W. Wang, and M. Preindl, "Modular Model-Predictive Control With Regulated Third-Harmonic Injection for Zero-Sequence Stabilized LCL Inverter" *IEEE Transactions on Industrial Applications*, vol. 58, no. 6, pp. 7634-7647, Nov. 2023.

[2] L. Zhou, M. Eull, and M. Preindl, "Optimization-Based Esti and model Predictive Control for High Performance, Low Cost Software-Defined Power Electronics," *IEEE Transactions on Power Electronics*, vol. 38, no. 1, pp. 1022-1035, Jan. 2023.

[3] L. Guo, Z. Xu, Y. Li, Y., and et al., "An inductance online identification-based model predictive control method for grid-connected inverters with an improved phase-locked loop," *IEEE Trans. Transport. Electrific.*, vol. 8, no. 2, pp. 2695–2709, Jun. 2022.

[4] C.Xue, D.Zhou, and Y.Li, "Hybrid model predictive current and voltage control for LCL-filtered grid-connected inverter," *IEEE Trans. Emerg. Sel. Topics Power Electron.*, vol. 9, no. 5, pp. 5747–5760, Oct. 2021.

[5] Y. Rong, Synchronized Communication Network for Real-Time Distributed Control Systems in Modular Power Converters, Virginia Polytechnic Institute and State University, Virginia, 2022.

[6] T M. Zaery, P. Wang, and et al., "Fully Distributed Controller for Economic Load Sharing of DC Microgrid Clusters", *2020 IEEE Applied Power Electronics Conference and Exposition (APEC)*, pp. 597-602

[7] S. K. Sahoo, A. K. Sinha and N. K. Kishore, "Control Techniques in AC DC and Hybrid AC–DC Microgrid: A Review", *IEEE J. Emerging Sel. Topics in Power Electron.*, vol. 6, no. 2, pp. 738-759, June 2018.

[8] Y. Chen, and J. Anderson, "System level synthesis with state and input constraints," in *Proc. IEEE CDC*, 2019, pp. 5258–5263.

[9] Y. Li, C. Lu, and Y. Tang, "Dynamic Control and Time-Delayed Channel Scheduling Co-design for Voltage Control in Active Distribution Networks," *IEEE Transactions on Smart Grid*, vol. 14, no. 8, pp. 1-12, Aug. 2021.

[10] T. V. Tran, K. K., and J.-S. Lai, "Optimized active disturbance rejection control with resonant extended state observer for grid voltage sensorless *LCL*-filtered inverter," *IEEE Trans. Power Electron.*, vol. 36, no. 11, pp. 13317–13331, Nov. 2021.

[11] C. Cheng, S. Xie, J. Xu, and Q. Qian, "State-and-disturbance-observer-based current control scheme for LCL-filtered single-phase grid-tied inverters under nonideal conditions," *IEEE Trans. Emerg. Sel. Topics Power Electron.*, vol. 10, no. 1, pp. 336–348, Feb. 2022.

[12] R. Errouissi and A. Al-Durra, "Design of PI controller together with active damping for grid-tied LCL-filter systems using disturbance-observer-based control approach," *IEEE Trans. Ind. Appl.*, vol. 54, no. 4, pp. 3820–3831, Jul./Aug. 2018.

[13] Y. A. Fahmy, and M. Preindl, "Circulating Current Control Enabling Parallel Grid Tied Inverter Operation for EV Fast Charging Stations," in 2023 IEEE Transportation Electrification Conference & Expo (ITEC), 2023, pp. 1-6.